National
Semiconductor

400029.2

Interface
Databook

- *Transmission Line Drivers and Receivers*
- *Bus Transceivers*
- *Peripheral Power Drivers*
- *Display Drivers*
- *Memory Support*
- *Microprocessor Support*
- *Level Translators and Buffers*
- *Frequency Synthesis*
- *Hi-Rel Interface*

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Introduction

Since its creation in 1973, National Semiconductor's Interface design and production teams have produced technically advanced products unparalleled in the semiconductor industry.

Growing from a line of eary drivers and receivers, which pioneered the introduction of the TRI-STATE® function, National Semiconductor's Interface product line today is the most comprehensive available—with over 200 devices in a variety of product categories.

Based on its advanced design and process capabilities, National's Interface product line includes:

- The industry's most advanced RS-232 drivers and receivers
- The industry's most advanced RS-422 drivers, receivers and transceivers
- The industry's most advanced RS-485 drivers, receivers and transceivers
- The industry's only offering of over 16 devices incorporating power up/down glitch-free protection
- The industry's first Trapezoidal™ bus transceiver
- The industry's first transceivers for the Future Bus standard
- The industry's first fault protected peripheral driver incorporating a major breakthrough in current sensing and shutdown circuitry.

In addition to the detailed Interface product datasheets included in this databook, complete product selection guides can be found at the beginning of each section for quick reference.

The Interface Appendix supplies helpful application notes, terms and definitions, cross references, design and process information and package information.

These Interface devices support and complement National's VLSI Advanced Peripheral product families. These Advanced Peripherals Processing Solutions are families of VLSI peripheral circuits designed to serve a variety of applications. The products are especially well suited for microcomputer and microprocessor based systems such as graphic workstations, personal computers, and many others. National Semiconductor's Advanced Peripheral devices are fully described in a series of databooks and handbooks.

Among the books are the following titles:

GRAPHICS
MASS STORAGE
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All the Advanced Peripheral products currently provided by National Semiconductor and their appropriate Advanced Peripheral Databook title are listed in a section following the Table of Contents of this databook.

For more information on National Semiconductor's INTERFACE and Advanced Peripheral products contact your local National authorized sales representative or distributor.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
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Section 1

Transmission Line Drivers/Receivers

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National Semiconductor

Transmission Line Drivers/Receivers

The common purpose of transmission line drivers and receivers is to transmit data quickly and reliably through a variety of environments over electrically long distances. This task is complicated by the fact that externally introduced noise and ground shifts can severely degrade the data.

The connection between two elements in a system should be considered a transmission line if the transmitted signal takes longer than twice its rise or fall time to travel from the driver to the receiver.

Single-Ended Data Transmission

In data processing systems today there are two basic means of communicating between components. One method is single-ended, which uses only one signal line for data transmission, and the other is differential, which uses two signal lines.

The Electronics Industry Association (EIA) has developed several standards to simplify the interface in data communications systems.

RS-232

The first of these, RS-232, was introduced in 1962 and has been widely used throughout the industry. RS-232 was developed for single-ended data transmission at relatively slow data rates (20 kBaud) over short distances (up to 50 ft.).

RS-423

With the need to transmit data faster and over longer distances, RS-423, a newer standard for single-ended applications, was established. RS-423 extends the maximum data rate to 100 kBaud (up to 30 ft.) and the maximum distance to 4000 feet (up to 1 kBaud). RS-423 also requires high impedance driver outputs with power off so as not to load the transmission line.

Differential Data Transmission

When transmitting at very high data rates, over long distances and through noisy environments, single-ended transmission is often inadequate. In these applications, differential data transmission offers superior performance. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line.

RS-422

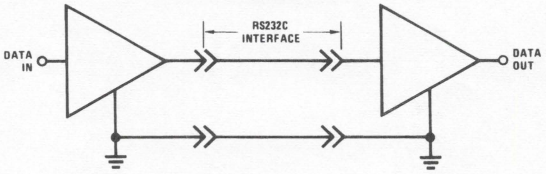
RS-422 was defined by the EIA for this purpose and allows data rates up to 10 MBaud (up to 40 ft.) and line lengths up to 4000 feet (up to 100 kBaud).

Drivers designed to meet this standard are well suited for party-line type applications where only one driver is connected to, and transmits on, a bus and up to 10 receivers can receive the data. While a party-line type of application has many uses, RS-422 devices cannot be used to construct a truly multipoint bus. A multipoint bus consists of multiple drivers and receivers connected to a single bus, and any one of them can transmit or receive data.

RS-485

To meet the need for truly multipoint communications, the EIA established RS-485 in 1983. RS-485 meets all the requirements of RS-422, but in addition, this new standard allows up to 32 drivers and 32 receivers to be connected to a single bus—thus allowing a truly multipoint bus to be constructed.

RS-232C Application



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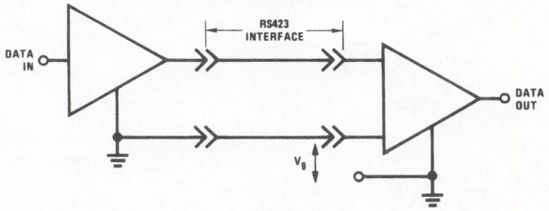
EIA RS-423 Application



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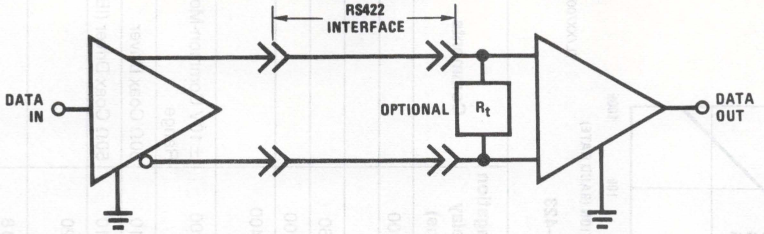
Differential Data Transmission (Continued)

EIA RS-422 Application



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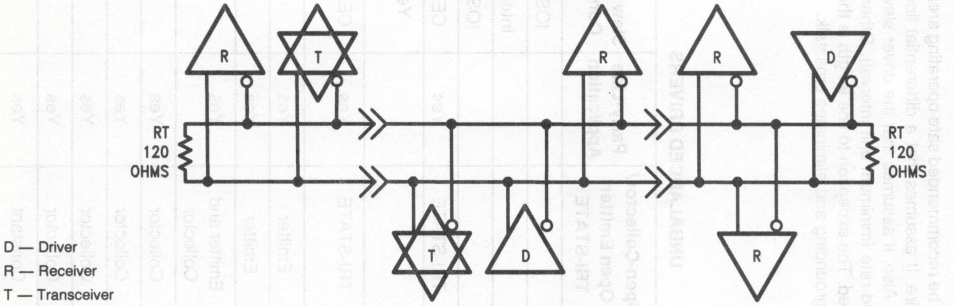
The key features of RS-485:

- Implements a truly multipoint bus consisting of up to 32 drivers and 32 receivers
- An extended common-mode range for both drivers and receivers in TRI-STATE and with power off (−7V to +12V)
- Drivers can withstand bus contention and bus faults

National Semiconductor produces a variety of drivers, receivers, and transceivers for these four very popular transmission standards and numerous other data transmission requirements.

Shown below is a table that highlights key aspects of the EIA Standards. More detailed comparisons can be found in the various application notes in Section 1.

RS-485 Application



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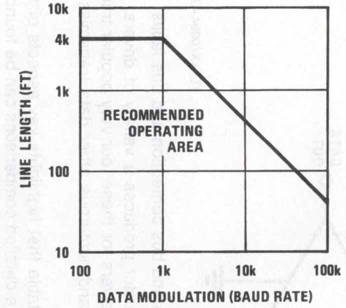
Specification		RS-232C	RS-423	RS-422	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers
Maximum Cable Length		50 feet	4000 feet	4000 feet	4000 feet
Maximum Data Rate		20 kb/s	100 kb/s	10 Mb/s	10 Mb/s
Driver Output Maximum Voltage		±25V	±6V	−0.25V to +6V	−7V to +12V
Driver Output Signal Level	Loaded	±5V	±3.6V	±2V	±1.5V
	Unloaded	±15V	±6V	±5V	±5V
Driver Load Impedance		3 kΩ to 7 kΩ	450Ω min	100Ω	54Ω
Maximum Driver Output Current (High Impedance State)	Power On	— —	— —	— —	±100 μA
	Power Off	$V_{MAX}/300\Omega$	±100 μA	±100 μA	±100 μA
Slew Rate		30 V/μs max	Controls Provided	— —	— —
Receiver Input Voltage Range		±15V	±12V	−7V to +7V	−7V to +12V
Receiver Input Sensitivity		±3V	±200 mV	±200 mV	±200 mV
Receiver Input Resistance		3 kΩ to 7 kΩ	4 kΩ min	4 kΩ min	12 kΩ min

Line length is a function of data rate (baud) and slew rate. The recommended safe operating area (line length vs baud rate) is shown below for 24 AWG wire. It assumes that a differential line receiver is used which is referenced at the driver ground. Also, it assumes that the driver slew rate is between 0.1 to 0.3 times the reciprocal of the baud rate (minimum unit interval). Otherwise, line lengths greater than 50 feet are not recommended. The exception to line length is the 360 I/O coaxial interface. The coaxial provides improved grounding and eliminates crosstalk.



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RS-423

UNBALANCED DRIVERS

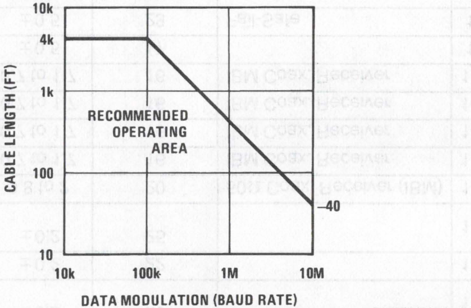
Standard	Device Number		Circuits Per Package	Power Supplies (V)	Open-Collector/ Open Emitter TRI-STATE	Party-Line Application	Slew Rate Control	Output Current (mA)	Output Voltage (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-232	DS1488		4	±9 or ±15			IOS/C	±6	±6 or ±9	200		1-13
RS-232	DS14C88			±9 or ±15			Internal	±6	±7 or ±11			1-17
RS-232	DS75150		2	±12			IOS/C	±10	±5	60		1-149
RS-423	DS3691	DS1691A	4	+5 or ±5	TRI-STATE	Yes	CEXT	±20	±2	200		1-81
RS-423	DS9636AC/ μA9636AC	DS9636AM/ μA9636AM	2	±12			Yes	±60	±6	1400		1-223
MIL-188-114	DS3692	DS1692	4	+5 or ±5	TRI-STATE	Yes	CEXT	±20	±2	200	±10V Common-Mode Range	1-87
360 I/O	DS75121	DS55121	2	5	Emitter	Yes		−100	2.4	10	50Ω Coax Driver	1-134
360 I/O	DS75123		2	5	Emitter	Yes		−100	2.4	10	50Ω Coax Driver (IBM)	1-136
	DS75450		2	5	Emitter and Collector	Yes		300	0.7	20		3-41
	DS75451	DS55451	2	5	Collector	Yes		300	0.7	18		3-41
	DS75452	DS55452	2	5	Collector	Yes		300	0.7	26		3-41
	DS75453	DS55453	2	5	Collector	Yes		300	0.7	18		3-41
	DS75454	DS55454	2	5	Collector	Yes		300	0.7	27		3-41
	DS75110A/ μA75110A	DS55110A/ μA55110A	2	±5	Constant Current	Yes		12		15		1-112

UNBALANCED RECEIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Input Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-232	DS1489		4	5		CEXT	250	±25	3	30		1-23
RS-232	DS1489A		4	5		CEXT	1150	±25	3	30	Preferential in Applications to DS1489	1-23
RS-232	DS14C89		4	5				±25	3			1-17
RS-232	DS75154		4	5 or 15		CEXT	800	±25	3	22		1-153
RS-232		DS9627/μA9627	2	±12	Strobed				±3	250		1-219
RS-423	DS26C32		4	5	TRI-STATE							1-37
RS-423	DS26F32C	DS26F32M	4	5	TRI-STATE		30	±7	±0.2	22		1-40
RS-423	DS26LS32C	DS26LS32M	4	5	TRI-STATE		100	±7	±0.2	17		1-44
RS-423	DS26LS32AC		4	5	TRI-STATE		100	±7	±0.2	23	Fail-Safe	1-44
RS-423	DS3486		4	5	TRI-STATE		100	±15	±0.2	25		1-54
RS-423	DS34C86		4	5	TRI-STATE							1-47
RS-423	DS34F86	DS35F86	4	5	TRI-STATE			±7	±0.2	22		1-50
RS-423	DS88C20	DS78C20	2	5	Strobed	CEXT	50	±25	±0.2	50		1-172
RS-423	DS88C120	DS78C120	2	5	Strobed	CEXT	50	±25	±0.2	50	Fail-Safe	1-187
RS-423	DS88LS120	DS78LS120	2	5 to 15	Strobed	CEXT	50	±25	±0.2	50	Fail-Safe	1-195
RS-423	DS9637AC/ μA9637AC	DS9637AM/ μA9637AM	2	5								1-227
RS-423	DS9639AC/ μA9639AC		2	5								1-236
RS-423	DS96F173C	DS96F173M	4	5	TRI-STATE		50	+12/−7	±0.2	22		1-250
RS-423	DS96173C/ μA96173C	DS96173M/ μA96173M	4	5	TRI-STATE		50	+12/−7	±0.2	25		1-255
RS-423	DS96F175C	DS96F175M	4	5	TRI-STATE		50	+12/−7	±0.2	22		1-250
RS-423	DS96175C/ μA96175C	DS96175M/ μA96175M	4	5	TRI-STATE		50	+12/−7	±0.2	25		1-255
360 I/O	DS75124		3	5	Strobed		400	7	0.8 to 2	20	50Ω Coax. Receiver (IBM)	1-138
360 I/O	DS75125		7	5				−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-141
360 I/O	DS75127		7	5				−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-141
360 I/O	DS75128		8	5	Strobed			−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-145
360 I/O	DS75129		8	5	Strobed			−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-145
	DS26LS33C	DS26LS33M	4	5	TRI-STATE		200	±15	±0.5	17		1-44
	DS26LS33AC		4	5	TRI-STATE		200	±15	±0.5	23	Fail-Safe	1-44
		DS9615/μA9615	2	5		Yes		±15	±0.5	75		1-129
		DS9622/μA9622	2	+5 −10	Strobed			±10		50		1-216

BALANCED DIFFERENTIAL TRANSMISSION LINE DRIVERS AND RECEIVERS

The balanced or differential scheme of data transmission is preferred for applications incorporating high data rates and long transmission lines in the presence of high common-mode noise. Induced signals appear as common-mode levels and are rejected by the differential line receiver.



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RS-422

BALANCED DIFFERENTIAL TRANSMISSION LINE DRIVERS AND RECEIVERS (Continued)

BALANCED DRIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Open Collector	Party-Line Application	TRI-STATE	V_{OH} (V) I_{OH} (mA)	V_{OL} (V) I_{OL} (mA) (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-422	DS26C31											1-27
RS-422	DS26F31C	DS26F31M	4	5		Yes	Yes	2.5/−20	0.5/20	15		1-31
RS-422	DS26LS31C	DS26LS31M	4	5		Yes	Yes	2.5/−20	0.5/20	15		1-34
RS-422	DS3487	DS3587	4	5		Yes	Yes	2.0/−50	0.5/48	15		1-66
RS-422	DS34C87											1-58
RS-422	DS34F87	DS35F87	4	5		Yes	Yes	2.5/−20	0.5/48	15		1-62
RS-422	DS3691	DS1691A	2	+5 or ±5		Yes	Yes	2/−20	−2/20	200		1-81
RS-422	DS8921, 21A		1	5		No	No	2.5/−20	0.5/20	12	Transceiver	1-202
RS-422	DS8922 DS8922A		2	5		Yes	Yes	2.5/−20	0.5/20	12	Dual Transceiver with Driver/Receiver Pair Disable	1-207
RS-422	DS8923 DS8923A		2	5		Yes	Yes	2.5/−20	0.5/20	12	Dual Transceiver with Separate Driver and Receiver Disables	1-207
RS-422	DS9638C/ μA9638C	DS9638M/ μA9638M	2	5				2.0/−40	0.5/40	20		1-232
RS-485	DS3695		1	5		Yes	Yes			15	Transceiver	1-98
RS-485	DS36F95	DS16F95	1	5		Yes	Yes			16		1-92
RS-485	DS3696		1	5		Yes	Yes			15	Transceiver with Line Fault Reporting	1-98
RS-485	DS3697		1	5		Yes	Yes			15	Repeater	1-98
RS-485	DS3698		1	5		Yes	Yes			15	Repeater with Line Fault Reporting	1-98
RS-485	DS75176A		1	5		Yes	Yes				Transceiver	1-158
RS-485	DS96F172C	DS96F172M	4	5		Yes	Yes			16		1-240
RS-485	DS96172/ μA96172		4	5		Yes	Yes			20		1-245
RS-485	DS96F174C	DS96F174M	4	5		Yes	Yes			16		1-240
RS-485	DS96174/ μA96174		4	5		Yes	Yes			20		1-245
RS-485	DS96176/ μA96176		1	5		Yes	Yes			20	Transceiver	1-260
RS-485	DS96F177C	DS96F177M	1	5		Yes	Yes				Repeater	1-267
RS-485	DS96177/ μA96177		1	5		Yes	Yes			20	Repeater	1-274

BALANCED DRIVERS

Standard	Device Number Commercial 0°C to +70°C	Device Number Military −55°C to +125°C	Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Common-Mode Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
RS-485	DS96F178C	DS96F178M	1	5		Yes	Yes				Repeater	1-267
	DS8830	DS7830	2	5		No	No	1.8/−40	0.5/40	10		1-176
	DS8831	DS7831	2	5		Yes	Yes	1.8/−40	0.5/40	10		1-180
	DS8832	DS7832	2	5		Yes	Yes	1.8/−40	0.5/40	10	DS8831 without V_{CC} Clamp Diode	1-180
	DS8924		4	5		Yes	Yes	2.0/−48	0.5/48	12		1-213
	DS75113	DS55113	2	5	Optional	Yes	Yes	2.0/−40	0.4/40	13		1-117
	DS75114	DS55114	2	5	Optional			2.0/−40	0.4/40	15		1-124
	DS9614/ μA9614		2	5							See DS55114	1-124
	MM88C29	MM78C29	2	5 or 15				2.9/−57	0.4/11	100		1-281
	MM88C30	MM78C30	2	5 or 15				2.9/−57	0.4/11	100		1-281

BALANCED RECEIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Common-Mode Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-422	DS26C32		4		TRI-STATE							1-37
RS-422	DS26F32C	DS26F32M	4	5	TRI-STATE		30	±7	±0.2	22		1-40
RS-422	DS26LS32C	DS26LS32M	4	5	TRI-STATE		100	±7	±200	17		1-44
RS-422	DS26LS32AC		4	5	TRI-STATE		100	±7	±200	17	Fail-Safe	1-44
RS-422	DS3486		4	5	TRI-STATE		80	±10	±200	17		1-54
RS-422	DS34C86		4	5	TRI-STATE							1-47
RS-422	DS34F86	DS35F86	4	5	TRI-STATE			±7	±0.2	22		1-50
RS-422	DS88C20	DS78C20	2	5 to 15	Strobed	Yes	50	±10	±200	60	Fail-Safe CMOS Compatible	1-172
RS-422	DS88C120	DS78C120	2	5 to 15	Strobed	Yes	50	±10	±200	60		1-187
RS-422	DS88LS120	DS78LS120	2	5	Strobed	Yes	50	±10	±200	50		1-195
RS-422	DS8921		1	5			50	±7	±200			1-202
RS-422	DS8921A		1	5			50	±7	±200		Low Skew	1-202
RS-422	DS8922		2	5	TRI-STATE		50	±7	±200			1-207
RS-422	DS8922A		2	5	TRI-STATE		50	±7	±200		Low Skew	1-207
RS-422	DS8923		2	5	TRI-STATE		50	±7	±200			1-207
RS-422	DS8923A		2	5	TRI-STATE		50	±7	±200		Low Skew	1-207
RS-422	DS9637AC/ μA9637AC	DS9637AM/ μA9637AM	2	5				±7	±0.2	25		1-227
RS-422	DS9639A/ μA9639A		2	5				±7	±0.2	85		1-236

BALANCED RECEIVERS Continued

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Common-Mode Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-485	DS3695		1	5	TRI-STATE		70	+12/−7	±200	22	Transceiver	1-98
RS-485	DS36F95	DS16F95	1	5	TRI-STATE		50	+12/−7	±0.2	16	Transceiver	1-92
RS-485	DS3696		1	5	TRI-STATE		70	+12/−7	±200	22	Transceiver with Line Fault Reporting	1-98
RS-485	DS3697		1	5	TRI-STATE		70	+12/−7	±200	22	Repeater	1-98
RS-485	DS3698		1	5	TRI-STATE		70	+12/−7	±200	22	Repeater with Line Fault Reporting	1-98
RS-485	DS75176A		1	5	TRI-STATE		70	+12/−7	±200		Transceiver	1-158
RS-485	DS96F173C	DS96F173M	4	5	TRI-STATE		50	+12/−7	±0.2	22		1-250
RS-485	DS96173/ μA96173		4	5	TRI-STATE		50	+12/−7	±0.2	25		1-255
RS-485	DS96F175C	DS96F175M	4	5	TRI-STATE		50	+12/−7	±0.2	22		1-250
RS-485	DS96175/ μA96175		4	5	TRI-STATE		50	+12/−7	±0.2	25		1-255
RS-485	DS96176		1	5	TRI-STATE		50	+12/−7	±0.2	25	Transceiver	1-260
	DS3603	DS1603	2	±5	TRI-STATE			±3	±25	17		1-69
	DS3650	DS1650	4	±5	TRI-STATE			±3	±25	10		1-73
	DS3652	DS1652	4	±5	Strobed			±3	±25	10		1-73
	DS8820	DS7820	2	5	Strobed	Yes		±15	±1000	40		1-163
	DS8820A	DS7820A	2	5	Strobed	Yes		±15	±1000	30		1-167
	DS75107	DS55107	2	±5	Strobed			±3	±25	17		1-205
	DS75108	DS55108	2	±5	Strobed			±3	±25	17		1-105
	DS75115	DS55115	2	5	Strobed	Yes		±15	±500	20		1-129
	DS75208		2	±5	Strobed			±3	±10	17		1-105
		DS9615/ μA9615	2	5		Yes		±15	±0.5	75	See DS55115	1-129
		DS9622/ μA9622	2	+5/−10	Strobed			±10		50		1-216

National Semiconductor

DS1488 Quad Line Driver

General Description

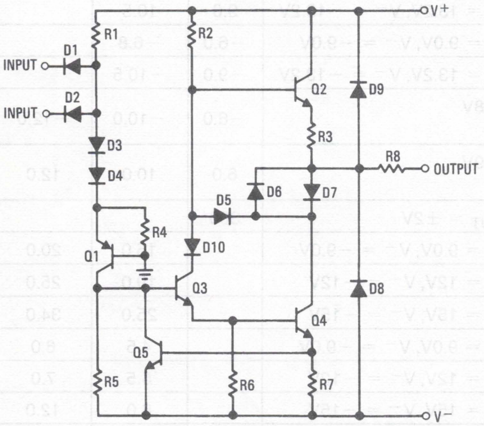
The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

Features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

Schematic and Connection Diagrams

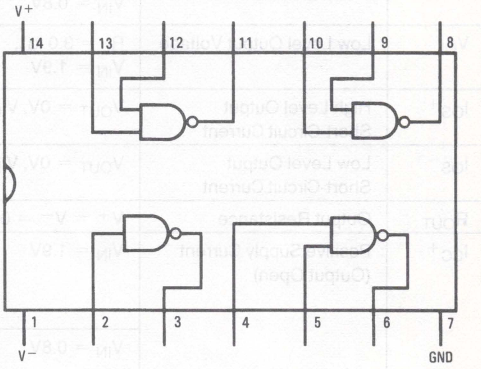
1/4 Circuit



V+
R1
R2
D1
INPUT
D2
INPUT
D3
D4
Q2
D9
R3
R8
OUTPUT
D6
D7
D5
R4
D10
Q1
Q3
D8
Q4
Q5
R5
R6
R7
V−

TL/F/5776-1

Dual-In-Line Package



V+
14
13
12
11
10
9
8
1
2
3
4
5
6
7
V−
GND

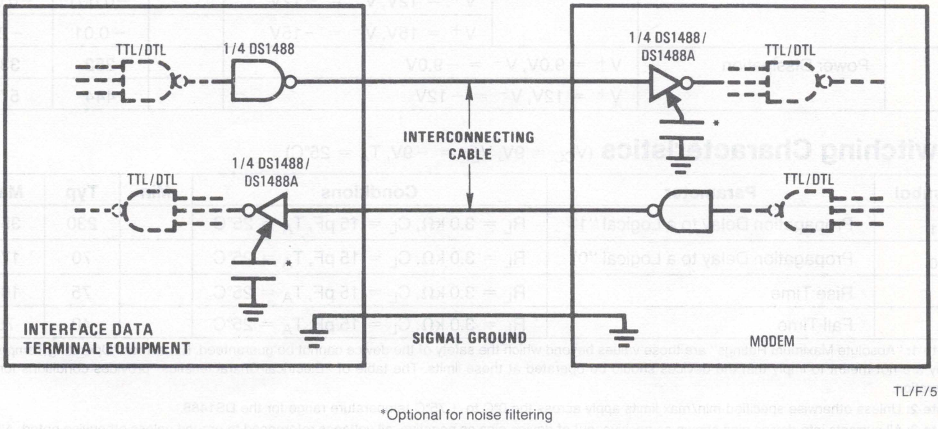
TL/F/5776-2

Top View

Order Number DS1488J, DS1488M or DS1488N
See NS Package Number J14A, M14A or N14A

Typical Applications

RS-232C Data Transmission



TTL/DTL
1/4 DS1488
1/4 DS1488/
DS1488A
TTL/DTL
*
INTERCONNECTING
CABLE
TTL/DTL
1/4 DS1488/
DS1488A
TTL/DTL
*
INTERFACE DATA
TERMINAL EQUIPMENT
SIGNAL GROUND
MODEM

TL/F/5776-3

*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V^+	±15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded DIP Package	1280 mW
SO Package	974 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 10.2 mW/°C above 25°C; derate SO package 7.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) $V_{CC}+ = 9V$, $V_{CC}- = -9V$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_{IL} = 3.0\ k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V$, $V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$	−6.0	−6.8		V
			$V^+ = 13.2V$, $V^- = -13.2V$	−9.0	−10.5		V
$I_{OS}{}^+$	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
$I_{OS}{}^-$	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
$I_{CC}{}^+$	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V$, $V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V$, $V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V$, $V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V$, $V^- = -15V$		8.0	12.0	mA
$I_{CC}{}^-$	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V$, $V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V$, $V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V$, $V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V$, $V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V$, $V^- = -9.0V$			252	333	mW
		$V^+ = 12V$, $V^- = -12V$			444	576	mW

Switching Characteristics ($V_{CC} = 9V$, $V_{EE} = -9V$, $T_A = 25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC} (\Delta T / \Delta V)$$

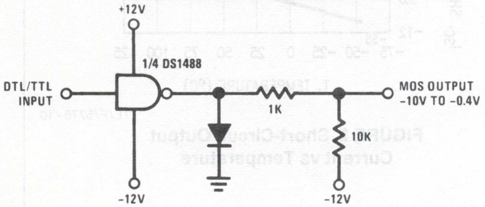
where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

See Typical Performance Characteristics.

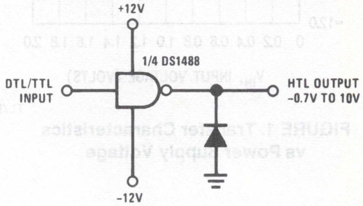
Typical Applications (Continued)

DTL/TTL-to-MOS Translator


+12V
1/4 DS1488
DTL/TTL INPUT
1K
MOS OUTPUT -10V TO -0.4V
10K
-12V
-12V

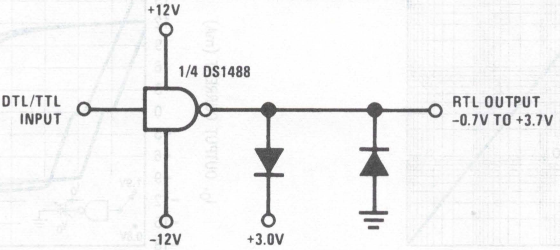
TL/F/5776-4

DTL/TTL-to-HTL Translator


+12V
1/4 DS1488
DTL/TTL INPUT
HTL OUTPUT -0.7V TO 10V
-12V

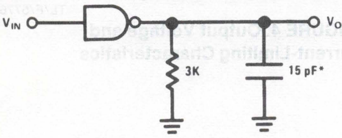
TL/F/5776-5

DTL/TTL-to-RTL Translator


+12V
1/4 DS1488
DTL/TTL INPUT
RTL OUTPUT -0.7V TO +3.7V
-12V
+3.0V

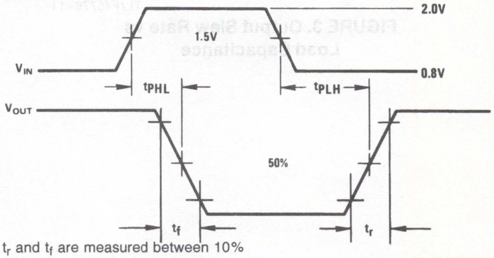
TL/F/5776-6

AC Load Circuit and Switching Time Waveforms


V_{IN}
V_{OUT}
3K
15 pF*

TL/F/5776-7

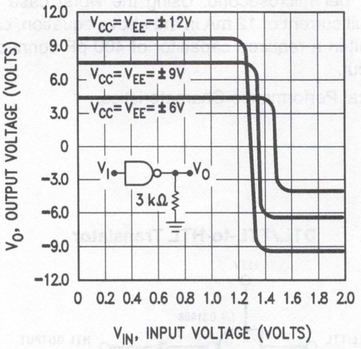
*C_L includes probe and jig capacitance.


2.0V
1.5V
V_{IN}
0.8V
t_{PHL}
t_{PLH}
V_{OUT}
50%
t_f
t_r

t_r and t_f are measured between 10% and 90% of the output waveform.

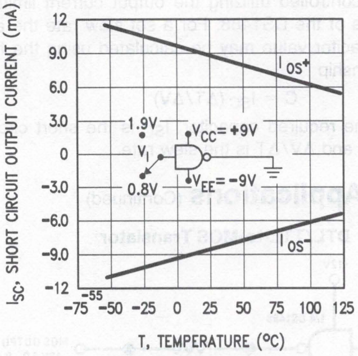
TL/F/5776-8

Typical Performance Characteristics $T_A = +25°C$ unless otherwise noted



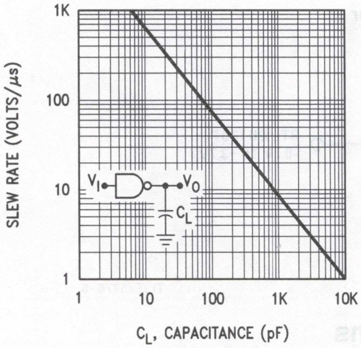
TL/F/5776-9

FIGURE 1. Transfer Characteristics vs Power Supply Voltage



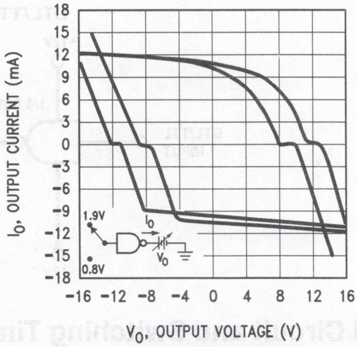
TL/F/5776-10

FIGURE 2. Short-Circuit Output Current vs Temperature



TL/F/5776-11

FIGURE 3. Output Slew Rate vs Load Capacitance



TL/F/5776-12

FIGURE 4. Output Voltage and Current-Limiting Characteristics

National Semiconductor

DS14C88/DS14C89A Quad CMOS Line Driver/Receiver

General Description

The DS14C88 and DS14C89A, pin-for-pin replacements for the DS1488/MC1488 and the DS1489/MC1489, are line drivers/receivers designed to interface data terminal equipment (DTE) with data communications equipment (DCE). These devices translate standard TTL or CMOS logic levels to/from levels conforming to RS-232-C and CCITT V.24 standards.

Both devices are fabricated in low threshold CMOS metal gate technology. They provide very low power consumption in comparison to their bipolar equivalents; 900 μA versus 26 mA for the receiver and 500 μA versus 25 mA for the driver.

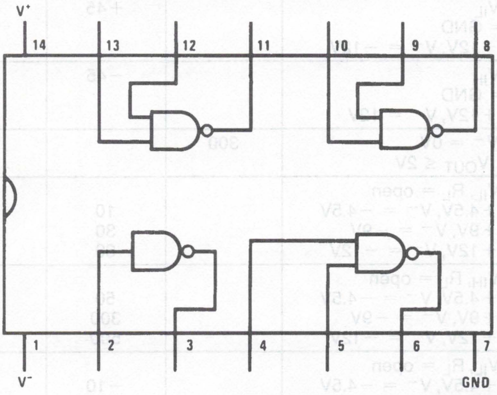
The DS14C88/DS14C89A simplify designs by eliminating the need for external capacitors. For the DS14C88, slew rate control in accordance with RS-232-C is provided on chip, eliminating the output capacitors. For the DS14C89A, noise pulse rejection circuitry eliminates the need for response control filter capacitors. When replacing the DS1489 with DS14C89A, the response control filter pins can be tied high, low or not connected.

Features

- Meets EIA RS-232-C and CCITT V.24 standard
- Low power consumption
- Pin-for-pin equivalent to DS1488/MC1488 and DS1489/MC1489
- Low Delay Slew
- DS14C88 Driver
  - — Power-off source impedance 300Ω min.
  - — Wide operating voltage range: 4.5V–12.6V
  - — TTL/LSTTL compatible
- DS14C89A
  - — Internal noise filter
  - — Inputs withstand ±30V
  - — Fail-safe operating mode
  - — Internal input threshold with hysteresis

Connection Diagrams

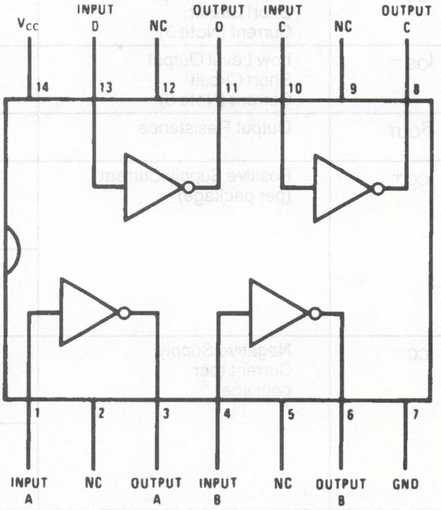
DS14C88 Dual-In-Line Package



TL/F/8508–9

Order Number DS14C88J, DS14C88N and DS14C88M
See NS Package Number J14A, M14A or N14A

DS14C89A Dual-In-Line Package



TL/F/8508–2

Order Number DS14C89AJ, DS14C89AM or DS14C89AN
See NS Package Number J14A, M14A or N14A

DS14C88 Quad CMOS Line Driver

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	$(V^+)+0.3V$ to GND $-0.3V$
Voltage at Any Output Pin (Note 2)	$-25V$ to $+25V$
Storage Temp.	$-65°C$ to $+150°C$
Power Dissipation	(See Note 2)
Junction Temperature	$+150°C$
Lead Temp. (Soldering 10 sec.)	$+260°C$
Supply Voltage V^+	$+13V$
V^-	$-13V$

This product does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max
Supply Voltage V^+ (GND = 0V)	$+4.5V$	$+12.6V$
Supply Voltage V^- (GND = 0V)	$-4.5V$	$-12.6V$
Temperature Range	0°C	+75°C

DC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V^+ = 4.5V$ to $12V$, GND = 0V, $V^- = -4.5V$ to $-12V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{IL}, I_{IH}	Maximum Input Current	V_{IN} = GND or V^+	−10	10	μA
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage	$V^+ \geq 7V, V^- \leq -7V$	GND	0.8	V
		$V^+ \leq 7V, V^- \geq -7V$	GND	0.6	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IL}$ $R_L = 3k\Omega$ or $7k\Omega$			
		$V^+ = +4.5V, V^- = -4.5V$	3.0		V
		$V^+ = +9V, V^- = -9V$	6.5		V
		$V^+ = +12V, V^- = -12V$	9.0		V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ $R_L = 3k\Omega$ or $7k\Omega$			
		$V^+ = +4.5V, V^- = -4.5V$		−3.0	V
		$V^+ = +9V, V^- = -9V$		−6.5	V
		$V^+ = +12V, V^- = -12V$		−9.0	V
$I_{OS}+$	High Level Output Short Circuit Current (Note 3)	$V_{IN} = V_{IL}$ V_{OUT} = GND $V^+ = +12V, V^- = -12V$		+45	mA
$I_{OS}-$	Low Level Output Short Circuit Current (Note 3)	$V_{IN} = V_{IH}$ V_{OUT} = GND $V^+ = +12V, V^- = 12V$		−45	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$ $-2V \leq V_{OUT} \leq 2V$	300		Ω
$I_{CC}+$	Positive Supply Current (per package)	$V_{IN} = V_{IL}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		10	μA
		$V^+ = +9V, V^- = -9V$		30	μA
		$V^+ = +12V, V^- = -12V$		60	μA
		$V_{IN} = V_{IH}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		50	μA
		$V^+ = +9V, V^- = -9V$		300	μA
		$V^+ = +12V, V^- = -12V$		500	μA
$I_{CC}-$	Negative Supply Current (per package)	$V_{IN} = V_{IL}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		−10	μA
		$V^+ = +9V, V^- = -9V$		−10	μA
		$V^+ = +12V, V^- = -12V$		−10	μA
		$V_{IN} = V_{IH}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		−30	μA
		$V^+ = +9V, V^- = -9V$		−30	μA
		$V^+ = +12V, V^- = -12V$		−60	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Power Dissipation N-Package: 1300 mW at 25°C, J-Package: 1000 mW at 25°C.

Note 3: $I_{OS}+$ and $I_{OS}-$ values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.

Note 4: For additional details on ESD, contact the local National Semiconductor Sales Office.

DS14C88 Quad CMOS Line Driver

AC Electrical Characteristics

T_A = 0°C to +75°C, V^+ = +4.5V to 12V, GND = 0V, V^- = −4.5V to −12V, R_L = 3 kΩ, C_L = 50 pF unless otherwise specified (Notes 5 and 6).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logic "1"	$V^+ = +4.5V, V^- = -4.5V$ $V^+ = +9V, V^- = -9V$ $V^+ = +12V, V^- = -12V$			6.0 5.0 4.0	μs μs μs
t_{pd0}	Propagation Delay to a Logic "0"	$V^+ = +4.5V, V^- = -4.5V$ $V^+ = +9V, V^- = -9V$ $V^+ = +12V, V^- = -12V$			6.0 5.0 4.0	μs μs μs
t_r, t_f	Output Rise and Fall Time (Note 7)		0.2			μs
t_{SK}	Typical Propagation Delay Skew	$V^+ = 12V, V^- = -12V$		400		ns
S_R	Output Slew Rate (Note 7)	R_L = 3 kΩ to 7 kΩ 15 pF ≤ C_L ≤ 2.5 nF			30	V/μs

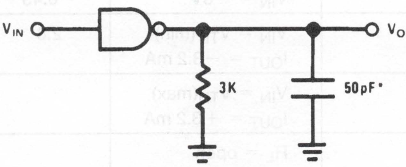
Note 5: AC input waveforms for test purposes:

$t_r = t_f \leq 20$ ns, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ (0.6V at $V^+ = 4.5$, $V^- = -4.5V$)

Note 6: Input rise and fall times must not exceed 5 μs.

Note 7: The output slew rate, rise time, and fall time are measured by measuring the time from +3.0V to −3.0V on the output waveforms.

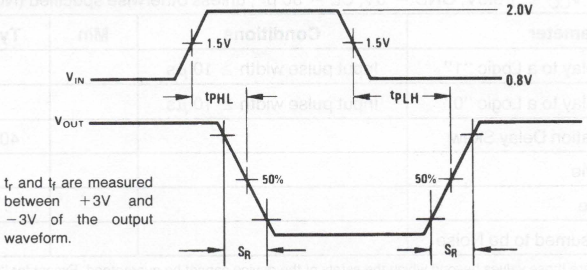
AC Load Circuit



*C_L includes probe and jig capacitance.

TL/F/8508-7

Switching Time Waveforms



2.0V
1.5V
1.5V
VIN
0.8V
tPHL
tPLH
VOUT
50%
50%
tr and tf are measured between +3V and −3V of the output waveform.
SR
SR

TL/F/8508-8

DS14C89A Quad CMOS Line Receiver

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	−30V to +30V
Voltage at Any Output Pin	(V_{CC}) +0.3V to GND − 0.3V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +75°C
Junction Temperature	+150°C
Lead Temp. (Soldering 10 sec)	+260°C
Supply Voltage	+6V

This product does not meet 2000V ESD rating. (Note 3)

Operating Conditions

	Min	Max
Supply Voltage V_{CC} (GND = 0V)	+4.5V	+5.5V
Temperature Range	0°C	+75°C

DC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $+4.5 \le V_{CC} \le 5.5V$, GND = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage		1.3		2.7	V
V_{TL}	Input Low Threshold Voltage		0.5		1.9	V
V_H	Typical Input Hysteresis			1.0		V
I_{IN}	Input Current	$V_{IN} = +25V$	3.6		8.3	mA
		$V_{IN} = -25V$	−3.6		−8.3	mA
		$V_{IN} = +3V$	+0.43		+1.0	mA
		$V_{IN} = -3V$	−0.43		−1.0	mA
V_{OH}	Output High Voltage	$V_{IN} = V_{TL}$(min) $I_{OUT} = -3.2$ mA	2.8			V
V_{OL}	Output Low Voltage	$V_{IN} = V_{TH}$(max) $I_{OUT} = +3.2$ mA			0.4	V
I_{CC}	Supply Current	R_L = open $V_{IN} = V_{TH}$ (max) or V_{TL} (min)			+900	μA

AC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $+4.5V \le V_{CC} \le +5.5V$, GND = 0V, CL = 50 pF, unless otherwise specified (Note 2)

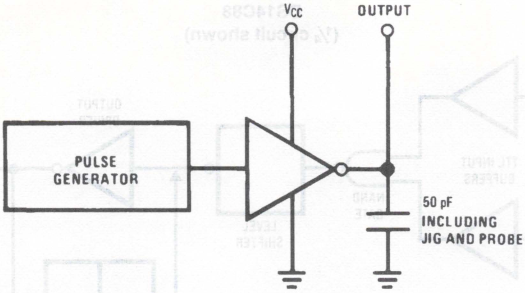
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay to a Logic "1"	Input pulse width ≥ 10 μs			6.5	μs
t_{PHL}	Propagation Delay to a Logic "0"	Input pulse width ≥ 10 μs			6.5	μs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise Time				300	ns
t_f	Output Fall Time				300	ns
t_{nw}	Pulse Width Assumed to be Noise				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = +3V$, $V_{IL} = -3V$, f = 20 kHz.

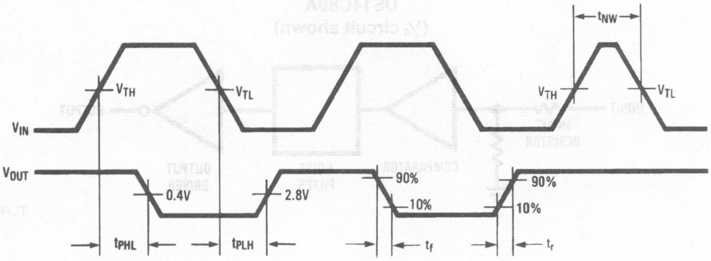
Note 3: For additional details on ESD, contact the local National Semiconductor Sales Office.

DS14C89A AC Test Circuit


VCC
OUTPUT
PULSE GENERATOR
50 pF
INCLUDING
JIG AND PROBE

TL/F/8508–4

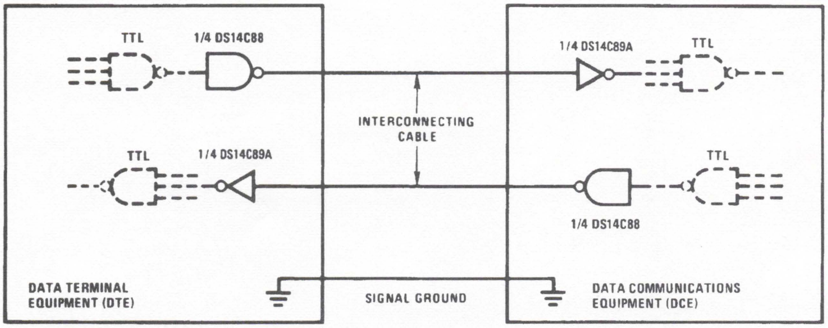
DS14C89A Timing Diagram


tNW
VTH
VTL
VIN
VTH
VTL
VOUT
0.4V
2.8V
90%
10%
90%
10%
tPHL
tPLH
tf
tr

TL/F/8508–5

Typical Applications for DS14C88 and DS14C89A

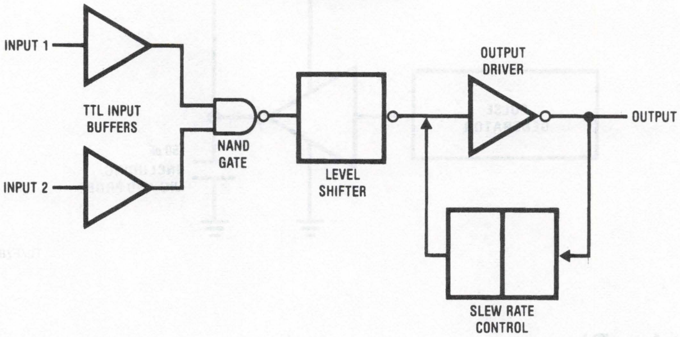
RS232C Data Transmission


TTL
1/4 DS14C88
1/4 DS14C89A
TTL
INTERCONNECTING
CABLE
TTL
1/4 DS14C89A
TTL
1/4 DS14C88
DATA TERMINAL
EQUIPMENT (DTE)
SIGNAL GROUND
DATA COMMUNICATIONS
EQUIPMENT (DCE)

TL/F/8508–3

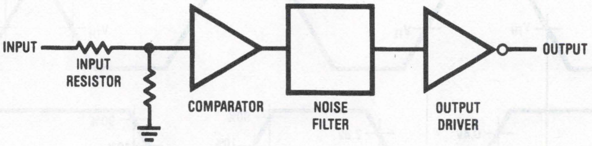
Block Diagrams

DS14C88
(¼ circuit shown)


INPUT 1
TTL INPUT BUFFERS
INPUT 2
NAND GATE
LEVEL SHIFTER
OUTPUT DRIVER
OUTPUT
SLEW RATE CONTROL

TL/F/8508-6

DS14C89A
(¼ circuit shown)


INPUT
INPUT RESISTOR
COMPARATOR
NOISE FILTER
OUTPUT DRIVER
OUTPUT

TL/F/8508-1

National Semiconductor

DS1489/DS1489A Quad Line Receiver

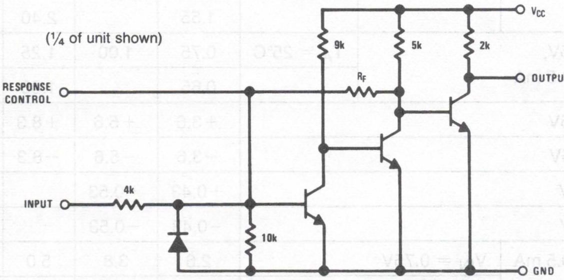
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA Standard RS-232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

Features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

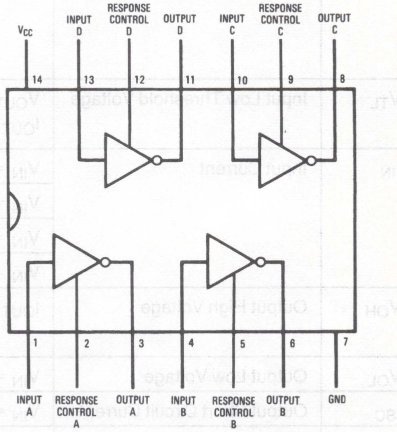
Schematic and Connection Diagrams


(¼ of unit shown)
RESPONSE CONTROL
INPUT
4k
10k
9k
5k
2k
R_F
V_{CC}
OUTPUT
GND

DS1489: R_F = 10k
DS1489A: R_F = 2k

TL/F/5777-1

Dual-In-Line Package

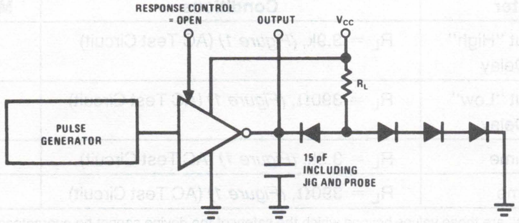

V_{CC}
INPUT D
RESPONSE CONTROL D
OUTPUT D
INPUT C
RESPONSE CONTROL C
OUTPUT C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INPUT A
RESPONSE CONTROL A
OUTPUT A
INPUT B
RESPONSE CONTROL B
OUTPUT B
GND

TL/F/5777-2

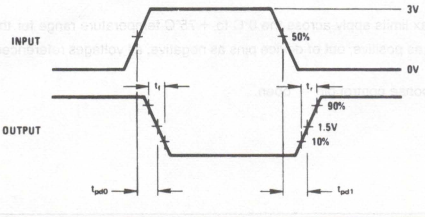
Top View

Order Number DS1489J, DS1489AJ, DS1489M, DS1489AM, DS1489N or DS1489AN
See NS Package Number J14A, M14A or N14A

AC Test Circuit and Voltage Waveforms


RESPONSE CONTROL = OPEN
OUTPUT
V_{CC}
R_L
PULSE GENERATOR
15 pF INCLUDING JIG AND PROBE

TL/F/5777-3


INPUT
3V
50%
0V
t_f
t_r
OUTPUT
90%
1.5V
10%
t_{pd0}
t_{pd1}

TL/F/5777-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded DIP Package	1207 mW
SO Package	1042 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 9.7 mW/°C above 25°C; derate SO package 8.33 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for $V_{CC} = 5.0V \pm 1\%$, $0°C \le T_A \le +75°C$ unless otherwise specified.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage	$V_{OUT} \le 0.45V$, $I_{OUT} = 10$ mA	DS1489	$T_A = 25°C$	1.0	1.25	1.5	V
					0.9		1.6	V
			DS1489A	$T_A = 25°C$	1.75	2.00	2.25	V
					1.55		2.40	V
V_{TL}	Input Low Threshold Voltage	$V_{OUT} \ge 2.5V$, $I_{OUT} = -0.5$ mA		$T_A = 25°C$	0.75	1.00	1.25	V
					0.65		1.35	V
I_{IN}	Input Current	$V_{IN} = +25V$			+3.6	+5.6	+8.3	mA
		$V_{IN} = -25V$			−3.6	−5.6	−8.3	mA
		$V_{IN} = +3V$			+0.43	+0.53		mA
		$V_{IN} = -3V$			−0.43	−0.53		mA
V_{OH}	Output High Voltage	$I_{OUT} = -0.5$ mA	$V_{IN} = 0.75V$		2.6	3.8	5.0	V
			Input = Open		2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA				0.33	0.45	V
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.75V$				−3.0		mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$				14	26	mA
P_d	Power Dissipation	$V_{IN} = 5.0V$				70	130	mW

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Input to Output "High" Propagation Delay	$R_L = 3.9k$, *(Figure 1)* (AC Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	$R_L = 390\Omega$, *(Figure 1)* (AC Test Circuit)		20	50	ns
t_r	Output Rise Time	$R_L = 3.9k$, *(Figure 1)* (AC Test Circuit)		110	175	ns
t_f	Output Fall Time	$R_L = 390\Omega$, *(Figure 1)* (AC Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

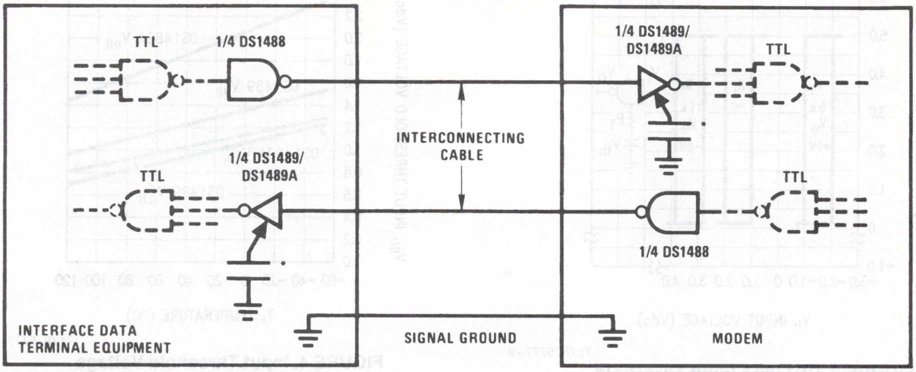
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

Typical Applications

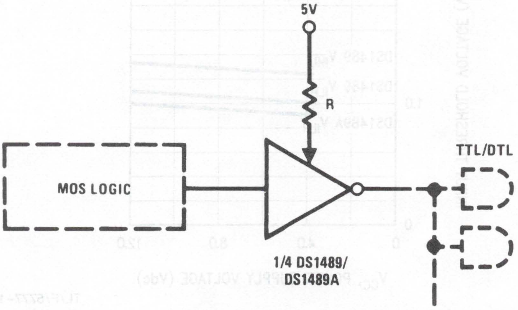
RS-232C Data Transmission


TTL
1/4 DS1488
1/4 DS1489/
DS1489A
TTL
INTERCONNECTING
CABLE
1/4 DS1489/
DS1489A
TTL
TTL
*
*
1/4 DS1488
INTERFACE DATA
TERMINAL EQUIPMENT
SIGNAL GROUND
MODEM

TL/F/5777-5

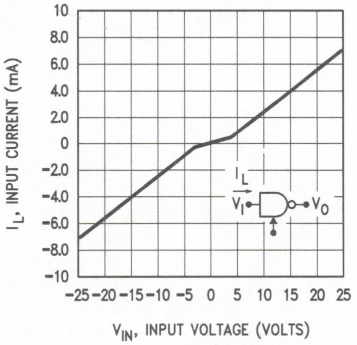
*Optional for noise filtering.

MOS to TTL/LS Translator


5V
R
MOS LOGIC
TTL/DTL
1/4 DS1489/
DS1489A

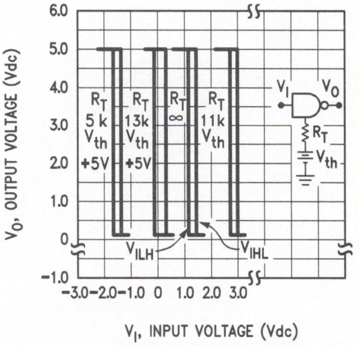
TL/F/5777-6

Typical Characteristics $V_{CC} = 5.0\ V_{DC}$, $T_A = +25°C$ unless otherwise noted



TL/F/5777-7

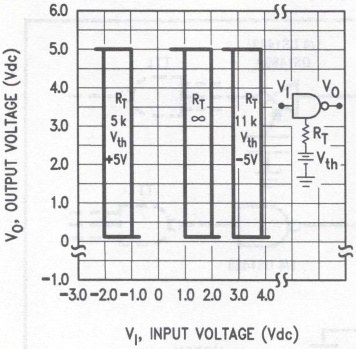
FIGURE 1. Input Current



TL/F/5777-8

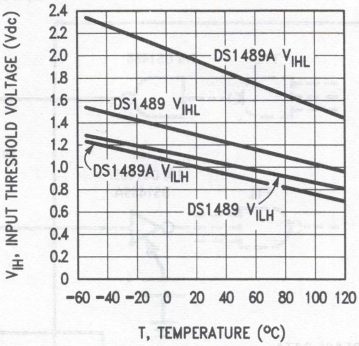
FIGURE 2. DS1489 Input Threshold Voltage Adjustment

Typical Characteristics $V_{CC} = 5.0\ V_{DC}$, $T_A = +25°C$ unless otherwise noted (Continued)



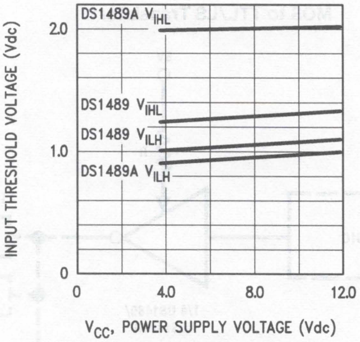
TL/F/5777-9

FIGURE 3. DS1489A Input Threshold Voltage Adjustment



TL/F/5777-10

FIGURE 4. Input Threshold Voltage vs Temperature



TL/F/5777-11

FIGURE 5. Input Threshold vs Power Supply Voltage

National Semiconductor

PRELIMINARY

DS26C31C CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

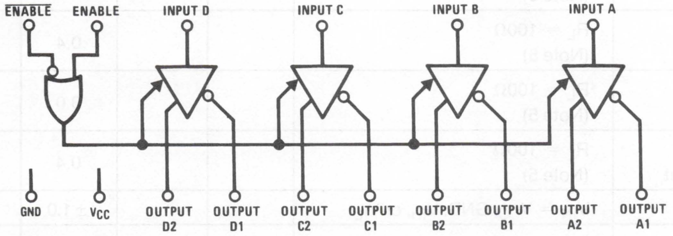
The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The DS26C31 also includes special power up and down circuitry which will TRI-STATE the outputs during power up or down, preventing spurious glitches on its outputs. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

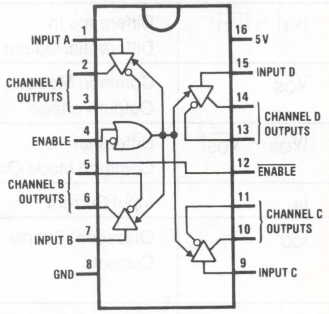
- TTL input compatible
- Typical propagation delays: 8 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

Logic and Connection Diagrams


ENABLE
ENABLE
INPUT D
INPUT C
INPUT B
INPUT A
GND
VCC
OUTPUT D2
OUTPUT D1
OUTPUT C2
OUTPUT C1
OUTPUT B2
OUTPUT B1
OUTPUT A2
OUTPUT A1

TL/F/8574-2

Dual-In-Line Package


INPUT A
1
16
5V
2
15
INPUT D
CHANNEL A OUTPUTS
3
14
CHANNEL D OUTPUTS
13
ENABLE
4
12
ENABLE
5
CHANNEL B OUTPUTS
6
11
CHANNEL C OUTPUTS
10
INPUT B
7
GND
8
9
INPUT C

TL/F/8574-1

Top View

Order Number DS26C31CJ, DS26C31CM or DS26C31CN

See NS Package Number J16A, M16A or N16A

Truth Table

Active High Enable	Active Low Enable	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state

H = High logic state

X = Irrelevant

Z = TRI-STATE (high impedance)

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = -20$ mA	2.5			V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 20$ mA			0.5	V
V_T	Differential Output Voltage	$R_L = 100\Omega$ (Note 5)	2.0			V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference In Differential Output	$R_L = 100\Omega$ (Note 5)			0.4	V
V_{OS}	Common Mode Output Voltage	$R_L = 100\Omega$ (Note 5)			3.0	V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Difference In Common Mode Output	$R_L = 100\Omega$ (Note 5)			0.4	V
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}			±1.0	μA
I_{CC}	Quiescent Supply Current	$I_{OUT} = 0\ \mu$A, $V_{IN} = V_{CC}$ or GND V_{IN} = 2.4V or 0.5V (Note 6)		200 0.8		μA mA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{\text{ENABLE}} = V_{IL}$ $\text{ENABLE} = V_{IH}$		±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Note 7)	−30		−150	mA
I_{OFF}	Output Leakage Current Power Off	V_{CC} = 0V, V_{OUT} = 6V			100	μA
		V_{CC} = 0V, V_{OUT} = −0.25V			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Power Dissipation temperature derating-plastic "N" package: −12 mW/°C from 65°C to 85°C.
ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V \pm 10\%$, $t_r = t_f = 6$ ns (*Figures 1, 2, 3* and *4*) (Note 4)

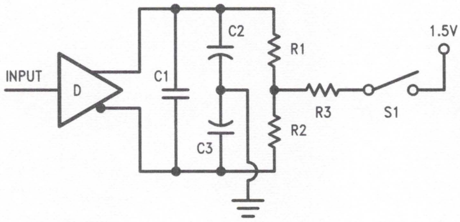
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		8		ns
Skew	(Note 8)	S1 Open		0.5		ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		8		ns
t_{PZH}	Output Enable Time	S1 Closed		18		ns
t_{PZL}	Output Enable Time	S1 Closed		19		ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		9		ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		9		ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			10		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

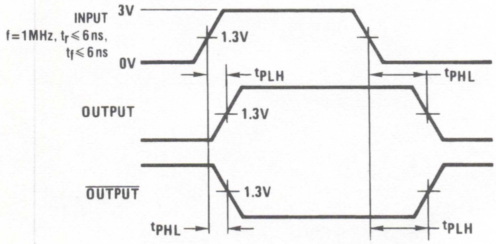
AC Test Circuit and Switching Time Waveforms


INPUT
D
C1
C2
C3
R1
R2
R3
S1
1.5V

TL/F/8574-3

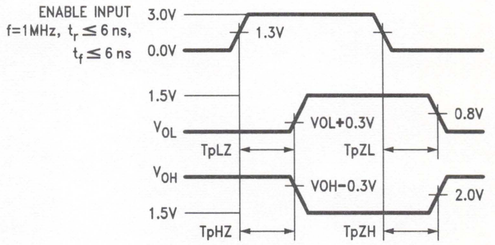
Note: C1 = C2 = C3 = 40 pF, R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit


INPUT
f=1MHz, tr≤6ns,
tf≤6ns
3V
0V
1.3V
tPLH
tPHL
OUTPUT
1.3V
OUTPUT
1.3V
tPHL
tPLH

TL/F/8574-4

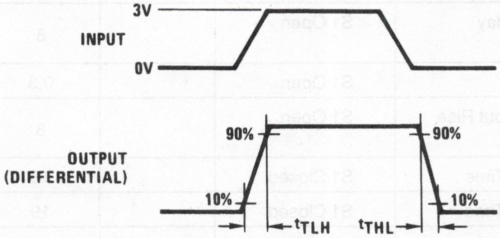
FIGURE 2. Propagation Delays


ENABLE INPUT
f=1MHz, tr≤6 ns,
tf≤6 ns
3.0V
0.0V
1.3V
1.5V
VOL
VOL+0.3V
0.8V
TpLZ
TpZL
VOH
VOH−0.3V
2.0V
1.5V
TpHZ
TpZH

TL/F/8574-5

FIGURE 3. Enable and Disable Times

AC Test Circuit and Switching Time Waveforms (Continued)


3V
INPUT
0V
90%
90%
OUTPUT
(DIFFERENTIAL)
10%
10%
t_{TLH}
t_{THL}

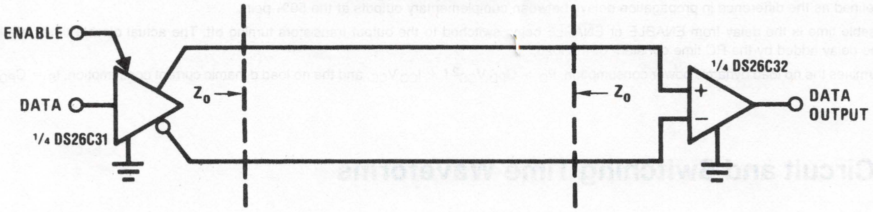
Input pulse; f = 1MHz, 50%; $t_r = t_f \leq 6$ns.

TL/F/8574-7

FIGURE 4. Differential Rise and Fall Times

Typical Applications

Two-Wire Balanced System, RS-422


ENABLE
DATA
1/4 DS26C31
Z_0
Z_0
1/4 DS26C32
+
−
DATA
OUTPUT

TL/F/8574-8

National Semiconductor

DS26F31C/DS26F31M Quad High Speed Differential Line Driver

General Description

The DS26F31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26F31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The DS26F31 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F31 features lower power, extended temperature range, and improved specifications.

The circuit provides an enable and disable function common to all four drivers. The DS26F31C/DS26F31M features TRI-STATE® outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

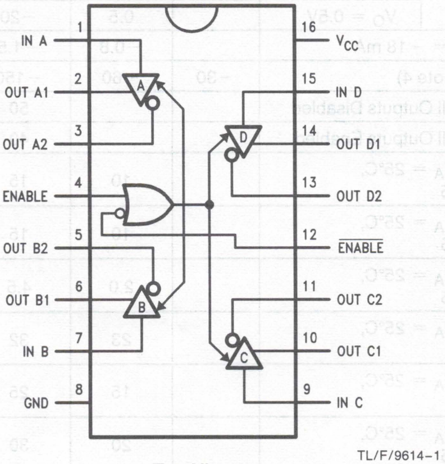
The DS26F31C/DS26F31M offers optimum performance when used with the DS26F32 Quad Differential Line Receiver.

Features

- Low power version
- Output skew—2.0 ns typical
- Input to output delay—12 ns
- Operation from single +5.0V supply
- 16-lead ceramic and molded DIP Package
- Outputs won't load line when V_{CC} = 0V
- Four line drivers in one package for maximum package density
- Output short circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Extended temperature range

Connection and Logic Diagrams

16-Lead Dual-In-Line Package and SO-16 Package



Top View

Order Number DS26F31CJ or DS26F31MJ
See NS Package Number J16A*

Order Number DS26F31CN
See NS Package Number N16A

Order Number DS26F31CM
See NS Package Number M16A

*For most current package information contact product marketing.

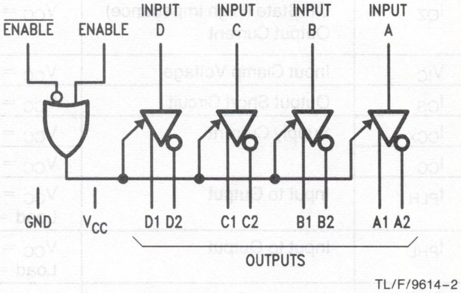


FIGURE 1. Logic Symbol

Function Table (Each Driver)

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO Package	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-16 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW
Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Operating Range

DS26F31C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F31M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = −20 mA		2.5	3.2		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = 20 mA			0.32	0.5	V
V_{IH}	Input Voltage HIGH	V_{CC} = Min		2.0			V
V_{IL}	Input Voltage LOW	V_{CC} = Max				0.8	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4V			−0.10	−0.20	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7V			0.5	20	μA
I_{IR}	Input Reverse Current	V_{CC} = Max, V_I = 7.0V			0.001	0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
I_{OS}	Output Short Circuit	V_{CC} = Max (Note 4)		−30	−60	−150	mA
I_{CCX}	Supply Current	V_{CC} = Max, All Outputs Disabled				50	mA
I_{CC}		V_{CC} = Max, All Outputs Enabled				40	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			10	15	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			10	15	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			2.0	4.5	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			23	32	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			15	25	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			20	30	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			23	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

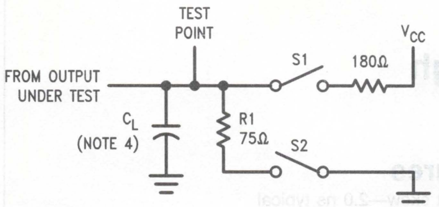
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F31M and across the 0°C to +70°C range for the DS26F31C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

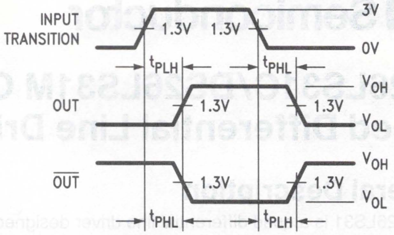
Note 5: C_L = 30 pF, V_I = 1.3V to V_O = 1.3V, V_{PULSE} = 0V to +3V (See AC Load Test Circuit for TRI-STATE Outputs).

Test Circuit and Timing Waveforms


TEST POINT
V_{CC}
FROM OUTPUT UNDER TEST
S1
180Ω
C_L (NOTE 4)
R1 75Ω
S2

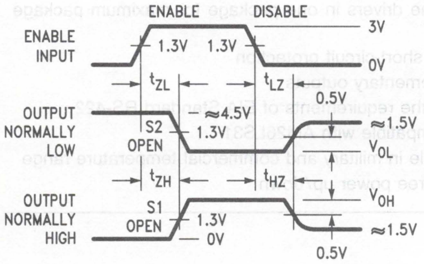
TL/F/9614-3

FIGURE 2. AC Load Test Circuit for TRI-STATE Outputs


INPUT TRANSITION
3V
1.3V
1.3V
0V
t_{PLH}
t_{PHL}
OUT
V_{OH}
1.3V
1.3V
V_{OL}
$\overline{OUT}$
V_{OH}
1.3V
1.3V
V_{OL}
t_{PHL}
t_{PLH}

TL/F/9614-4

FIGURE 3. Propagation Delay (Notes 1 and 3)


ENABLE
DISABLE
ENABLE INPUT
3V
1.3V
1.3V
0V
t_{ZL}
t_{LZ}
0.5V
OUTPUT NORMALLY LOW
≈4.5V
S2 OPEN
1.3V
≈1.5V
V_{OL}
t_{ZH}
t_{HZ}
V_{OH}
OUTPUT NORMALLY HIGH
S1 OPEN
1.3V
0V
≈1.5V
0.5V

TL/F/9614-5

FIGURE 4. Enable and Disable Times (Notes 2 and 3)

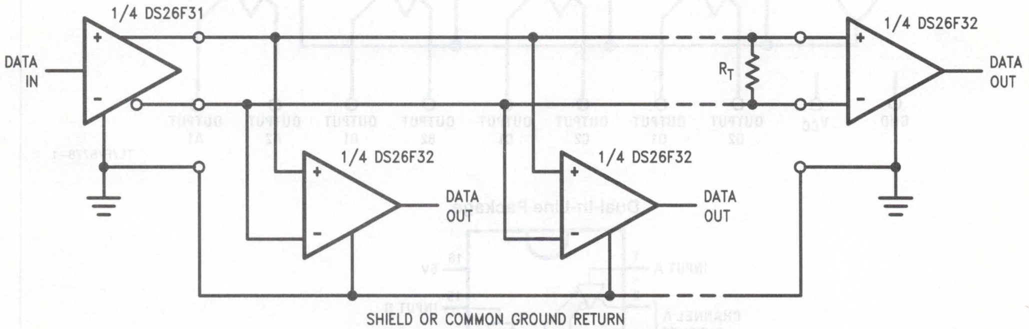
Note 1: Diagram shown for Enable Low. Switches S1 and S2 open.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, Z_O = 50Ω, t_r ≤ 6.0 ns, t_f ≤ 6.0 ns.

Note 4: C_L includes probe and jig capacitance.

Typical Application


1/4 DS26F31
DATA IN
+
-
1/4 DS26F32
DATA OUT
R_T
1/4 DS26F32
DATA OUT
1/4 DS26F32
DATA OUT
SHIELD OR COMMON GROUND RETURN

TL/F/9614-6

FIGURE 5. Typical Application

National Semiconductor

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

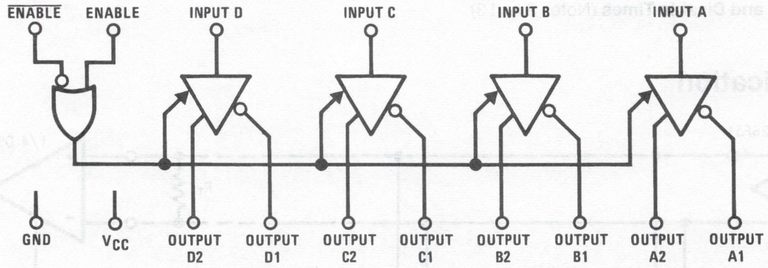
The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which keeps the output in a high impedance state (TRI-STATE) during power up or down preventing erroneous glitches on the transmission lines.

Features

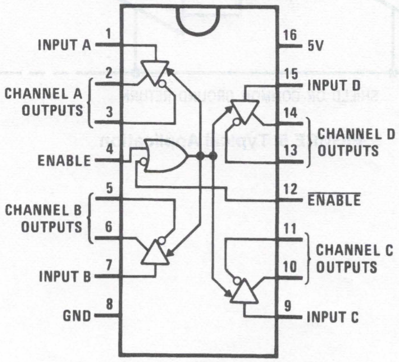
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0V$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range
- Glitch free power up/down

Logic and Connection Diagrams


ENABLE
ENABLE
INPUT D
INPUT C
INPUT B
INPUT A
GND
VCC
OUTPUT D2
OUTPUT D1
OUTPUT C2
OUTPUT C1
OUTPUT B2
OUTPUT B1
OUTPUT A2
OUTPUT A1

TL/F/5778-1

Dual-In-Line Package


INPUT A
1
2
CHANNEL A OUTPUTS
3
ENABLE
4
5
CHANNEL B OUTPUTS
6
INPUT B
7
GND
8
16
5V
15
INPUT D
14
CHANNEL D OUTPUTS
13
12
ENABLE
11
CHANNEL C OUTPUTS
10
9
INPUT C

TL/F/5778-2

Top View

Order Number DS26LS31CJ, DS26LS31CM, DS26LS31CN or DS26LS31MJ

See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	−0.25 to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -20$ mA	2.5			V
V_{OL}	Output Low Voltage	$I_{OL} = 20$ mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	$V_{IN} = 0.4V$		−40	−200	μA
I_{IH}	Input High Current	$V_{IN} = 2.7V$			20	μA
I_I	Input Reverse Current	$V_{IN} = 7V$			0.1	mA
I_O	TRI-STATE Output Current	$V_O = 2.5V$			20	μA
		$V_O = 0.5V$			−20	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -18$ mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	$C_L = 30$ pF		10	15	ns
t_{PHL}	Input to Output	$C_L = 30$ pF		10	15	ns
Skew	Output to Output	$C_L = 30$ pF		2.0	6.0	ns
t_{LZ}	Enable to Output	$C_L = 10$ pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	$C_L = 10$ pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	$C_L = 30$ pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	$C_L = 30$ pF, S1 Open		20	30	ns

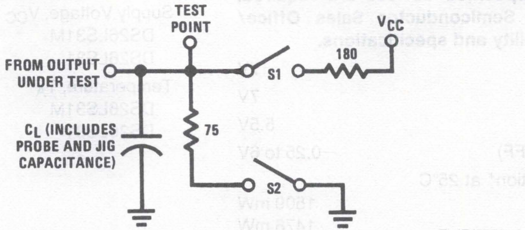
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS726LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

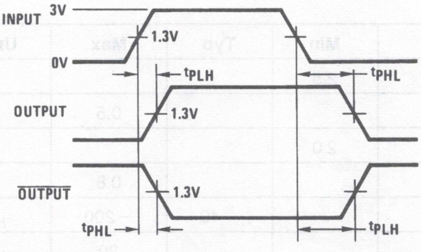
Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms


TEST POINT
VCC
FROM OUTPUT UNDER TEST
S1
180
CL (INCLUDES PROBE AND JIG CAPACITANCE)
75
S2
TL/F/5778-3

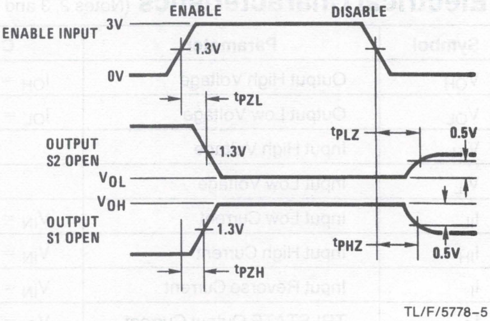
Note: S1 and S2 of load circuit are closed except where shown.

FIGURE 1. AC Test Circuit


INPUT
3V
0V
1.3V
tPLH
tPHL
OUTPUT
1.3V
OUTPUT
1.3V
tPHL
tPLH
TL/F/5778-4

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 2. Propagation Delays

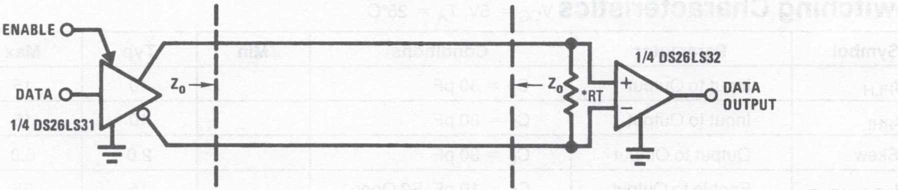

ENABLE
DISABLE
ENABLE INPUT
3V
0V
1.3V
tPZL
tPLZ
0.5V
OUTPUT S2 OPEN
1.3V
VOL
VOH
OUTPUT S1 OPEN
1.3V
tPHZ
0.5V
tPZH
TL/F/5778-5

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422


ENABLE
DATA
1/4 DS26LS31
Zo
Zo
*RT
1/4 DS26LS32
DATA OUTPUT
TL/F/5778-6

*R_T is optional although highly recommended to reduce reflection.

National Semiconductor

PRELIMINARY

DS26C32C Quad Differential Line Receiver

General Description

The DS26C32 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

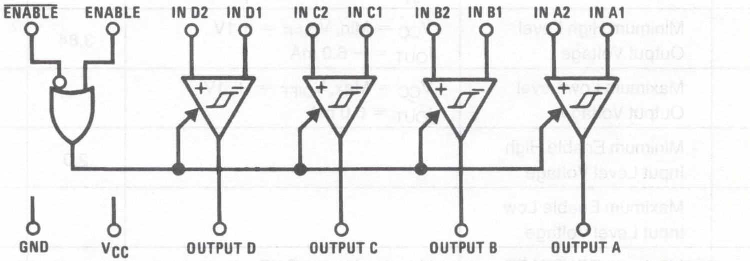
The DS26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Each receiver is also equipped with input fail-safe circuitry, which causes the output to go to a logic "1" state when the inputs are open.

The DS26C32 provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Input fail-safe circuitry
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

Logic Diagram

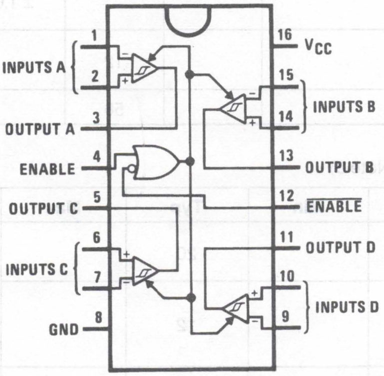


ENABLE
$\overline{\text{ENABLE}}$
IN D2
IN D1
IN C2
IN C1
IN B2
IN B1
IN A2
IN A1
GND
V_{CC}
OUTPUT D
OUTPUT C
OUTPUT B
OUTPUT A

TL/F/8764–1

Connection Diagram

Dual-In-Line Package



1
2
INPUTS A
3
OUTPUT A
4
ENABLE
5
OUTPUT C
6
7
INPUTS C
8
GND
16
V_{CC}
15
14
INPUTS B
13
OUTPUT B
12
$\overline{\text{ENABLE}}$
11
OUTPUT D
10
9
INPUTS D

TL/F/8764–2

Top View

Order Number DS26C32CJ, DS26C32CM, DS26C32CN, DS26C32MJ or DS26C32MN
See NS Package J16A, M16A or N16A

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1

Hi-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Current Per Output	±25 mA

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−0.2		+0.2	V
R_{IN}	Input Resistance	$-7V < V_{CM} < +7V$ (One Input AC GND)		10		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND		−1.1		mA
		$V_{IN} = -10V$, Other Input = GND		+1.6		mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, $V_{DIFF} = +1V$ $I_{OUT} = 6.0$ mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{ENABLE} = V_{IL}$, $ENABLE = V_{IH}$		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, $V_{DIFF} = +1V$		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	$C_L = 50$ pF $V_{DIFF} = 2.5V$		20		ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		12		ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		14		ns

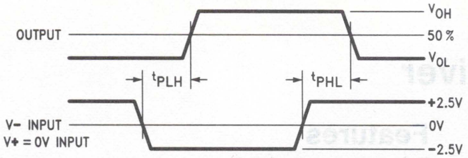
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the −40°C to +85°C temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Test and Switching Waveforms

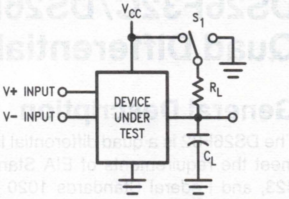
Propagation Delay



OUTPUT
V_{OH}
50 %
V_{OL}
t_{PLH}
t_{PHL}
V− INPUT
V+ = 0V INPUT
+2.5V
0V
−2.5V

TL/F/8764-3

Test Circuit for TRI-STATE Output Tests



V_{CC}
S_1
R_L
V+ INPUT
V− INPUT
DEVICE UNDER TEST
C_L

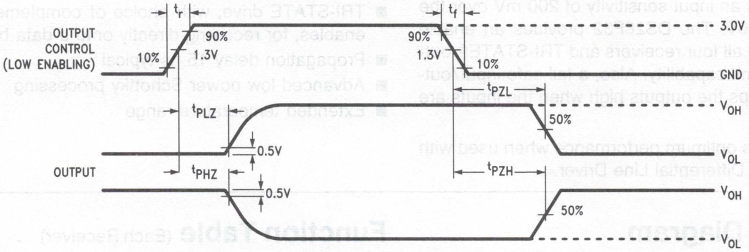
TL/F/8764-4

C_L includes load and test jig capacitance.

S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S1 = Gnd for t_{PZH} and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms



t_r
t_f
OUTPUT CONTROL (LOW ENABLING)
10%
90%
1.3V
90%
1.3V
10%
3.0V
GND
t_{PLZ}
t_{PZL}
V_{OH}
50%
0.5V
V_{OL}
OUTPUT
t_{PHZ}
t_{PZH}
0.5V
V_{OH}
50%
V_{OL}

TL/F/8764-5

National Semiconductor

DS26F32C/DS26F32M
Quad Differential Line Receiver

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE® outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

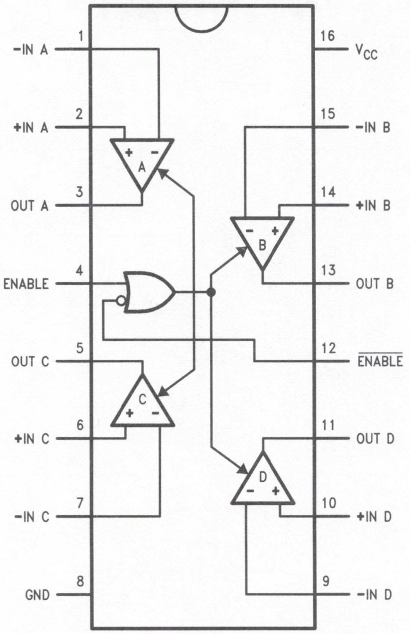
The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Features

- Low power version
- Input voltage range of ±7.0V (differential or common mode) ±0.2V sensitivity over the input voltage range
- Meets all the requirements of EIA standards RS-422 and RS-423
- Input impedance (18k typical)
- 30 mV input hysteresis
- Operation from single +5.0V supply
- Fail-safe input/output relationship. Output always high when inputs are open
- TRI-STATE drive, with choice of complementary output enables, for receiving directly onto a data bus
- Propagation delay 15 ns typical
- Advanced low power Schottky processing
- Extended temperature range

Connection Diagram

16-Lead DIP and SO-16 Package



TL/F/9615–1

Top View

Function Table (Each Receiver)

Differential Inputs	Enables		Outputs
A−B	E	Ē	V
$V_{ID} \geq 0.2V$	H X	X L	H H
$V_{ID} \leq -0.2V$	H X	X L	L L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial

Order Number DS26F32CJ or DS26F32MJ
See NS Package Number* J16A

Order Number DS26F32CM
See NS Package Number M16A

Order Number DS26F32CN
See NS Package Number N16A

*For most current package information contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to + 175°C
Molded DIP and SO-16	−65°C to + 150°C
Operating Temperature Range	
DS26F32M	−55°C to +125°C
DS26F32C	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec)	300°C
Molded DIP and SO-16 (soldering, 10 sec)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Supply Voltage	7.0V
Common Mode Voltage Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50 mA

Operating Range

DS26F32C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F32M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics Over operating range, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$-7.0V \leq V_{CM} \leq +7.0V$, $V_O = V_{OL}$ or V_{OH}		−0.2	±0.06	+0.2	V
R_I	Input Resistance	$-15V \leq V_{CM} \leq +15V$, One Input AC Ground		14	18		kΩ
I_I	Input Current (under Test)	$V_I = +15V$, Other Input $-15V \leq V_I \leq +15V$				2.3	mA
		$V_I = -15V$, Other Input $-15V \leq V_I \leq +15V$				−2.8	
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $\Delta V_I = +1.0V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	0°C to +70°C	2.8	3.4		V
			−55°C to +125°C	2.5	3.4		
V_{OL}	Output Voltage LOW	V_{CC} = Min, $\Delta V_I = -1.0V$, $V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 4.0\ mA$			0.4	V
			$I_{OL} = 8.0\ mA$			0.45	
V_{IL}	Enable Voltage LOW					0.8	V
V_{IH}	Enable Voltage HIGH			2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min, $I_I = -18\ mA$				−1.5	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	
I_{IL}	Enable Current LOW	$V_I = 0.4V$			−0.2	−0.36	mA
I_{IH}	Enable Current HIGH	$V_I = 2.7V$			0.5	10	μA
I_I	Enable Input High Current	$V_I = 5.5V$			1.0	50	μA
I_{OS}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max, (Note 4) $\Delta V_I = +1.0V$		−15	−50	−85	mA
I_{CC}	Supply Current	V_{CC} = Max, All V_I = GND, Outputs Disabled			30	50	mA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

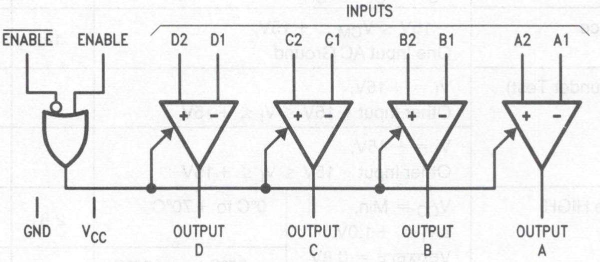
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F32M and across the 0°C to +70°C range for the DS26F32C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

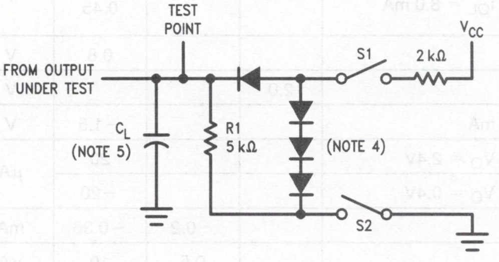
Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		15	22	ns
t_{PHL}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		15	22	ns
t_{LZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		14	18	ns
t_{HZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		15	20	ns
t_{ZL}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		13	18	ns
t_{ZH}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15 pF, See Test Circuit *(Figure 2)*		12	16	ns


INPUTS
ENABLE
ENABLE
D2
D1
C2
C1
B2
B1
A2
A1
+
−
GND
V_{CC}
OUTPUT D
OUTPUT C
OUTPUT B
OUTPUT A

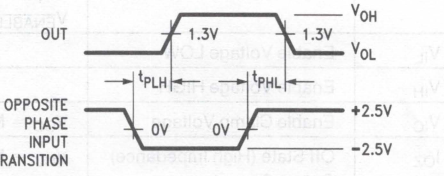
TL/F/9615-2

FIGURE 1. Logic Symbol


TEST POINT
V_{CC}
FROM OUTPUT UNDER TEST
S1
2 kΩ
C_L (NOTE 5)
R1 5 kΩ
(NOTE 4)
S2

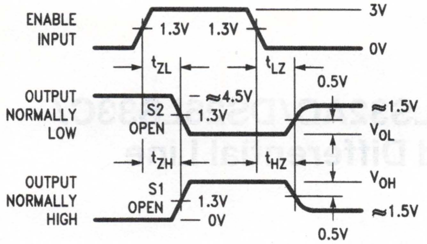
TL/F/9615-3

FIGURE 2. Load Test Circuit for Three-State Outputs


OUT
1.3V
1.3V
V_{OH}
V_{OL}
t_{PLH}
t_{PHL}
OPPOSITE PHASE INPUT TRANSITION
+2.5V
0V
0V
−2.5V

TL/F/9615-4

FIGURE 3. Propagation Delay (Notes 1, 2 and 3)


ENABLE INPUT
1.3V
1.3V
3V
0V
t_{ZL}
t_{LZ}
0.5V
OUTPUT NORMALLY LOW
≈4.5V
S2 OPEN
1.3V
≈1.5V
V_{OL}
t_{ZH}
t_{HZ}
V_{OH}
OUTPUT NORMALLY HIGH
S1 OPEN
1.3V
0V
≈1.5V
0.5V

TL/F/9615-5

FIGURE 4. Enable and Disable Times (Notes 1, 2 and 3)

Note 1: Diagram shown for ENABLE Low.

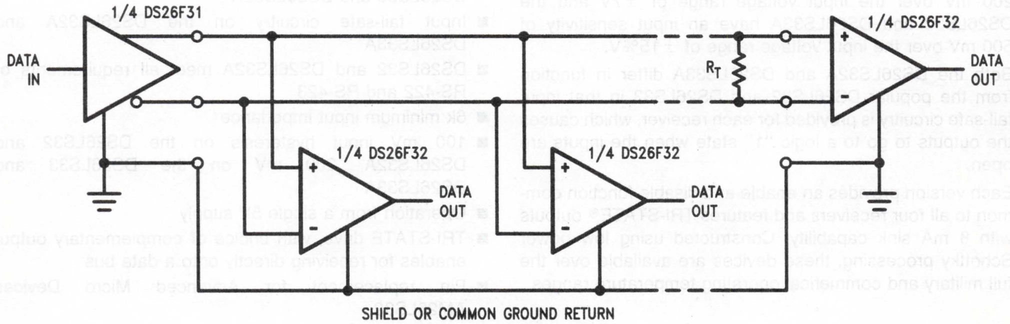
Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.

Note 4: All diodes are IN916 or IN3064.

Note 5: C_L includes probe and jig capacitance.

Typical Application


1/4 DS26F31
DATA IN
1/4 DS26F32
R_T
DATA OUT
1/4 DS26F32
DATA OUT
1/4 DS26F32
DATA OUT
SHIELD OR COMMON GROUND RETURN

TL/F/9615-6

FIGURE 5

National Semiconductor

DS26LS32C/DS26LS32M/DS26LS32AC/DS26LS33C/DS26LS33M/DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ±15%V.

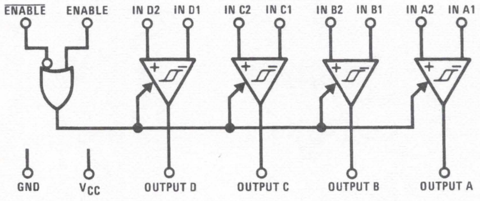
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input fail-safe circuitry is provided for each receiver, which causes the outputs to go to a logic "1" state when the inputs are open.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33 and DS26LS33A
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33 and DS26LS33A
- Input fail-safe circuitry on the DS26LS32A and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus
- Pin replacement for Advanced Micro Devices AM26LS32

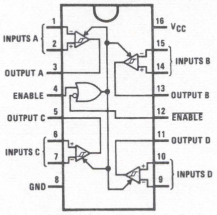
Logic Diagram



TL/F/5255–1

Connection Diagram

Dual-In-Line Package



TL/F/5255–2

Top View

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
1	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1*

HI-Z = TRI-STATE

*DS26LS32A and DS26LS33A only

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32MJ, DS26LS32CJ, DS26LS32CM, DS26LS32CN, DS26LS32ACJ, DS26LS32ACN, DS26LS32ACM, DS26LS33MJ, DS26LS33CJ, DS26LS33CN, DS26LS33ACJ or DS26LS33ACN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1362 mW
SO Package DS26LS32	1002 mW
DS26LS232A	1051 mW
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C.

Derate SO Package 8.01 mW/°C for DS26LS32
8.41 mW/°C for DS26LS32A

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	4.75	5.25	V
Temperature, (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	0	+70	°C

Electrical Characteristics over the operating temperature range unless otherwise specified (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, $-7V \le V_{CM} \le +7V$	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, $-15V \le V_{CM} +15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = 15V$, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
		$V_{IN} = -15V$, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = MIN, $\Delta V_{IN} = 1V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, $\Delta V_{IN} = -1V$, $V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 4$ mA			0.4	V
			$I_{OL} = 8$ mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18$ mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	μA
I_{IL}	Enable Low Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable High Current	$V_{IN} = 2.7V$				20	μA
I_{SC}	Output Short-Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = 1V$		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled	DS26LS32, DS26LS32A		52	70	mA
			DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	$V_{IN} = 5.5V$				100	μA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5V$, $V_{CM} = 0V$	DS26LS32, DS26S32A		100		mV
			DS26LS33, DS26LS33A		200		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, all currents out of device pins are shown as negative, all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

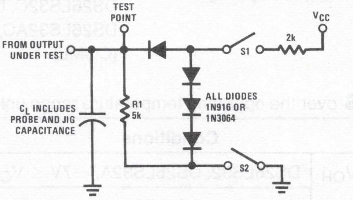
Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	$C_L = 15$ pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	$C_L = 5$ pF		20	30		15	22	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	$C_L = 15$ pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

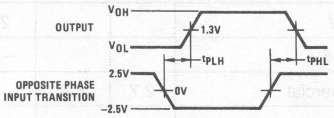
AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE Outputs


TEST POINT
VCC
FROM OUTPUT UNDER TEST
S1
2k
CL INCLUDES PROBE AND JIG CAPACITANCE
R1 5k
ALL DIODES 1N916 OR 1N3064
S2

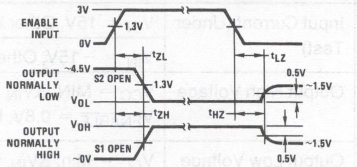
TL/F/5255-3

Propagation Delay (Notes 1 and 3)


VOH
OUTPUT
VOL
1.3V
tPLH
tPHL
2.5V
OPPOSITE PHASE INPUT TRANSITION
0V
−2.5V

TL/F/5255-4

Enable and Disable Times (Notes 2 and 3)


3V
ENABLE INPUT
1.3V
0V
tZL
tLZ
≈4.5V
S2 OPEN
OUTPUT NORMALLY LOW
1.3V
VOL
0.5V
~1.5V
tZH
tHZ
VOH
OUTPUT NORMALLY HIGH
S1 OPEN
0V
0.5V
~1.5V

TL/F/5255-5

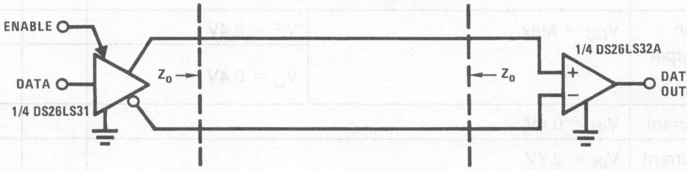
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

Note 3: Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \le 15$ ns; $t_f \le 6.0$ ns.

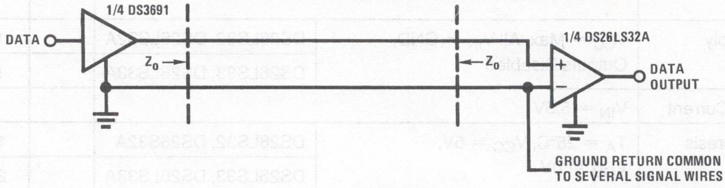
Typical Applications

Two-Wire Balanced Systems, RS-422


ENABLE
DATA
1/4 DS26LS31
Zo
Zo
1/4 DS26LS32A
DATA OUTPUT

TL/F/5255-6

Single Wire with Common Ground Unbalanced Systems, RS-423


1/4 DS3691
DATA
Zo
Zo
1/4 DS26LS32A
DATA OUTPUT
GROUND RETURN COMMON TO SEVERAL SIGNAL WIRES

TL/F/5255-7

National Semiconductor

PRELIMINARY

DS34C86 Quad CMOS Differential Line Receiver

General Description

The DS34C86 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

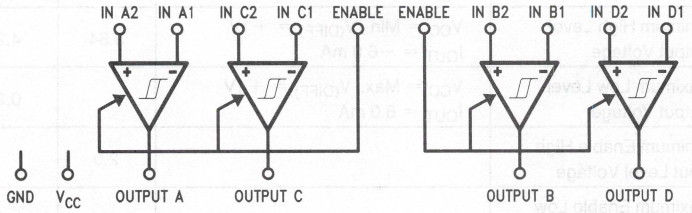
The DS34C86 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86 is pin compatible with the DS3486.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

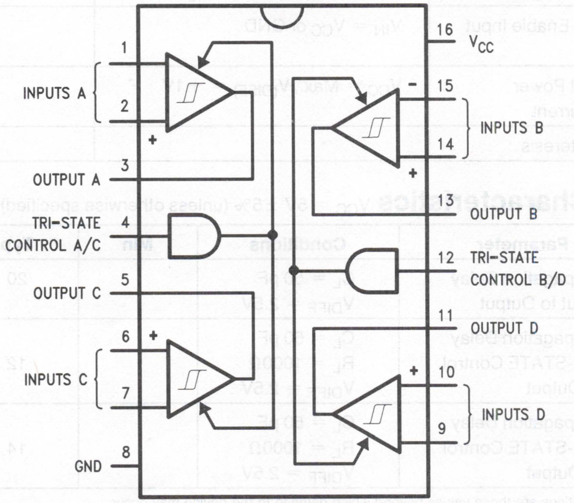
Logic Diagram


IN A2
IN A1
IN C2
IN C1
ENABLE
ENABLE
IN B2
IN B1
IN D2
IN D1
+
−
GND
V_{CC}
OUTPUT A
OUTPUT C
OUTPUT B
OUTPUT D

TL/F/8699–1

Connection Diagram

Dual-In-Line Package


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
INPUTS A
OUTPUT A
TRI-STATE CONTROL A/C
OUTPUT C
INPUTS C
GND
V_{CC}
INPUTS B
OUTPUT B
TRI-STATE CONTROL B/D
OUTPUT D
INPUTS D
+
−

TL/F/8699–2

Top View

Order Number DS34C86J, DS34C86M, and DS34C86N
See NS Package Number J16A, M16A and N16A

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	260°C
Current Per Output	±25 mA

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−0.2		+0.2	V
R_{IN}	Input Resistance	$-7V < V_{CM} < +7V$ (One Input AC GND)		10		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		+1.1 −1.6		mA mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)} = +1V$ $I_{OUT} = 6.0$ mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)} = +1V$		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

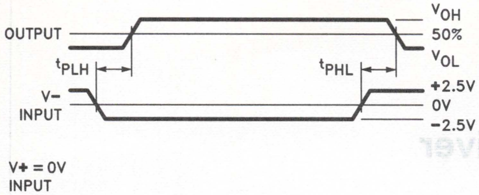
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	$C_L = 50$ pF $V_{DIFF} = 2.5V$		20		ns
t_{PLZ}, t_{PHZ}	Propagation Delay TRI-STATE Control to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		12		ns
t_{PZL}, t_{PZH}	Propagation Delay TRI-STATE Control to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		14		ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

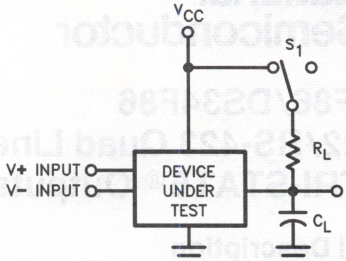
Note 3: Unless otherwise specified, Min/Max limits apply across the −40°C to +85°C temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Propagation Delay


OUTPUT
V-
INPUT
V+ = 0V
INPUT
t_{PLH}
t_{PHL}
V_{OH}
50%
V_{OL}
+2.5V
0V
−2.5V

TL/F/8699-3

Test Circuit for TRI-STATE Output Tests


V_{CC}
S_1
R_L
V+ INPUT
V− INPUT
DEVICE UNDER TEST
C_L

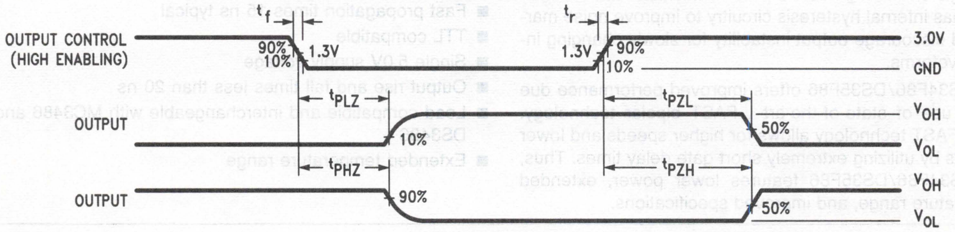
TL/F/8699-4

C_L Includes load and test jig capacitance.

S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S1 = GND for t_{PZH}, and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms


OUTPUT CONTROL
(HIGH ENABLING)
OUTPUT
OUTPUT
t_f
t_r
90%
10%
1.3V
1.3V
90%
10%
3.0V
GND
t_{PLZ}
t_{PZL}
10%
50%
V_{OH}
V_{OL}
t_{PHZ}
t_{PZH}
90%
50%
V_{OH}
V_{OL}

TL/F/8699-5

National Semiconductor

DS35F86/DS34F86 RS-422/RS-423 Quad Line Receiver with TRI-STATE® Outputs

General Description

The DS34F86/DS35F86 RS-422/3 Quad Receiver features four independent receivers, which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. A PNP device buffers each output control lead to assure minimum loading for either logic one or logic zero inputs. In addition each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34F86/DS35F86 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F86/DS35F86 features lower power, extended temperature range, and improved specifications.

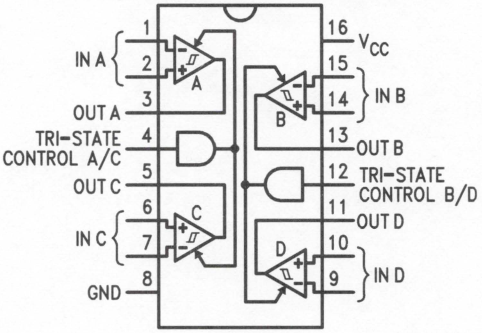
The DS34F86/DS35F86 offers optimum performance when used with the DS34F87/DS35F87 Quad Line Driver.

Features

- Low power version
- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs
- Fast propagation times 15 ns typical
- TTL compatible
- Single 5.0V supply voltage
- Output rise and fall times less than 20 ns
- Lead compatible and interchangeable with MC3486 and DS3486
- Extended temperature range

Connection Diagram

16-Lead DIP and SO-16 Package


1
2
IN A
A
3
OUT A
TRI-STATE CONTROL A/C
4
5
OUT C
6
C
IN C
7
8
GND
16
VCC
15
B
14
IN B
13
OUT B
12
TRI-STATE CONTROL B/D
11
OUT D
10
D
9
IN D

TL/F/9616-1

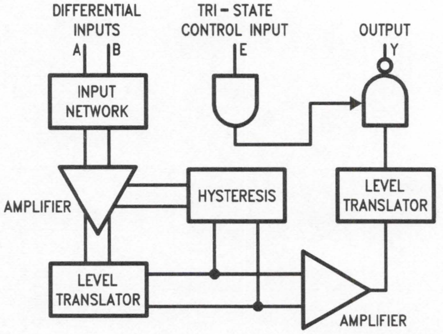
Top View

Order Number DS34F86J or DS35F86J
See NS Package Number J16A*

Order Number DS34F86M
See NS Package Number M16A

Order Number DS34F86N
See NS Package Number N16A

*For most current package information contact product marketing.


DIFFERENTIAL INPUTS
A
B
TRI-STATE CONTROL INPUT
E
OUTPUT
Y
INPUT NETWORK
AMPLIFIER
HYSTERESIS
LEVEL TRANSLATOR
LEVEL TRANSLATOR
AMPLIFIER

TL/F/9616-2

FIGURE 1. Block Diagram

Function Table (Each Receiver)

Differential Inputs AB	Enable E	Output Y
$V_{ID} \leq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-16	−65°C to +150°C
Operating Temperature Range	
DS35F86	−55°C to +125°C
DS34F86	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 seconds)	300°C
Molded DIP and SO-16 (soldering, 10 seconds)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW
Supply Voltage	8.0V
Input Voltage	8.0V
Input Common Mode Voltage	±15V
Input Differential Voltage	±25V

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Operating Conditions

DS34F86	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS35F86	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V
Input Common Mode Voltage Range	−7.0V to +7.0V
Input Differential Voltage Range	6V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2			V
V_{IL}	Input Voltage LOW					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage (Note 6)	$-7V \leq V_{IC} \leq 7V$, $V_{IH} = 2V$	$V_O = V_{OH}$			0.2	V
			$V_O = V_{OL}$	−0.2			
I_{IB}	Input Bias Current	$V_{CC} = 0V$ or 5.25V, Other inputs at 0V	$V_I = -10V$			−3.25	mA
			$V_I = -3V$			−1.50	
			$V_I = +3V$			+1.50	
			$V_I = +10V$			+3.25	
V_{OH}	Output Voltage HIGH (Note 5)	$-7V \leq V_{CM} \leq 7V$ $V_{IH} = 2V$, $I_O = -0.4$ mA, $V_{ID} = 0.4V$	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$-7V \leq V_{CM} \leq 7V$, $V_{IH} = 2V$	$I_O = 8$ mA, $V_{ID} = 0.4V$			0.5	V
I_{OZ}	Off State (High Impedance) Output Current	$V_{I(D)} = +3V$, $V_{IL} = 0.8V$, $V_O = 0.5V$				−10	μA
		$V_{I(D)} = -3V$, $V_{IL} = 0.8V$, $V_O = 2.7V$				10	
I_{OS}	Output Short Circuit Current (Note 4)	$V_{I(D)} = +3V$, $V_{IH} = 2V$, $V_O = 0V$		−15		−100	mA
I_{IL}	Input Current LOW (TRI-STATE Control)	$V_{IL} = 0.5V$				−100	μA
I_{IH}	Input Current HIGH (TRI-STATE Control)		$V_{IH} = 2.7V$			20	μA
			$V_{IH} = 5.25V$			40	
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IC} = -10$ mA				−1.5	V
I_{CC}	Supply Current	$V_{IL} = 0V$				50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F86 and across the 0°C to +70°C range for the DS34F86. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA RS-422/3 for exact conditions. Input balance and V_{OH}/V_{OL} levels are tested simultaneously for worse case.

Note 6: Differential input threshold voltage and guaranteed output levels are tested simultaneously for worse case.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (Figures 2 & 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$t_{PHL(D)}$	Propagation Delay Time Differential Inputs to Outputs	Output HIGH to LOW		15	22	ns
$t_{PLH(D)}$		Output LOW to HIGH		15	22	ns
t_{LZ}	Propagation Delay Time Controls to Outputs	Output LOW to TRI-STATE		14	18	ns
t_{HZ}		Output HIGH to TRI-STATE		15	20	ns
t_{ZH}		Output TRI-STATE to HIGH		12	16	ns
t_{ZL}		Output TRI-STATE to LOW		13	18	ns

Parameter Measurement Information

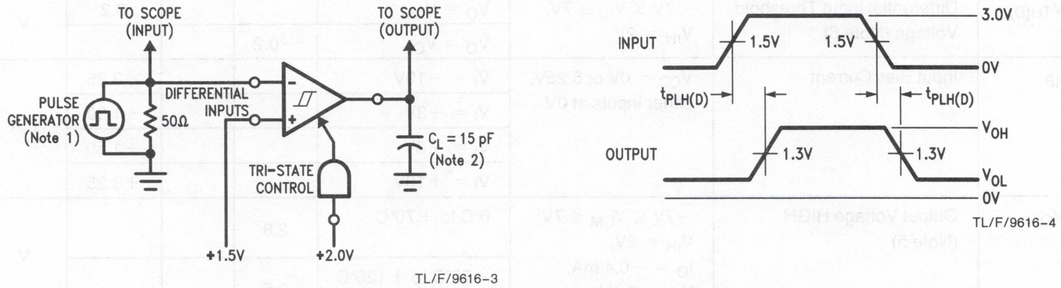
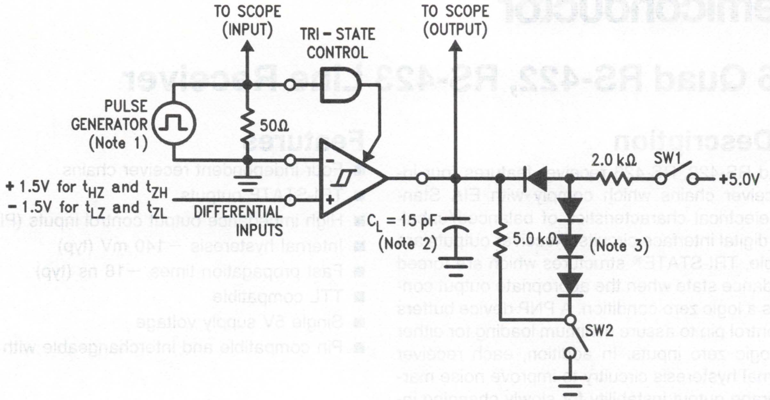

TO SCOPE (INPUT)
PULSE GENERATOR (Note 1)
50Ω
DIFFERENTIAL INPUTS
TO SCOPE (OUTPUT)
TRI-STATE CONTROL
$C_L = 15$ pF (Note 2)
+1.5V
+2.0V
TL/F/9616-3
INPUT
3.0V
1.5V
1.5V
0V
$t_{PLH(D)}$
$t_{PLH(D)}$
OUTPUT
1.3V
1.3V
V_{OH}
V_{OL}
0V
TL/F/9616-4

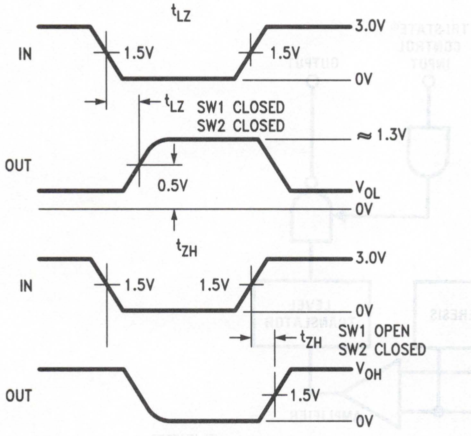
FIGURE 2. Propagation Delay Differential Input to Output

Parameter Measurement Information (Continued)


TO SCOPE (INPUT)
TRI-STATE CONTROL
TO SCOPE (OUTPUT)
PULSE GENERATOR (Note 1)
50Ω
+1.5V for t_{HZ} and t_{ZH}
−1.5V for t_{LZ} and t_{ZL}
DIFFERENTIAL INPUTS
C_L = 15 pF (Note 2)
2.0 kΩ
SW1
+5.0V
5.0 kΩ
(Note 3)
SW2

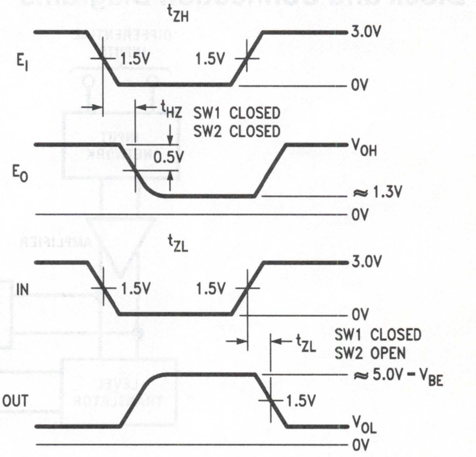
TL/F/9616-5

FIGURE 3. Propagation Delay TRI-STATE Control Input to Output


t_{LZ}
IN
1.5V
1.5V
3.0V
0V
t_{LZ}
SW1 CLOSED
SW2 CLOSED
≈ 1.3V
OUT
0.5V
V_{OL}
0V
t_{ZH}
IN
1.5V
1.5V
3.0V
0V
t_{ZH}
SW1 OPEN
SW2 CLOSED
V_{OH}
OUT
1.5V
0V

TL/F/9616-6

FIGURE 3a


t_{ZH}
E_I
1.5V
1.5V
3.0V
0V
t_{HZ}
SW1 CLOSED
SW2 CLOSED
V_{OH}
E_O
0.5V
≈ 1.3V
0V
t_{ZL}
IN
1.5V
1.5V
3.0V
0V
t_{ZL}
SW1 CLOSED
SW2 OPEN
≈ 5.0V − V_{BE}
OUT
1.5V
V_{OL}
0V

TL/F/9616-7

FIGURE 3b

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL} = 6.0$ ns (10% to 90%), $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN916 or equivalent.

National Semiconductor

DS3486 Quad RS-422, RS-423 Line Receiver

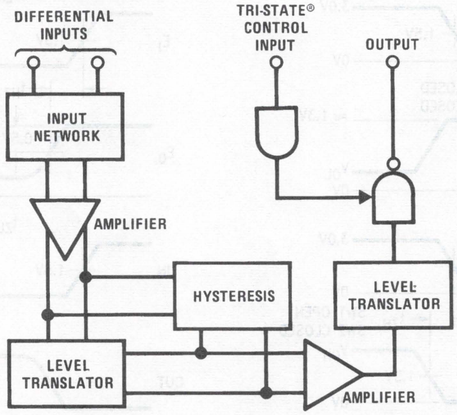
General Description

National's quad RS-422, RS-423 receiver features four independent receiver chains which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Features

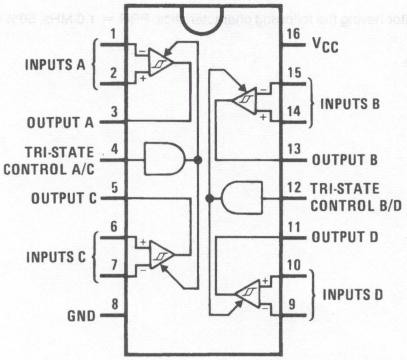
- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs (PIA compatible)
- Internal hysteresis −140 mV (typ)
- Fast propagation times −18 ns (typ)
- TTL compatible
- Single 5V supply voltage
- Pin compatible and interchangeable with MC3486

Block and Connection Diagrams


DIFFERENTIAL INPUTS
TRI-STATE® CONTROL INPUT
OUTPUT
INPUT NETWORK
AMPLIFIER
HYSTERESIS
LEVEL TRANSLATOR
LEVEL TRANSLATOR
AMPLIFIER

TL/F/5779–1

Dual-In-Line Package


1
2
INPUTS A
3
OUTPUT A
4
TRI-STATE CONTROL A/C
5
OUTPUT C
6
7
INPUTS C
8
GND
16
V_{CC}
15
14
INPUTS B
13
OUTPUT B
12
TRI-STATE CONTROL B/D
11
OUTPUT D
10
9
INPUTS D

TL/F/5779–2

Top View

Order Number DS3486J, DS3486M or DS3486N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	±25V
Input Differential Voltage, V_{ID}	±25V
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433mW
Molded Dip Package	1362 mW
SO Package	1002 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate Dip molded package 10.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	−7.0	7.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V. See Note 2.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)		2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage	−7V ≤ V_{IC} ≤ 7V, V_{IH} TRI-STATE = 2V I_O = −0.4 mA, V_{OH} ≥ 2.7V		0.070	0.2	V
		I_O = 8 mA, V_{OL} ≥ 0.5V		0.070	−0.2	V
$I_{IB\ (D)}$	Input Bias Current	V_{CC} = 0V or 5.25V, Other Inputs at 0V				
		V_I = −10V			−3.25	mA
		V_I = −3V			−1.50	mA
		V_I = 3V			1.50	mA
		V_I = 10V			3.25	mA
	Input Balance	−7V ≤ V_{IC} ≤ 7V, $V_{IH(3C)}$ = 2V, (Note 4)				
	V_{OH}	I_O = −0.4 mA, V_{ID} = 0.4V	2.7			V
	V_{OL}	I_O = 8 mA, V_{ID} = −0.4V			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)}$ = 3V, V_{IL} = 0.8V, V_{OL} = 0.5V			−40	μA
		$V_{I(D)}$ = −3V, V_{IL} = 0.8V, V_{OH} = 2.7V			40	μA
I_{OS}	Output Short-Circuit Current	$V_{I(D)}$ = 3V, V_{IH} TRI-STATE = 2V, V_O = 0V, (Note 3)	−15		−100	mA
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)	V_{IL} = 0.5V			−100	μA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)	V_{IH} = 2.7V			20	μA
		V_{IH} = 5.25V			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	I_{IN} = −10 mA			−1.5	V
I_{CC}	Power Supply Current	All Inputs V_{IL} = 0V			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

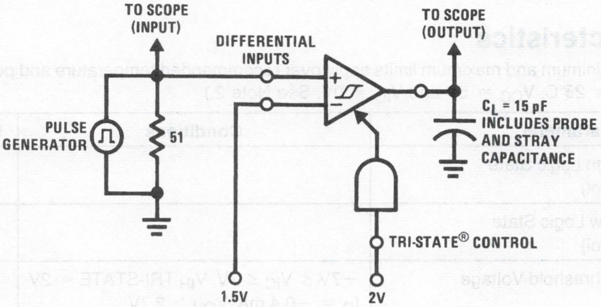
Note 3: Only one output at a time should be shorted.

Note 4: Refer to EIA RS-422/3 for exact conditions.

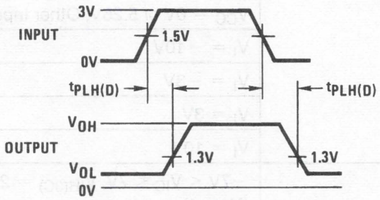
Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms


TO SCOPE (INPUT)
DIFFERENTIAL INPUTS
TO SCOPE (OUTPUT)
+
−
PULSE GENERATOR
51
C_L = 15 pF INCLUDES PROBE AND STRAY CAPACITANCE
TRI-STATE® CONTROL
1.5V
2V

TL/F/5779-3

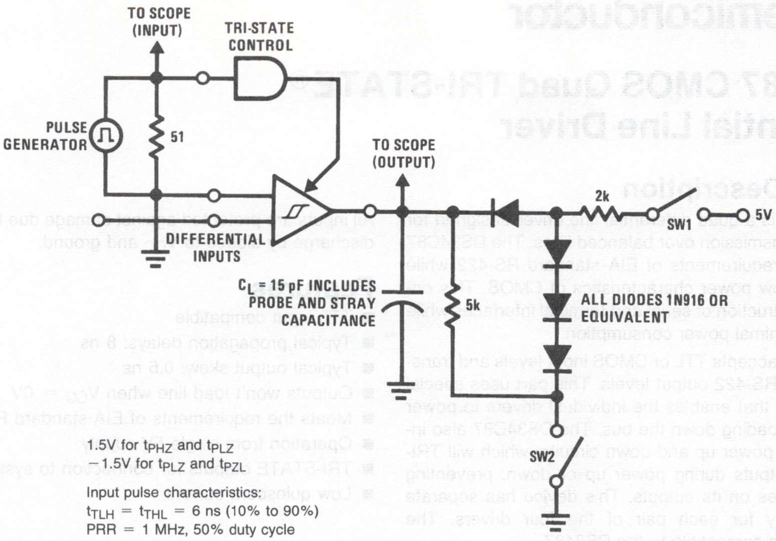

3V
INPUT
1.5V
0V
$t_{PLH(D)}$
$t_{PLH(D)}$
V_{OH}
OUTPUT
1.3V
1.3V
V_{OL}
0V

TL/F/5779-4

Input pulse characteristics:
t_{TLH} = t_{THL} = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

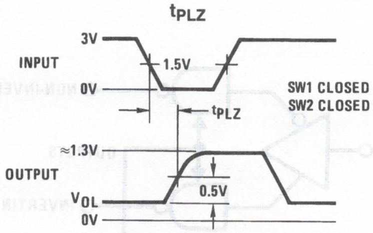
AC Test and Switching Time Waveforms (Continued)


TO SCOPE (INPUT)
TRI-STATE CONTROL
PULSE GENERATOR
51
TO SCOPE (OUTPUT)
2k
SW1
5V
DIFFERENTIAL INPUTS
C_L = 15 pF INCLUDES PROBE AND STRAY CAPACITANCE
5k
ALL DIODES 1N916 OR EQUIVALENT
SW2

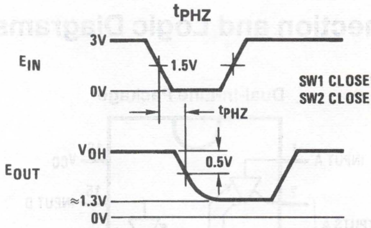
1.5V for t_{PHZ} and t_{PLZ}
−1.5V for t_{PLZ} and t_{PZL}

Input pulse characteristics:
$t_{TLH} = t_{THL} = 6$ ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

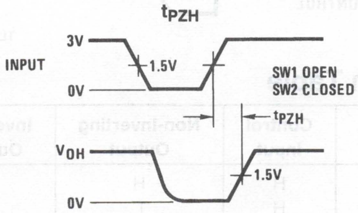
TL/F/5779–5


t_{PLZ}
3V
INPUT
1.5V
0V
t_{PLZ}
SW1 CLOSED
SW2 CLOSED
≈1.3V
OUTPUT
0.5V
V_{OL}
0V

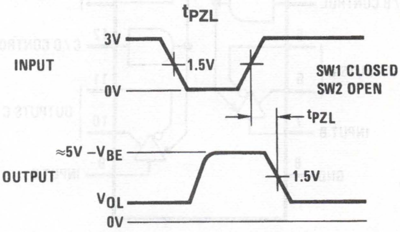
TL/F/5779–6


t_{PHZ}
3V
E_{IN}
1.5V
0V
t_{PHZ}
SW1 CLOSED
SW2 CLOSED
V_{OH}
0.5V
E_{OUT}
≈1.3V
0V

TL/F/5779–7


t_{PZH}
3V
INPUT
1.5V
0V
SW1 OPEN
SW2 CLOSED
t_{PZH}
V_{OH}
1.5V
0V

TL/F/5779–8


t_{PZL}
3V
INPUT
1.5V
0V
SW1 CLOSED
SW2 OPEN
t_{PZL}
≈5V −V_{BE}
OUTPUT
1.5V
V_{OL}
0V

TL/F/5779–9

FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor

PRELIMINARY

DS34C87 CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS34C87 is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The DS34C87 also includes special power up and down circuitry which will TRI-STATE the outputs during power up or down, preventing spurious glitches on its outputs. This device has separate enable circuitry for each pair of the four drivers. The DS34C87 is pin compatible to the DS3487.

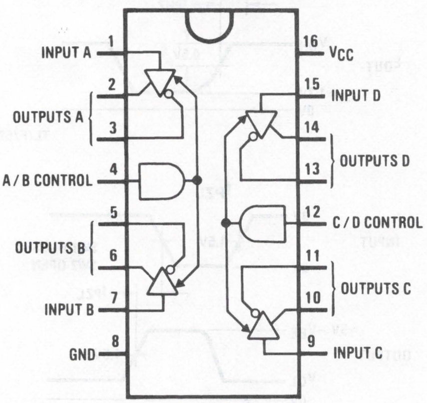
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 8 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

Connection and Logic Diagrams

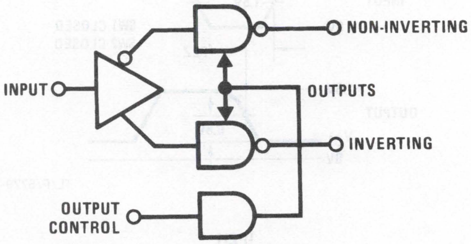
Dual-In-Line Package



TL/F/8576–1

Top View

Order Number DS34C87J, DS34C87N or DS34C87M
See NS Package Number J16A, M16A or N16A



TL/F/8576–2

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (Note 3) (P_D)	500 mW
Lead Temperature (T_L) (Soldering 4 sec)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltqge (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = -20$ mA	2.5			V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 48$ mA			0.5	V
V_T	Differential Output Voltage	$R_L = 100\ \Omega$ (Note 5)	2.0			V
$\lvert V_T\rvert - \lvert\overline{V}_T\rvert$	Difference In Differential Output	$R_L = 100\ \Omega$ (Note 5)			0.4	V
V_{OS}	Common Mode Output Voltage	$R_L = 100\ \Omega$ (Note 5)			3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	$R_L = 100\ \Omega$ (Note 5)			0.4	V
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}			±1.0	µA
I_{CC}	Quiescent Supply Current	$I_{OUT} = 0\ \mu A$, $V_{IN} = V_{CC}$ or GND V_{IN} = 2.4V or 0.5V (Note 6)		200 0.8		µA mA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Control = V_{IL}		±0.5	±5.0	µA
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Note 7)	−30		−150	mA
I_{OFF}	Output Leakage Current Power Off	V_{CC} = 0V: V_{OUT} = 6V V_{CC} = 0V: V_{OUT} = −0.25V			100 −100	µA µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.
ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V \pm 10\%$, $t_r = t_f = 6$ ns (*Figures 1, 2, 3,* and *4*) (Note 4)

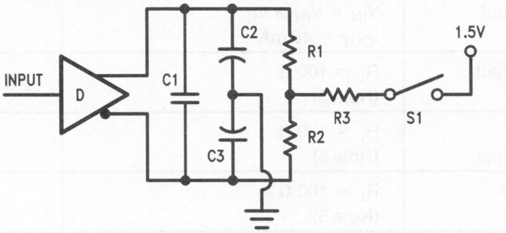
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		8		ns
Skew	(Note 8)	S1 Open		0.5		ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		8		ns
t_{PZH}	Output Enable Time	S1 Closed		13		ns
t_{PZL}	Output Enable Time	S1 Closed		15		ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		9		ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		10		ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			10		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V^2_{CC} f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Test Circuit and Switching Time Waveforms

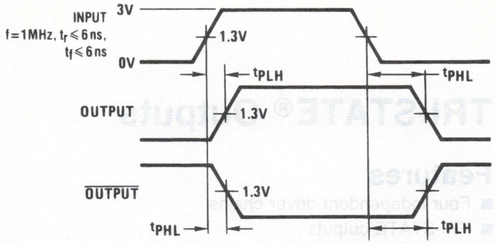


TL/F/8576-3

Note: C1 = C2 = C3 = 40 pF, R1 = R2 = 50Ω, R3 = 500Ω

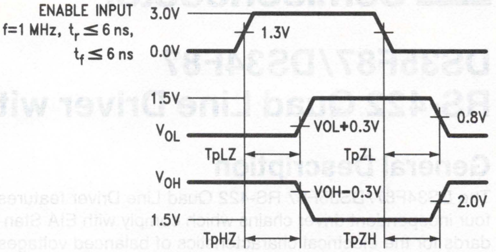
FIGURE 1. AC Test Circuit

AC Test Circuit and Switching Time Waveforms (Continued)


INPUT
f=1MHz, $t_r \leq 6$ ns, $t_f \leq 6$ ns
3V
0V
1.3V
t_{PLH}
t_{PHL}
OUTPUT
1.3V
OUTPUT
1.3V
t_{PHL}
t_{PLH}

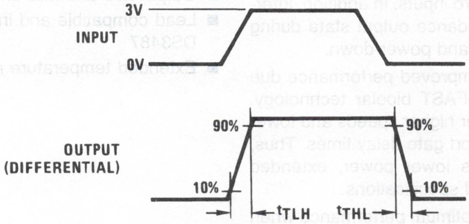
TL/F/8576-4

FIGURE 2. Propagation Delays


ENABLE INPUT
f=1 MHz, $t_r \leq 6$ ns, $t_f \leq 6$ ns
3.0V
0.0V
1.3V
1.5V
V_{OL}
VOL+0.3V
0.8V
TpLZ
TpZL
V_{OH}
VOH−0.3V
2.0V
1.5V
TpHZ
TpZH

TL/F/8576-5

FIGURE 3. Enable and Disable Times


3V
INPUT
0V
OUTPUT (DIFFERENTIAL)
90%
90%
10%
10%
t_{TLH}
t_{THL}

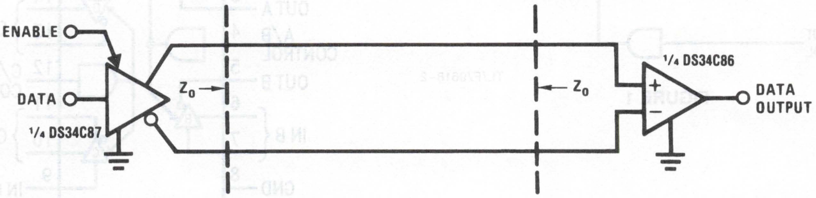
Input pulse; f = 1MHz, 50%; $t_r = t_f \leq 6$ns.

TL/F/8576-7

FIGURE 4. Differential Rise and Fall Times

Typical Applications

Two-Wire Balanced System, RS-422


ENABLE
DATA
1/4 DS34C87
Z_0
Z_0
1/4 DS34C86
+
−
DATA OUTPUT

TL/F/8576-8

National Semiconductor

DS35F87/DS34F87
RS-422 Quad Line Driver with TRI-STATE® Outputs

General Description

The DS34F87/DS35F87 RS-422 Quad Line Driver features four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltages digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. All input leads are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power-up and power-down.

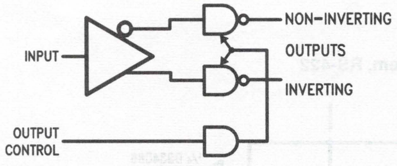
The DS34F87/DS35F87 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F87/DS35F87 features lower power, extended temperature range, and improved specifications.

The DS34F87/DS35F87 offers optimum performance when used with the DS34F86/DS35F86 Quad Line Receiver.

Features

- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs
- Fast propagation time
- TTL compatible
- Single 5.0V supply voltage
- Output rise and falls times less than 20 ns
- Lead compatible and interchangeable with MC3487 and DS3487
- Extended temperature range

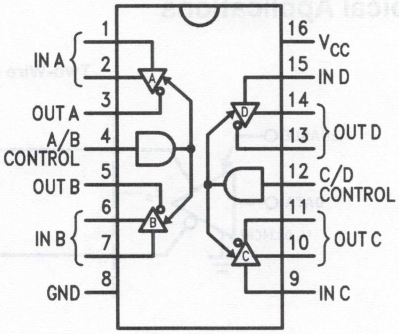
Block and Connection Diagrams



TL/F/9618-2

FIGURE 1

16-Lead DIP and SO-16 Package



TL/F/9618-1

Top View

Order Number DS34F87J or DS35F87J
See NS Package Number J16A*

Order Number DS34F87M
See NS Package Number M16A

Order Number DS34F87N
See NS Package Number N16A

*For most current package information, contact product marketing.

Function Table (Each Driver)

Input	Enable	Output	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-16	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP and SO-16 (soldering, 10 sec.)	265°C
Supply Voltage	8.0V
Input Voltage	5.5V

Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C; derate SO package 7.7 mW°C above 25°C.

Operating Range

DS34F87	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS35F87	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{IL}	Input Current LOW	$V_{IL} = 0.5V$			−200	μA
I_{IH}	Input Current HIGH	$V_{IH} = 2.7V$			+50	μA
		$V_{IH} = 5.5V$			+100	
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA			−1.5	V
V_{OL}	Output Voltage LOW	$I_{OL} = 48$ mA			0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20$ mA	2.5			V
I_{OS}	Output Short Circuit Current (Note 4)	$V_{IH} = 2.0V$	−40		−140	mA
I_{OZ}	Output Leakage Current Hi-Z State	$V_{IL} = 0.5V, V_{IL}(z) = 0.8V$			±100	μA
		$V_{IH} = 2.7V, V_{IL}(z) = 0.8V$			±100	
$I_{OL(off)}$	Output Leakage Current Power Off	$V_{OH} = 6.0V, V_{CC} = 0V$			+100	μA
		$V_{OL} = -0.25V, V_{CC} = 0V$			−100	
$V_{OS}-\overline{V}_{OS}$	Output Offset Voltage Difference (Note 5)				±0.4	V
V_{OD}	Output Differential Voltage (Note 5)		2.0			V
ΔV_{OD}	Output Differential Voltage Change				±0.4	V
I_{CCX}	Supply Current	Control Leads Gnd			50	mA
I_{CC}		Control Leads 2.0V			40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F87 and across the 0°C to +70°C range for the DS34F87. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

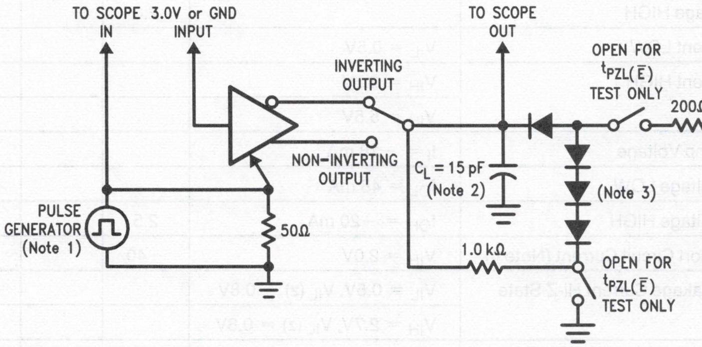
Note 5: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics $V_{CC} = 5.0\text{ V}, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Times	High to Low Input			20	ns
t_{PLH}		Low to High Input			15	ns
t_{THL}	Output Transition Times—Differential	High to Low Input			15	ns
t_{TLH}		Low to High Input			15	ns
$t_{PHZ(E)}$	Propagation Delay Control to Output	$R_L = 200, C_L = 50\text{ pF}$			25	ns
$t_{PLZ(E)}$		$R_L = 200, C_L = 50\text{ pF}$			25	ns
$t_{PZH(E)}$		$R_L = \infty, C_L = 50\text{ pF}$			25	ns
$t_{PZL(E)}$		$R_L = 200, C_L = 50\text{ pF}$			25	ns
SKEW	Output to Output	Load = (Note 1)			4.5	ns

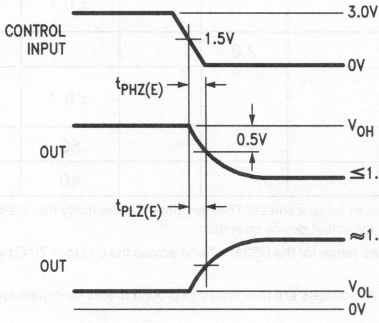
Note 1: $C_L = 50\text{ pF}, V_I = 1.5V \text{ to } V_O = 1.5V, V_{PULSE} = 0V \text{ to } +3.0V$.

Parameter Measurement Information


TO SCOPE
IN
3.0V or GND
INPUT
INVERTING
OUTPUT
NON-INVERTING
OUTPUT
PULSE
GENERATOR
(Note 1)
50Ω
TO SCOPE
OUT
$C_L = 15$ pF
(Note 2)
1.0 kΩ
OPEN FOR
$t_{PZL(\overline{E})}$
TEST ONLY
200Ω
+5V
(Note 3)
OPEN FOR
$t_{PZL(\overline{E})}$
TEST ONLY

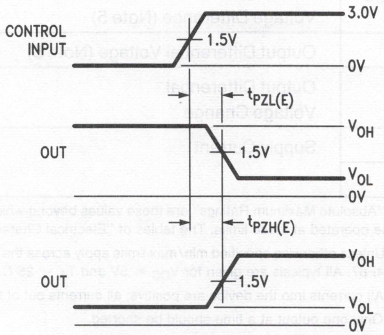
TL/F/9618-3

FIGURE 2. TRI-STATE Enable Test Circuit and Waveforms


CONTROL
INPUT
3.0V
1.5V
0V
$t_{PHZ(E)}$
V_{OH}
0.5V
OUT
≤1.5V
$t_{PLZ(E)}$
≈1.5V
OUT
V_{OL}
0V

TL/F/9618-4

FIGURE 2a


CONTROL
INPUT
3.0V
1.5V
0V
$t_{PZL(E)}$
V_{OH}
OUT
1.5V
V_{OL}
0V
$t_{PZH(E)}$
V_{OH}
OUT
1.5V
V_{OL}
0V

TL/F/9618-5

FIGURE 2b

Parameter Measurement Information (Continued)

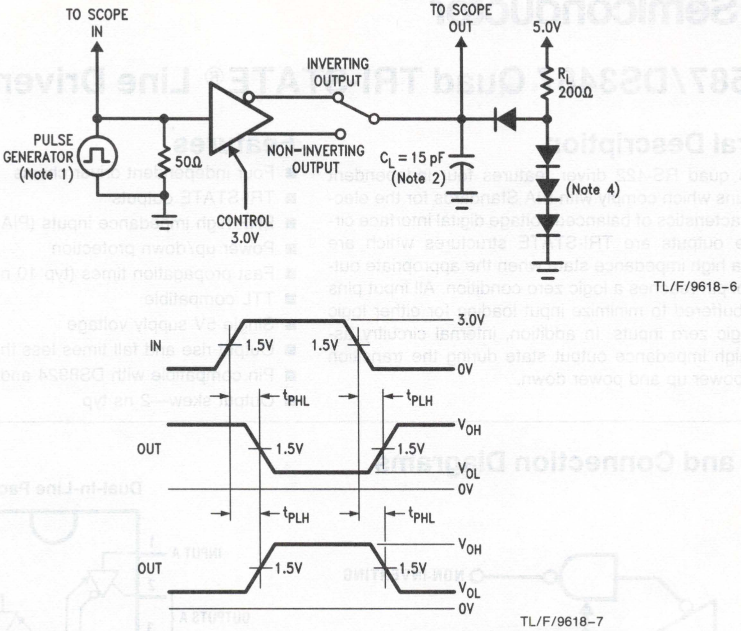

TO SCOPE
IN
TO SCOPE
OUT
5.0V
INVERTING
OUTPUT
R_L
200Ω
PULSE
GENERATOR
(Note 1)
50Ω
NON-INVERTING
OUTPUT
C_L = 15 pF
(Note 2)
(Note 4)
CONTROL
3.0V
TL/F/9618-6
3.0V
IN
1.5V
1.5V
0V
t_{PHL}
t_{PLH}
V_{OH}
OUT
1.5V
1.5V
V_{OL}
0V
t_{PLH}
t_{PHL}
V_{OH}
OUT
1.5V
1.5V
V_{OL}
0V
TL/F/9618-7

FIGURE 3. Propagation Delay Times Input to Output Waveforms and Test Circuit

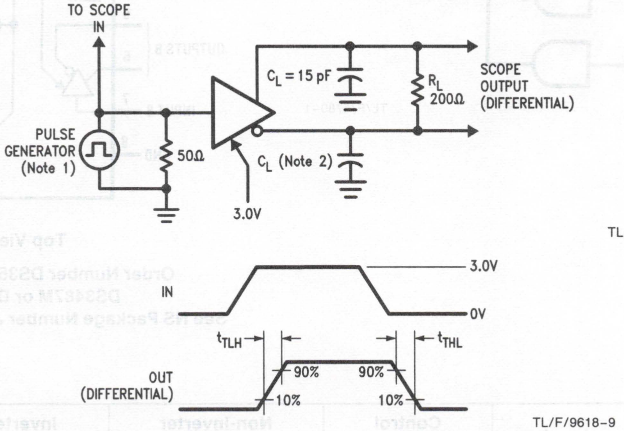

TO SCOPE
IN
C_L = 15 pF
R_L
200Ω
SCOPE
OUTPUT
(DIFFERENTIAL)
PULSE
GENERATOR
(Note 1)
50Ω
C_L (Note 2)
3.0V
TL/F/9618-8
3.0V
IN
0V
t_{TLH}
t_{THL}
OUT
(DIFFERENTIAL)
90%
90%
10%
10%
TL/F/9618-9

FIGURE 4. Output Transition Times Circuit and Waveforms

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL} \leq 5.0$ ns (10% to 90%), $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN3064 or equivalent.

Note 4: All diodes are IN914 or equivalent.

National Semiconductor

DS3587/DS3487 Quad TRI-STATE® Line Driver

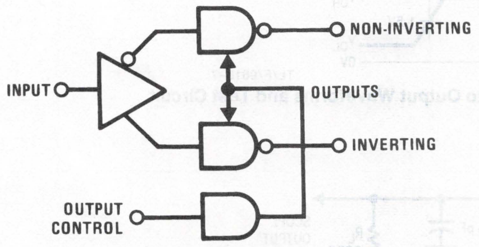
General Description

National's quad RS-422 driver features four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

Features

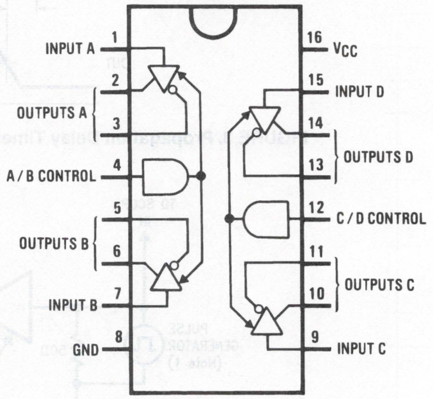
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs (PIA compatible)
- Power up/down protection
- Fast propagation times (typ 10 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with DS8924 and MC3487
- Output skew—2 ns typ

Block and Connection Diagrams


NON-INVERTING
INPUT
OUTPUTS
INVERTING
OUTPUT CONTROL

TL/F/5780-1

Dual-In-Line Package


INPUT A
1
2
OUTPUTS A
3
A/B CONTROL
4
5
OUTPUTS B
6
INPUT B
7
GND
8
16
VCC
15
INPUT D
14
13
OUTPUTS D
12
C/D CONTROL
11
10
OUTPUTS C
9
INPUT C

TL/F/5780-2

Top View

Order Number DS3587J, DS3487J, DS3487M or DS3487N
See NS Package Number J16A, M16A or N16A

Truth Table

Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate DIP molded package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3587	4.5	5.5	V
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3587	−55	+125	°C
DS3487	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	$V_{IL} = 0.5V$				−200	μA
I_{IH}	Input High Current		$V_{IH} = 2.7V$			50	μA
			$V_{IH} = 5.5V$			100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				−1.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 48$ mA				0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -20$ mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		$V_O = 0.5V$			−100	μA
			$V_O = 5.5V$			100	μA
I_{OFF}	Output Leakage Current Power OFF	$V_{CC} = 0V$	$V_O = 6V$			100	μA
			$V_O = -0.25V$			−100	μA
$\lvert V_{OS} - \overline{V}_{OS} \rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T \rvert - \lvert \overline{V}_T \rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF		17	25	ns
t_{PLZ}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF		15	25	ns
t_{PZH}	Enable to Output	$R_L = \infty$, $C_L = 50$ pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

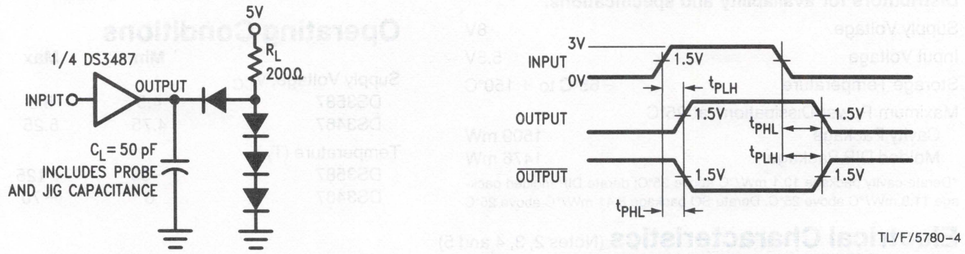
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms

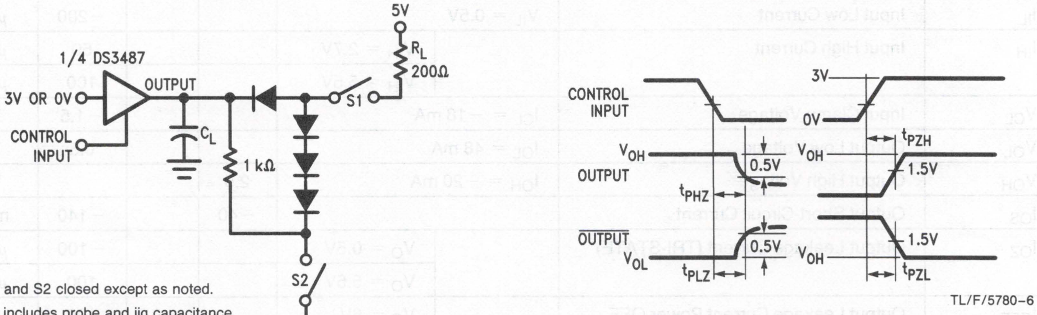

5V
R_L
200Ω
1/4 DS3487
INPUT
OUTPUT
C_L = 50 pF
INCLUDES PROBE
AND JIG CAPACITANCE
3V
INPUT
0V
1.5V
t_PLH
OUTPUT
1.5V
t_PHL
1.5V
t_PLH
OUTPUT
1.5V
1.5V
t_PHL

TL/F/5780-3

TL/F/5780-4

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 1. Propagation Delays


5V
R_L
200Ω
1/4 DS3487
3V OR 0V
OUTPUT
S1
CONTROL
INPUT
C_L
1 kΩ
S2
CONTROL
INPUT
3V
0V
t_PZH
V_OH
V_OH
0.5V
1.5V
OUTPUT
t_PHZ
OUTPUT
0.5V
1.5V
V_OL
V_OH
t_PLZ
t_PZL

S1 and S2 closed except as noted.

C_L includes probe and jig capacitance.

TL/F/5780-5

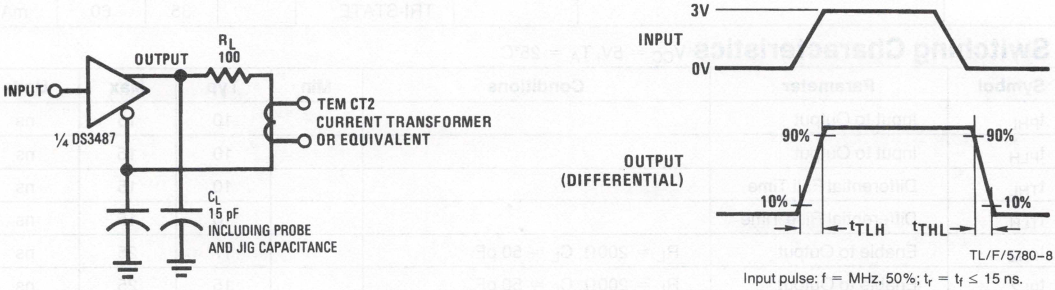
TL/F/5780-6

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

S1 = open for t_{PZH}

S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays


R_L
100
OUTPUT
INPUT
¼ DS3487
TEM CT2
CURRENT TRANSFORMER
OR EQUIVALENT
C_L
15 pF
INCLUDING PROBE
AND JIG CAPACITANCE
3V
INPUT
0V
90%
90%
OUTPUT
(DIFFERENTIAL)
10%
10%
t_TLH
t_THL

TL/F/5780-8

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

TL/F/5780-7

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

DS1603/DS3603 TRI-STATE® Dual Receivers

General Description

The DS1603/DS3603 are dual differential TRI-STATE line receivers designed for a broad range of system applications. They feature a high input impedance and low input current which reduces the loading effects on a digital transmission line, making them ideal for use in party line systems and general purpose applications like transducer preamplifiers, level translators and comparators.

The receivers feature a ±25 mV input sensitivity specified over a ±3V common mode range. Input protection diodes are incorporated in series with the collectors of the differential stage. These diodes are useful in applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off thus avoiding signal clamping. In addition, TTL compatible strobe and control lines are provide for flexibility in the application.

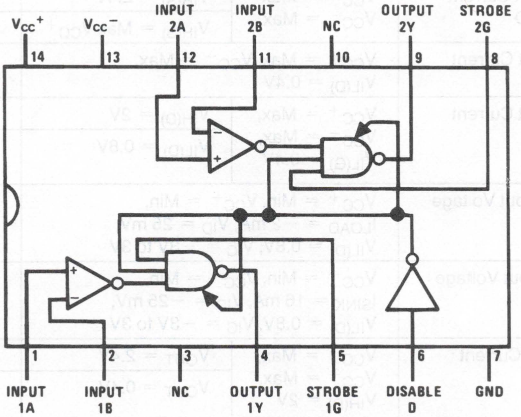
The DS1603/DS3603 are pin compatible with the DS75107, DS75108 and DS75208 series of dual line receivers.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±25 mV input sensitivity
- ±3V input common-mode range
- High-input inpedance with normal $V_{CC,}$ or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses

Connection Diagram

Dual-In-Line Package



TL/F/5781-2

Top View

Order Number DS1603J, DS3603J or DS3603N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{CC}+$)	7V
Supply Voltage ($V_{CC}-$)	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS1603			DS3603		
	Min	Nom	Max	Min	Nom	Max
Supply Voltage $V_{CC}+$	4.5V	5V	5.5V	4.75	5V	5.25V
Supply Voltage $V_{CC}-$	−4.5V	−5V	5.5V	4.75	5V	5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Electrical Characteristics $T_{MIN} \leq T_A \leq T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into 1A, 1B, 2A or 2B	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{ID} = 0.5V$, $V_{IC} = -3V$ to 3V			30	75	µA
I_{IL}	Low Level Input Current into 1A, 1B, 2A or 2B	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{ID} = -2V$, $V_{IC} = -3V$ to 3V				−10	µA
I_{IH}	High Level Input Current into 1G, 2G or D	$V_{CC}+ = \text{Max}$ $V_{CC}- = \text{Max}$	$V_{IH(S)} = 2.4V$			40	µA
			$V_{IH(S)} = \text{Max } V_{CC}+$			1	mA
I_{IL}	Low Level Input Current into D	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{IL(D)} = 0.4V$				−1.6	mA
I_{IL}	Low Level Input Current into 1G or 2G	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{IL(G)} = 0.4V$	$V_{IH(D)} = 2V$			−40	µA
			$V_{IL(D)} = 0.8V$			−1.6	mA
V_{OH}	High Level Output Voltage	$V_{CC}+ = \text{Min}$, $V_{CC}- = \text{Min}$, $I_{LOAD} = -2$ mA, $V_{ID} = 25$ mV, $V_{IL(D)} = 0.8V$, $V_{IC} = -3V$ to 3V		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC}+ = \text{Min}$, $V_{CC}- = \text{Min}$, $I_{SINK} = 16$ mA, $V_{ID} = -25$ mV, $V_{IL(D)} = 0.8V$, $V_{IC} = -3V$ to 3V				0.4	V
I_{OD}	Output Disable Current	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{IH(D)} = 2V$	$V_{OUT} = 2.4V$			40	µA
			$V_{OUT} = 0.4V$			−40	µA
I_{OS}	Short Circuit Output Current	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{IL(D)} = 0.8V$ (Note 4)		−18		−70	mA
$I_{CCH}+$	High Logic Level Supply Current from $V_{CC}+$	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{ID} = 25$ mV, $T_A = 25°C$			28	40	mA
$I_{CCH}-$	High Logic Level Supply Current from $V_{CC}-$	$V_{CC}+ = \text{Max}$, $V_{CC}- = \text{Max}$, $V_{ID} = 25$ mV, $T_A = 25°C$			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	$V_{CC}+ = \text{Min}$, $V_{CC}- = \text{Min}$, $I_{IN} = -12$ mA, $T_A = 25°C$			−1	−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603 and across the 0°C to +70°C range for the DS3603. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

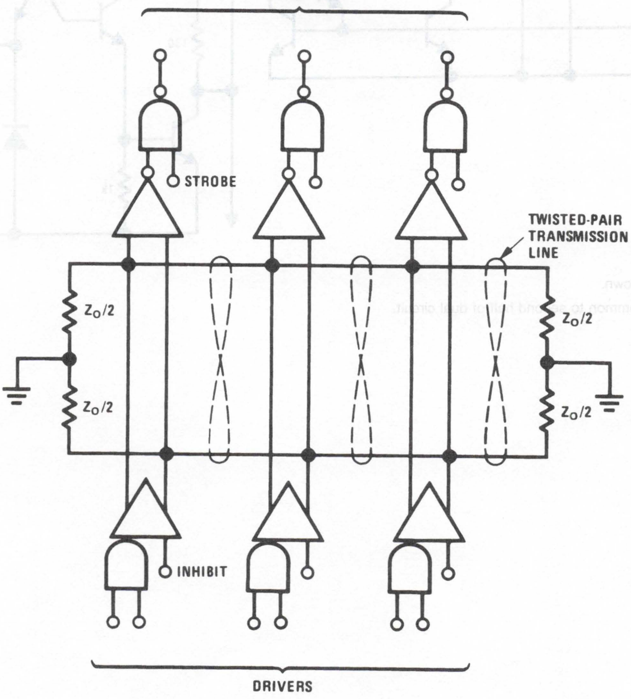
Switching Characteristics $V_{CC}^{+} = 5V$, $V_{CC}^{-} = -5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega$, $C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega$, $C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G to Output	$R_L = 390\Omega$, $C_L = 50$ pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G to Output	$R_L = 390\Omega$, $C_L = 50$ pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	$R_L = 390\Omega$, $C_L = 5$ pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	$R_L = 390\Omega$, $C_L = 5$ pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	$R_L = 1k$ to 0V, $C_L = 50$ pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	$R_L = 390\Omega$, $C_L = 50$ pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Typical Application

Line Receiver Used in a Party-Line or Data-Bus System

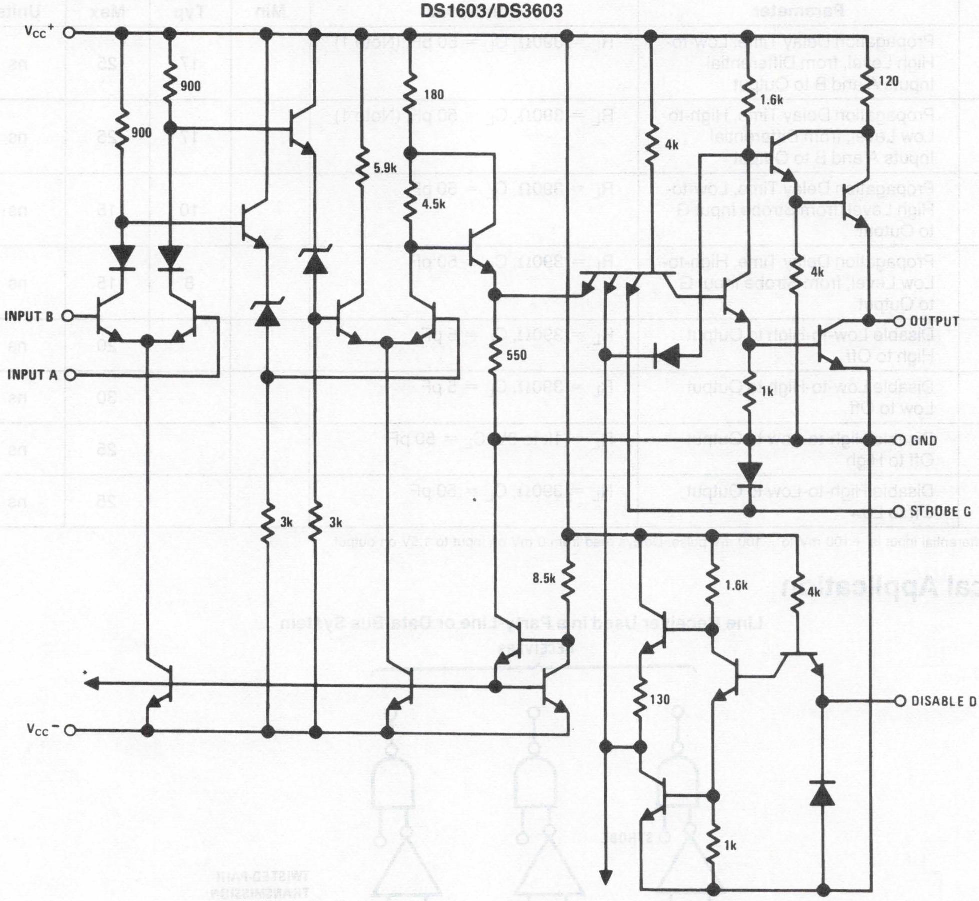


Line receivers are DS75107/DS75108 or DS3603

Line drivers are SN75109/μA75110/DS75110 or DS8831

TL/F/5781–3

Schematic Diagram (Note 1)


DS1603/DS3603
V_{CC}^+
900
900
180
5.9k
4.5k
4k
1.6k
120
4k
OUTPUT
INPUT B
INPUT A
550
1k
GND
STROBE G
3k
3k
8.5k
1.6k
4k
130
DISABLE D
1k
V_{CC}^-

TL/F/5781-6

Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

National Semiconductor

DS1650/DS1652/DS3650/DS3652 Quad Differential Line Receivers

General Description

The DS1650/DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS1650/DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

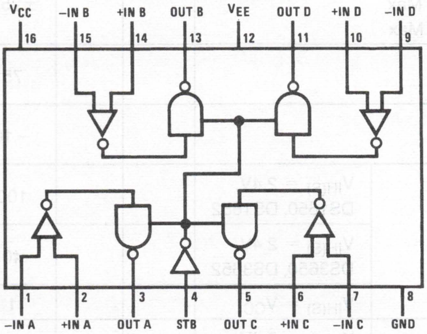
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration, the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



V_{CC}
16
−IN B
15
+IN B
14
OUT B
13
V_{EE}
12
OUT D
11
+IN D
10
−IN D
9
1
−IN A
2
+IN A
3
OUT A
4
STB
5
OUT C
6
+IN C
7
−IN C
8
GND

TL/F/5782–1

Top View

Order Number DS1650J, DS1652J, DS3650J, DS3652J, DS3650M, DS3652M, DS3650N or DS3652N

See NS Package Number J16A, M16A, or N16A

Truth Table

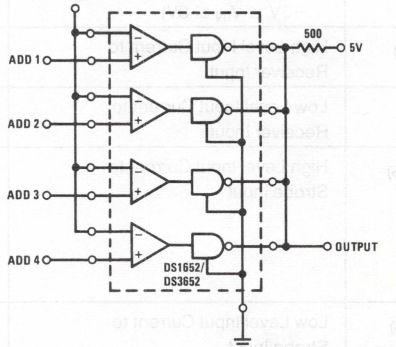
Input	Strobe	Output	
		DS1650/ DS3650	DS1652/ DS3652
$V_D \geq 25$ mV	L	H	Open
	H	Open	Open
$-25\text{ mV} \leq V_{ID} \leq 25\text{ mV}$	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State Open = TRI-STATE

H = High Logic State X = Indeterminate State

Typical Applications

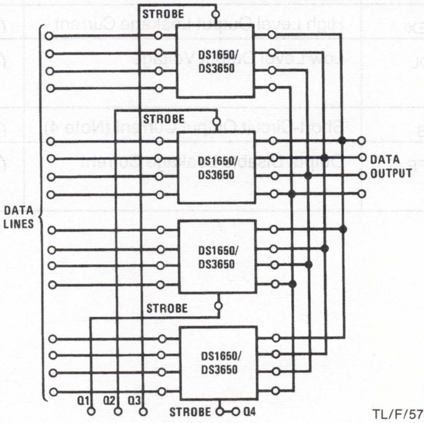
Implied "AND" Gating



V_{REF}
500
5V
ADD 1
ADD 2
ADD 3
ADD 4
OUTPUT
DS1652/
DS3652

TL/F/5782–2

Wired "OR" Data Selecting Using TRI-STATE Logic



STROBE
DS1650/
DS3650
STROBE
DS1650/
DS3650
DATA LINES
DATA OUTPUT
DS1650/
DS3650
STROBE
DS1650/
DS3650
Q1
Q2
Q3
STROBE
Q4

TL/F/5782–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	$+7.0\ V_{DC}$
V_{EE}	$-7.0\ V_{DC}$
Differential-Mode Input Signal Voltage Range, V_{IDR}	$\pm 6.0\ V_{DC}$
Common-Mode Input Voltage Range, V_{ICR}	$\pm 5.0\ V_{DC}$
Strobe Input Voltage, $V_{I(S)}$	$5.5\ V_{DC}$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1650, DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1650, DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1650, DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range Input to GND, V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

($V_{CC} = 5.0\ V_{DC}$, $V_{EE} = -5.0\ V_{DC}$, Min $\le T_A \le$ Max, unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = $-3V \le V_{IN} \le 3V$)	Min $\le V_{CC} \le$ Max Min $\ge V_{EE} \ge$ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)} = 2.4V$, DS1650, DS1652			100	µA
			$V_{IH(S)} = 2.4V$, DS3650, DS3652			40	µA
			$V_{IH(S)} = V_{CC}$			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)} = 0.4V$			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS1650, DS3650	2.4			V
I_{CEX}	High Level Output Leakage Current	*(Figure 1)*	DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V
			DS1650, DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS1650/DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS1650			100	µA
			DS3650			40	µA

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1650, DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

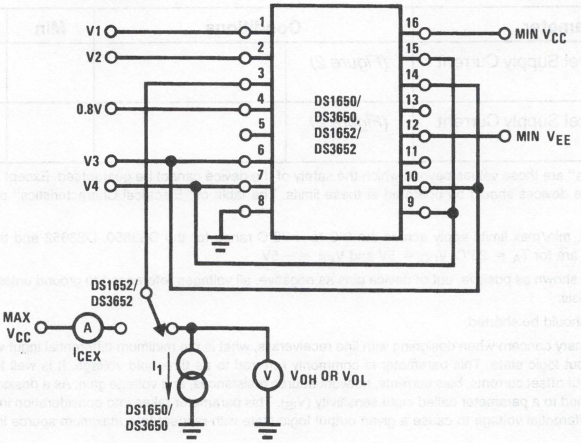
Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1650, DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics

(V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS1650/DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS1650/DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS1650/DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS1650/DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits

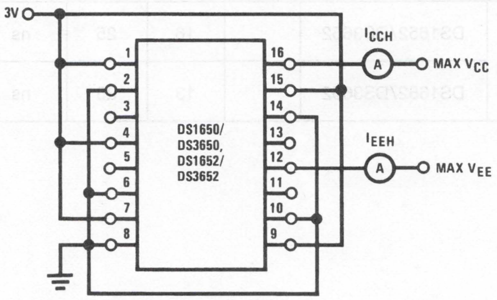

V1
V2
0.8V
V3
V4
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
DS1650/
DS3650,
DS1652/
DS3652
MIN VCC
MIN VEE
DS1652/
DS3652
MAX
VCC
A
ICEX
I1
V
VOH OR VOL
DS1650/
DS3650

TL/F/5782-4

	V1		V2		V3		V4		I1
	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS3652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		−0.4 mA −0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	+16 mA +16 mA

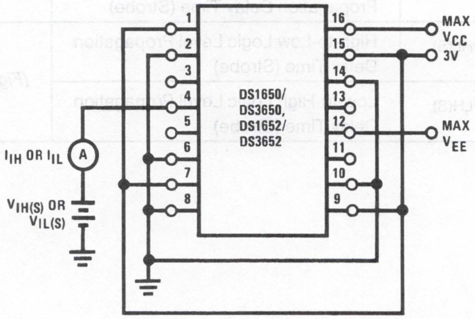
Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}


3V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
DS1650/
DS3650,
DS1652/
DS3652
ICCH
A
MAX VCC
IEEH
A
MAX VEE

TL/F/5782-5

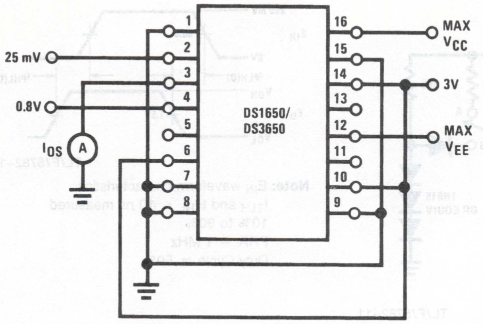
FIGURE 2. I_{CCH} and I_{EEH}


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
DS1650/
DS3650,
DS1652/
DS3652
MAX
VCC
3V
MAX
VEE
IIH OR IIL
A
VIH(S) OR
VIL(S)

TL/F/5782-6

FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$

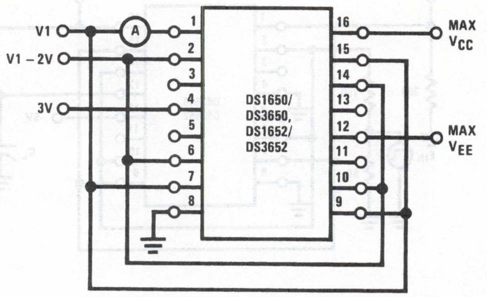
Electrical Characteristic Test Circuits (Continued)


25 mV
0.8V
I_{OS}
A
DS1650/
DS3650
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MAX
V_{CC}
3V
MAX
V_{EE}

TL/F/5782-7

Note: Channel A shown under test, other channels are tested similiarly. Only one output shorted at a time.

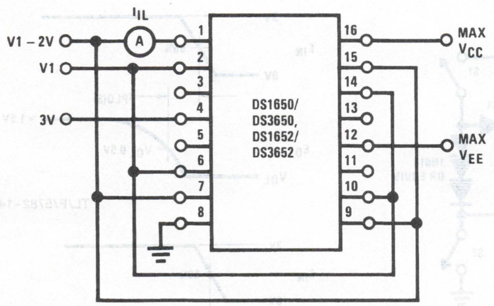
FIGURE 4. I_{OS}


V1
V1 – 2V
3V
A
DS1650/
DS3650,
DS1652/
DS3652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MAX
V_{CC}
MAX
V_{EE}

TL/F/5782-8

Note: Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to –3V.

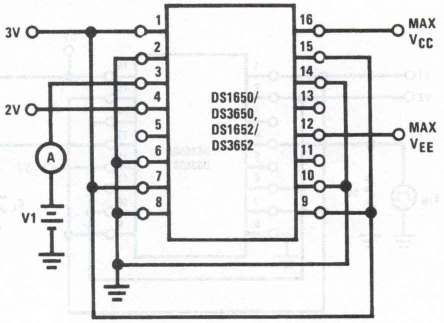
FIGURE 5. I_{IH}


I_{IL}
V1 – 2V
V1
3V
A
DS1650/
DS3650,
DS1652/
DS3652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MAX
V_{CC}
MAX
V_{EE}

TL/F/5782-9

Note: Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to –3V.

FIGURE 6. I_{IL}

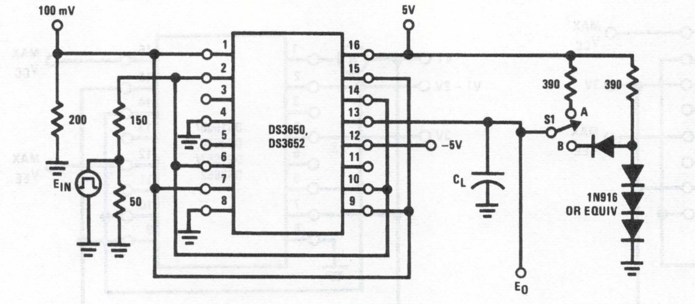

3V
2V
A
V1
DS1650/
DS3650,
DS1652/
DS3652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MAX
V_{CC}
MAX
V_{EE}

TL/F/5782-10

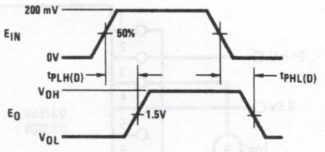
Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms


100 mV
5V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
DS3650,
DS3652
200
150
50
E$_{IN}$
−5V
C$_L$
390
390
S1
A
B
1N916
OR EQUIV
E$_O$

TL/F/5782-11

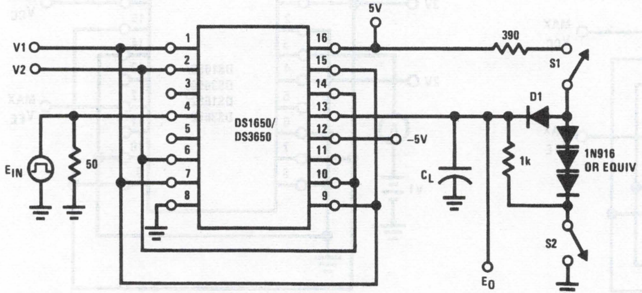

200 mV
E$_{IN}$
50%
0V
t$_{PLH(D)}$
t$_{PHL(D)}$
V$_{OH}$
E$_O$
1.5V
V$_{OL}$

TL/F/5782-12

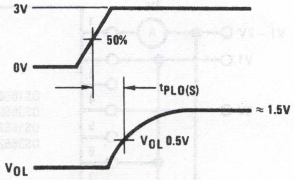
Note: E$_{IN}$ waveform characteristics:
t_{TLH} and t_{THL} $\leq$ 10 ns measured
10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

Note: Output of Channel B shown under test, other channels are tested similarly.
S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

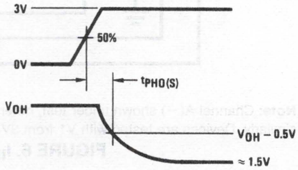
FIGURE 8. Receiver Propagation Dealy $t_{PLH(D)}$ and $t_{PHL(D)}$


V1
V2
5V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
DS1650/
DS3650
390
S1
D1
−5V
C$_L$
1k
1N916
OR EQUIV
S2
E$_{IN}$
50
E$_O$

TL/F/5782-13


3V
E$_{IN}$
50%
0V
t$_{PLO(S)}$
≈ 1.5V
E$_O$
V$_{OL}$ 0.5V
V$_{OL}$

TL/F/5782-14


3V
E$_{IN}$
50%
0V
t$_{PHO(S)}$
V$_{OH}$
E$_O$
V$_{OH}$ − 0.5V
≈ 1.5V

TL/F/5782-15

Note: Output of Channel B shown under test, other channels are tested similiarly.

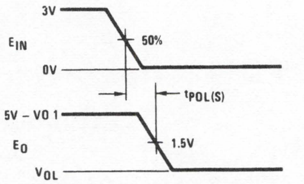
	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

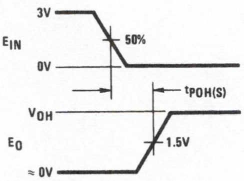
E$_{IN}$ waveform characteristics: t_{TLH} and t_{THL} $\leq$ 10 ns measured 10% to 90%

PRR = 1 MHz

Duty Cycle = 50%


3V
E$_{IN}$
50%
0V
t$_{POL(S)}$
5V − VO 1
E$_O$
1.5V
V$_{OL}$

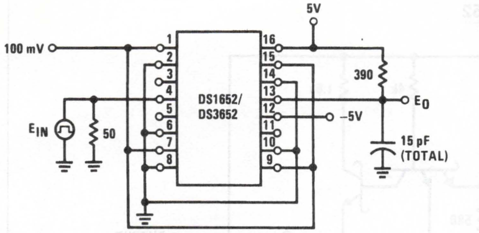
TL/F/5782-16


3V
E$_{IN}$
50%
0V
t$_{POH(S)}$
V$_{OH}$
E$_O$
1.5V
≈ 0V

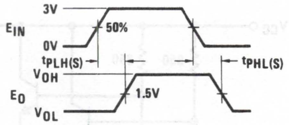
TL/F/5782-17

FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)


5V
100 mV
E_{IN}
50
DS1652/
DS3652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
390
E_O
−5V
15 pF
(TOTAL)

TL/F/5782-18


3V
E_{IN}
50%
0V
t_{PLH(S)}
t_{PHL(S)}
V_{OH}
E_O
1.5V
V_{OL}

TL/F/5782-19

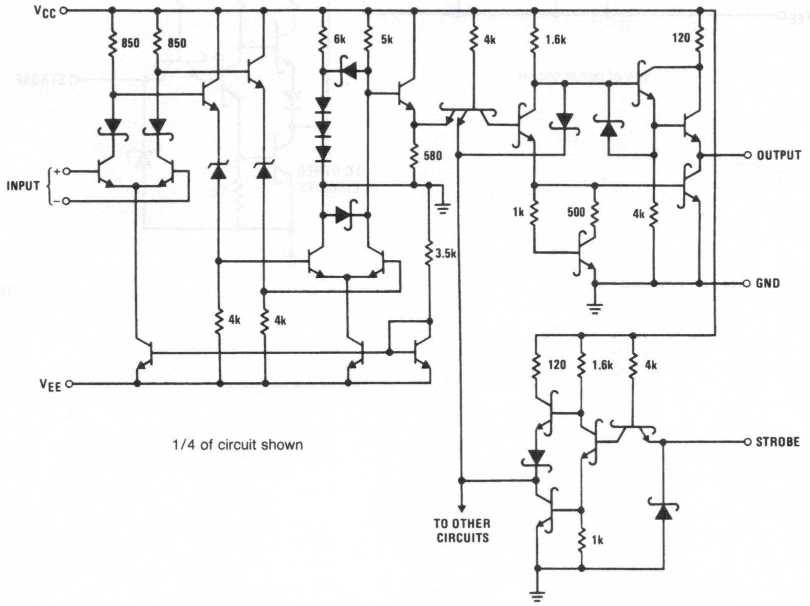
Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% and 90%
PRR = 1 MHz
Duty Cycle = 500 ns

Note: Output of Channel B shown under test, other channels are tested similarly.

FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams

DS1650/DS3650

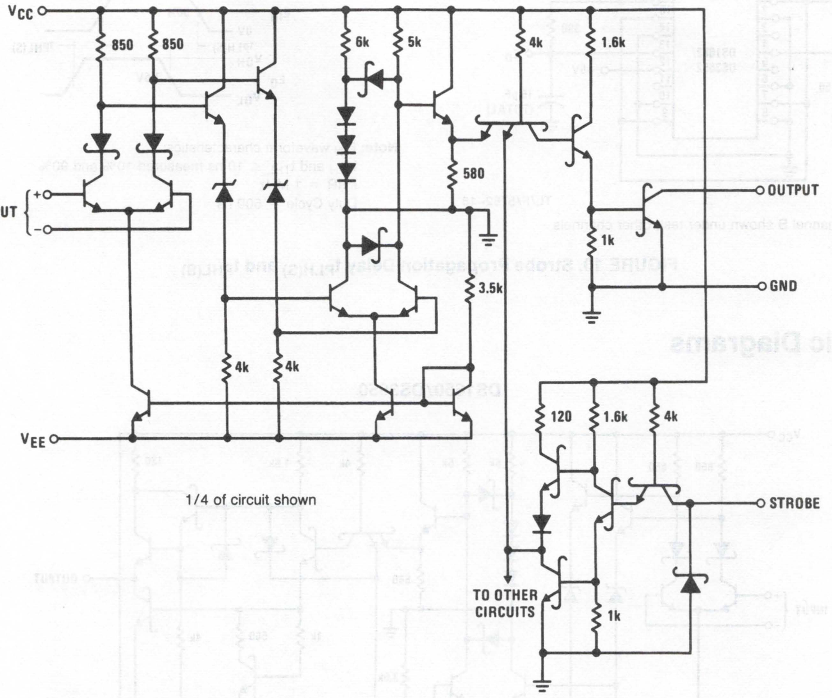

V_{CC}
850
850
6k
5k
4k
1.6k
120
580
INPUT
+
−
OUTPUT
1k
500
4k
3.5k
GND
4k
4k
V_{EE}
120
1.6k
4k
STROBE
TO OTHER CIRCUITS
1k

1/4 of circuit shown

TL/F/5782-20

Schematic Diagrams (Continued)

DS1652/DS3652


V_{CC}
850
850
6k
5k
4k
1.6k
580
INPUT
+
−
OUTPUT
1k
GND
3.5k
4k
4k
V_{EE}
120
1.6k
4k
STROBE
1/4 of circuit shown
TO OTHER CIRCUITS
1k

TL/F/5782-21

National Semiconductor

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

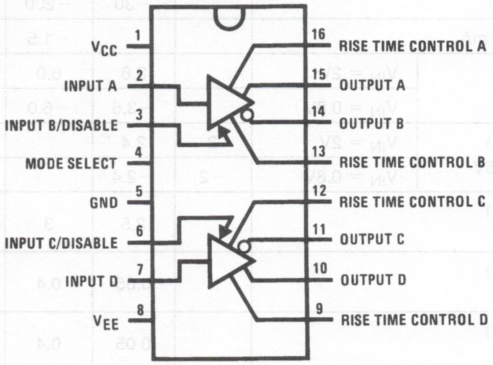
With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE control for individual outputs
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- Individual rise mode time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422 35 mW/driver typ
  - RS-423 26 mW/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Pin compatible with AM26LS30

Connection Diagram

With Mode Select LOW (RS-422 Connection)

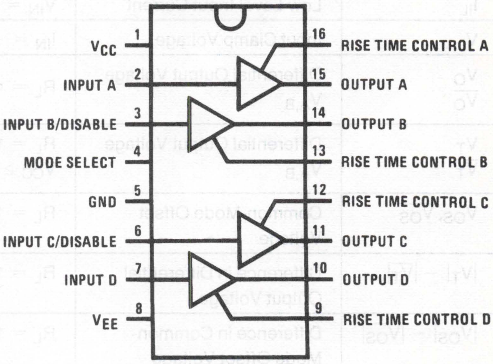


V_CC 1
INPUT A 2
INPUT B/DISABLE 3
MODE SELECT 4
GND 5
INPUT C/DISABLE 6
INPUT D 7
V_EE 8
16 RISE TIME CONTROL A
15 OUTPUT A
14 OUTPUT B
13 RISE TIME CONTROL B
12 RISE TIME CONTROL C
11 OUTPUT C
10 OUTPUT D
9 RISE TIME CONTROL D

TL/F/5783–1

Top View

With Mode Select HIGH (RS-423 Connection)



V_CC 1
INPUT A 2
INPUT B/DISABLE 3
MODE SELECT 4
GND 5
INPUT C/DISABLE 6
INPUT D 7
V_EE 8
16 RISE TIME CONTROL A
15 OUTPUT A
14 OUTPUT B
13 RISE TIME CONTROL B
12 RISE TIME CONTROL C
11 OUTPUT C
10 OUTPUT D
9 RISE TIME CONTROL D

TL/F/5783–2

Top View

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J, DS3691M or DS3691N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	$V_{IN} = 2V$		3.6	6.0	V
			$V_{IN} = 0.8V$		−3.6	−6.0	V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	$R_L = 100\Omega$ $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	2	2.4		V
			$V_{IN} = 0.8V$	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	$R_L = 100\Omega$			2.5	3	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.05	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common-Mode Offset Voltage	$R_L = 100\Omega$			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T}\rvert$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE} = 2.4V$		±10			V
I_{XA}	Output Leakage Current Power OFF	$V_{CC} = 0V$	$V_{CMR} = 10V$			100	μA
I_{XB}			$V_{CMR} = -10V$			−100	μA
I_{OX}	TRI-STATE Output Current	$V_{CC} = $ Max	$V_{CMR} \leq 10V$			100	μA
			$V_{CMR} \geq -10V$			−100	μA
I_{SA}	Output Short Circuit Current	$V_{IN} = 0.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
I_{SB}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 0V$		−80	−150	mA
			$V_{OB} = 6V$		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output Rise Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_f	Output Fall Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns
t_{PZH}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PLZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PHZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Output Voltage	R_L = ∞, (Note 6) V_{CC} ≥ 4.75V	V_{IN} = 2V	4.0	4.4	6.0	V
$\overline{V_O}$			V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω V_{CC} ≥ 4.75V	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$			V_{IN} = 0.4V	−3.6	−4.1		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$ = 4.75V, R_L = 450Ω			0.02	0.4	V
$I_X{}^+$	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 6V		2	100	μA
$I_X{}^-$	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = −6V		−2	−100	μA
$I_S{}^+$	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
$I_S{}^-$	Output Short Circuit Current	V_O = 0V	V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

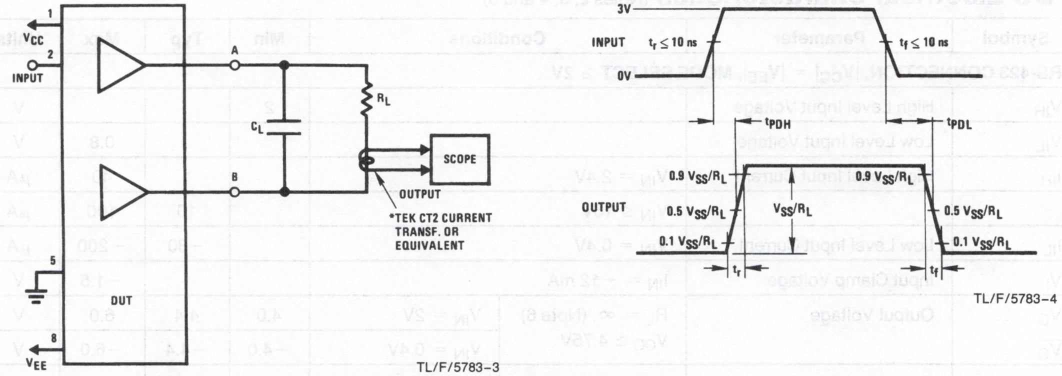
Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF *(Figure 3)*		0.06		µs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns

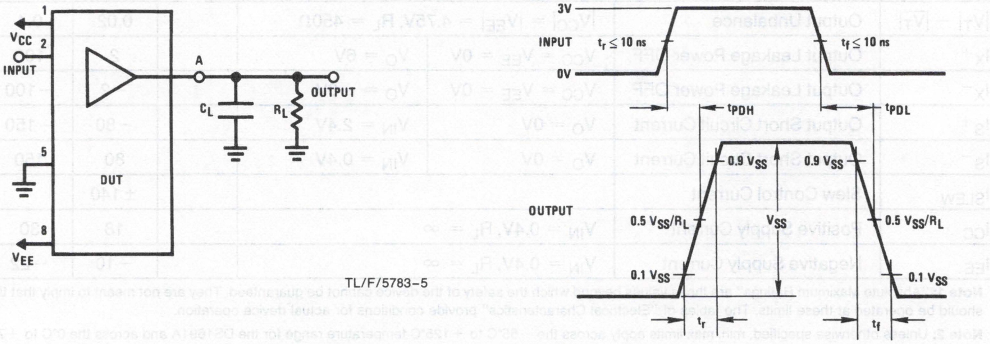
AC Test Circuits and Switching Time Waveforms


1
VCC
2
INPUT
A
RL
CL
SCOPE
B
OUTPUT
*TEK CT2 CURRENT TRANSF. OR EQUIVALENT
5
DUT
8
VEE
3V
INPUT
tr ≤ 10 ns
tf ≤ 10 ns
0V
tPDH
tPDL
0.9 VSS/RL
0.9 VSS/RL
OUTPUT
0.5 VSS/RL
VSS/RL
0.5 VSS/RL
0.1 VSS/RL
0.1 VSS/RL
tr
tf

TL/F/5783-4

TL/F/5783-3

FIGURE 1. Differential Connection

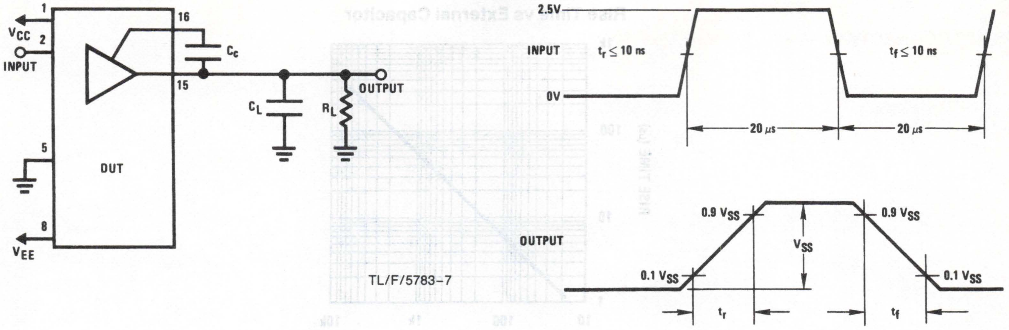

1
VCC 2
INPUT
A
CL
RL
OUTPUT
5
DUT
8
VEE
3V
INPUT
tr ≤ 10 ns
tf ≤ 10 ns
0V
tPDH
tPDL
0.9 VSS
0.9 VSS
OUTPUT
0.5 VSS/RL
VSS
0.5 VSS/RL
0.1 VSS
0.1 VSS
tr
tf

TL/F/5783-5

TL/F/5783-6

FIGURE 2. RS-423 Connection

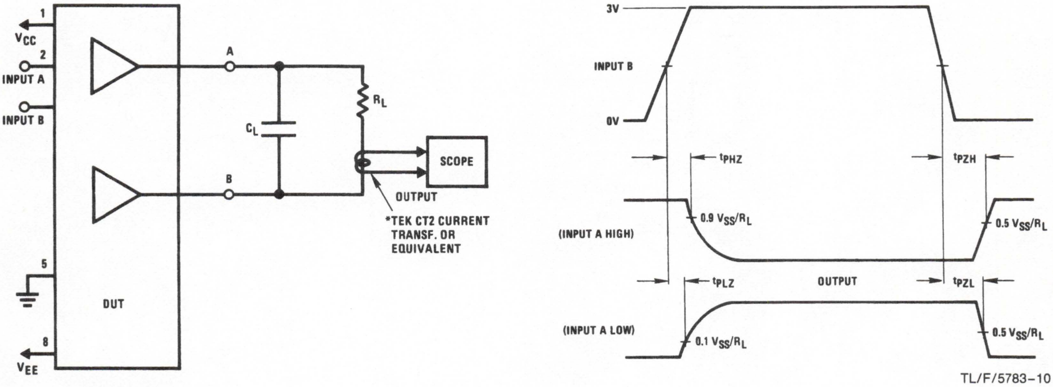
AC Test Circuits and Switching Time Waveforms (Continued)


1
V_CC 2
INPUT
16
15
C_c
C_L
R_L
OUTPUT
5
DUT
8
V_EE
2.5V
INPUT
t_r ≤ 10 ns
t_f ≤ 10 ns
0V
20 μs
20 μs
0.9 V_SS
0.9 V_SS
V_SS
OUTPUT
0.1 V_SS
0.1 V_SS
t_r
t_f

TL/F/5783-7

TL/F/5783-8

FIGURE 3. Rise Time Control for RS-423

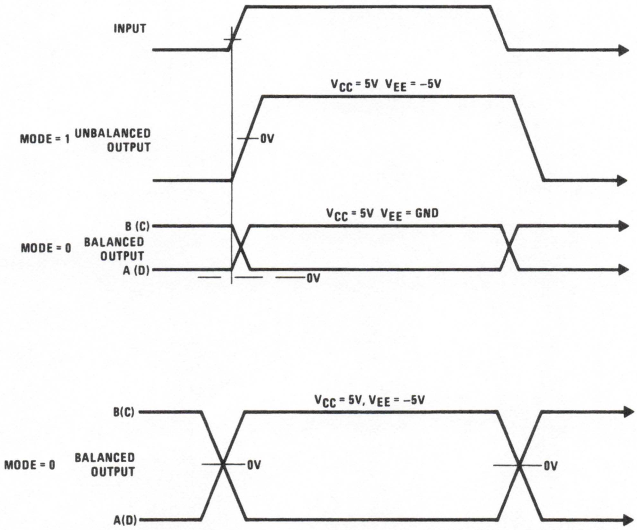

1
V_CC
2
INPUT A
INPUT B
A
R_L
C_L
B
SCOPE
OUTPUT
*TEK CT2 CURRENT TRANSF. OR EQUIVALENT
5
DUT
8
V_EE
3V
INPUT B
0V
t_PHZ
t_PZH
0.9 V_SS/R_L
0.5 V_SS/R_L
(INPUT A HIGH)
t_PLZ
OUTPUT
t_PZL
(INPUT A LOW)
0.1 V_SS/R_L
0.5 V_SS/R_L

TL/F/5783-10

TL/F/5783-9

FIGURE 4. TRI-STATE Delays

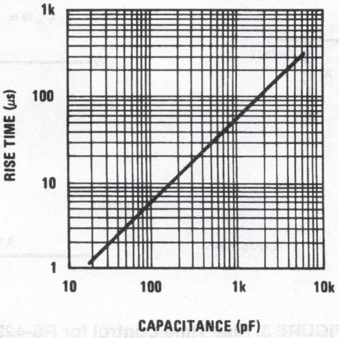
Switching Waveforms


INPUT
V_CC = 5V V_EE = −5V
MODE = 1 UNBALANCED OUTPUT
0V
V_CC = 5V V_EE = GND
B (C)
MODE = 0 BALANCED OUTPUT
A (D)
0V
V_CC = 5V, V_EE = −5V
B(C)
MODE = 0 BALANCED OUTPUT
0V
0V
A(D)

TL/F/5783-11

Typical Rise Time Control Characteristics

Rise Time vs External Capacitor



TL/F/5783–12

National Semiconductor

DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

The DS1692/DS3692 are low power Schottky TTL line drivers electrically similar to the DS1691A/DS3691 but tested to meet the requirements of MIL-STD-188-114 (see Application Note AN-216). They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end cross-talk to other receivers in the cable.

With the mode select pin low, the DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

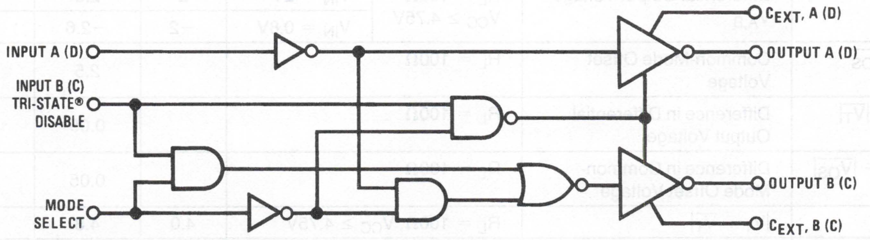
Features

- Dual differential line driver or quad single-ended line driver
- TRI-STATE differential drivers meet MIL-STD-188-114
- Short circuit protection for both source and sink outputs
- Individual rise time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption

Differential mode	35 mW/driver typ
Single-ended mode	26 mW/driver typ

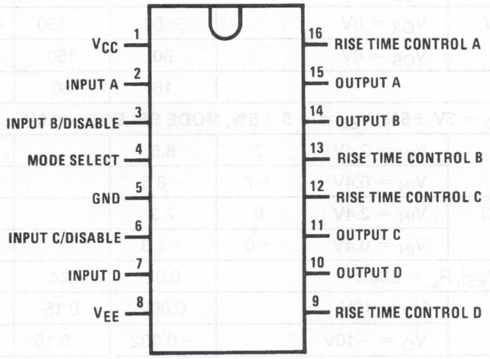
- Low current PNP inputs compatible with TTL, MOS and CMOS

Logic Diagram (½ Circuit Shown)


CEXT, A (D)
INPUT A (D)
OUTPUT A (D)
INPUT B (C)
TRI-STATE®
DISABLE
MODE
SELECT
OUTPUT B (C)
CEXT, B (C)

TL/F/5784–1

Connection Diagram


VCC 1
INPUT A 2
INPUT B/DISABLE 3
MODE SELECT 4
GND 5
INPUT C/DISABLE 6
INPUT D 7
VEE 8
16 RISE TIME CONTROL A
15 OUTPUT A
14 OUTPUT B
13 RISE TIME CONTROL B
12 RISE TIME CONTROL C
11 OUTPUT C
10 OUTPUT D
9 RISE TIME CONTROL D

TL/F/5784–2

Top View

Order Number DS1692J, DS3692J or DS3692N
See NS Package Number J16A or N16A

Truth Table

Inputs			Outputs	
Mode	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1692	−55	+125	°C
DS3692	0	+70	°C

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS1692, V_{CC} = 5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	$V_{IN} = 2V$	2.5	3.6		V
			$V_{IN} = 0.8V$	−2.5	−3.6		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	$R_L = 100\Omega$ $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	2	2.6		V
			$V_{IN} = 0.8V$	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	$R_L = 100\Omega$			2.5	3	V
$\|V_T\| - \|\overline{V_T}\|$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.05	0.4	V
$\|V_{OS}\| - \|\overline{V_{OS}}\|$	Difference in Common-Mode Offset Voltage	$R_L = 100\Omega$			0.05	0.4	V
V_{SS}	$\|V_T - \overline{V_T}\|$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$		4.0	4.8		V
I_{OX}	TRI-STATE Output Current	$V_O \leq -10V$			−0.002	−0.15	mA
		$V_O \geq 15V$			0.002	0.15	mA
I_{SA}	Output Short Circuit Current	$V_{IN} = 0.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
I_{SB}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 0V$		−80	−150	mA
			$V_{OB} = 6V$		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ±10%, V_{EE} = −5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} = −5 ±5%, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	$V_{IN} = 2.4V$	7	8.5		V
			$V_{IN} = 0.4V$	−7	−8.5		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	$R_L = 200\Omega$	$V_{IN} = 2.4V$	6	7.3		V
			$V_{IN} = 0.4V$	−6	−7.3		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$, $R_L = 200\Omega$			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		$V_O = 10V$		0.002	0.15	mA
			$V_O = -10V$		−0.002	−0.15	mA
$I_S{}^+$ $I_S{}^-$	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
			$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew Control Current				±140		µA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$		1	40	µA
		$V_{IN} \leq 15V$		10	100	µA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$		−30	−200	µA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA			−1.5	V
I_{XA} I_{XB}	Output Leakage Current Power OFF	$V_{CC} = V_{EE} = 0V$, $V_O = 15V$		0.01	0.15	mA
		$V_{CC} = V_{EE} = 0V$, $V_O = -15V$		−0.01	−0.15	mA

Switching Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
V_{CC} = 5V, V_{EE} = −5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns

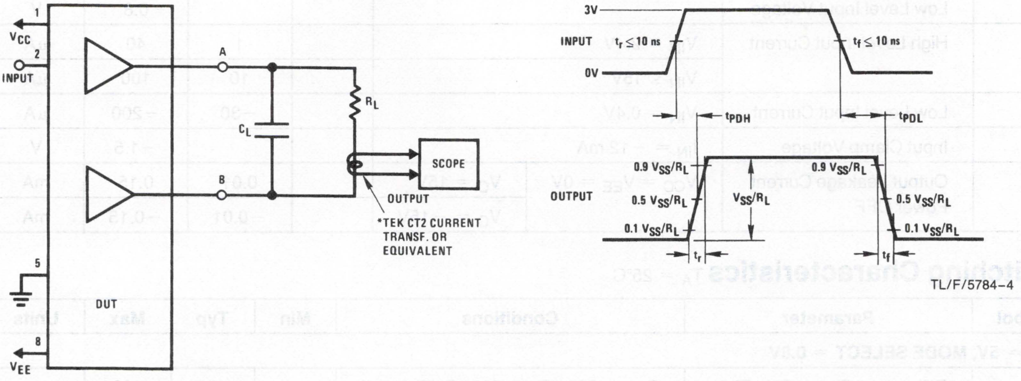
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1692 and across the 0°C to +70°C range for the DS3692. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

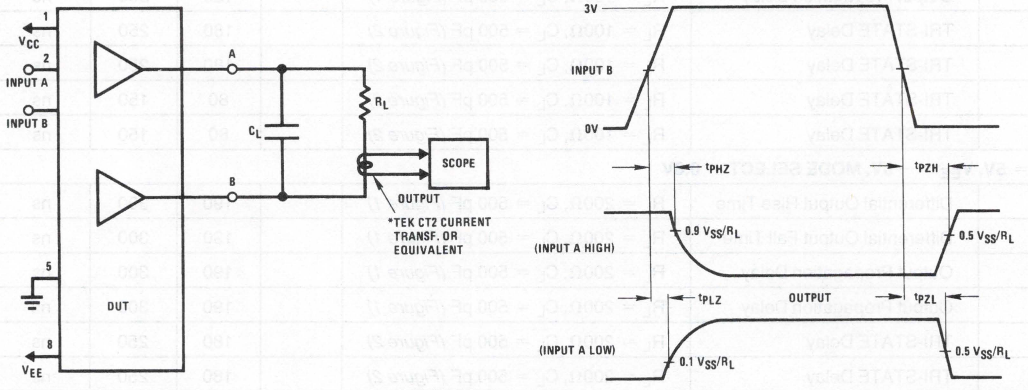
AC Test Circuits and Switching Time Waveforms


1
VCC
2
INPUT
A
RL
CL
B
SCOPE
OUTPUT
*TEK CT2 CURRENT TRANSF. OR EQUIVALENT
5
DUT
8
VEE
3V
INPUT
tr ≤ 10 ns
tf ≤ 10 ns
0V
tPDH
tPDL
0.9 VSS/RL
0.5 VSS/RL
0.1 VSS/RL
OUTPUT
VSS/RL
tr
tf

TL/F/5784-3

TL/F/5784-4

FIGURE 1. Differential Connection

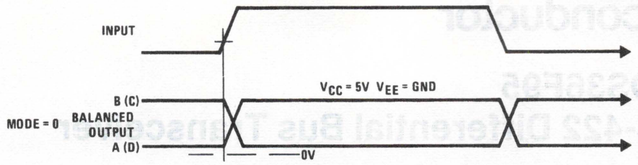

1
VCC
2
INPUT A
INPUT B
A
RL
CL
SCOPE
B
OUTPUT
*TEK CT2 CURRENT TRANSF. OR EQUIVALENT
5
DUT
8
VEE
3V
INPUT B
0V
tPHZ
tPZH
0.9 VSS/RL
0.5 VSS/RL
(INPUT A HIGH)
tPLZ
OUTPUT
tPZL
(INPUT A LOW)
0.1 VSS/RL
0.5 VSS/RL

TL/F/5784-5

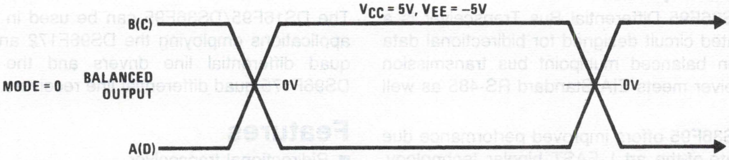
TL/F/5784-6

FIGURE 2. TRI-STATE Delays for DS1692/DS3692

Switching Waveforms

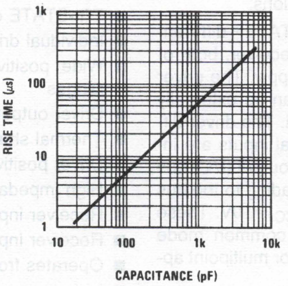

INPUT
VCC = 5V VEE = GND
B (C)
MODE = 0
BALANCED OUTPUT
A (D)
0V

TL/F/5784–7


VCC = 5V, VEE = −5V
B(C)
MODE = 0
BALANCED OUTPUT
0V
0V
A(D)

TL/F/5784–8

Typical Rise Time Control Characteristics



TL/F/5784–9

National Semiconductor

PRELIMINARY

DS16F95/DS36F95
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS16F95/DS36F95 offers improved performance due to the use of state-of-the art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS16F95/DS36F95 features lower power, extended temperature range, and improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when $V_{CC} = 0V$. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions.

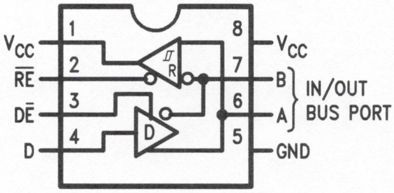
The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Meets SCSI specifications
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability +60 mA maximum
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power version
- Extended temperature range
- Pin compatible with DS3695 and SN75176A

Connection Diagram

8-Lead Dual-In-Line Package



TL/F/9629-1

Top View

Order Number DS16F95J, DS36F95J or DS36F95N
See NS Package Number* J08A or N08E

*For most current package information, contact product marketing.

Function Tables

Driver

Differential Inputs	Enable	Outputs	
D	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A–B	**$\overline{RE}$**	**R**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-8 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
SO Package	810 mW
Supply Voltage	7.0V
Differential Input Voltage	±25V
Enable Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C; derate SO package 6.5 mW°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS36F95	4.75	5.0	5.25	V
DS16F95	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	
Operating Temperature (T_A)				
DS36F95	0	+25	+70	°C
DS16F95	−55	+25	+125	

Driver Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -55$ mA	0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	$I_{OL} = 55$ mA	0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.3	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 100\Omega$, *Figure 1*		2.0	2.25		V
		$R_L = 54\Omega$, *Figure 1*		1.5	2.0		
V_{OD}	Differential Output Voltage	$V_{CM} = -7.0V$ to $+12V$	0°C to +70°C	1.5			V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω, *Figure 1*				±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled	$V_O = +12V$			1.0	mA
			$V_O = -7.0V$			−0.8	
I_{IH}	Input Current HIGH	$V_I = 2.4V$				20	μA
I_{IL}	Input Current LOW	$V_I = 0.4V$				−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0V$				−250	mA
		$V_O = 0V$				−150	
		$V_O = V_{CC}$				150	
		$V_O = +12V$				250	
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			28	mA
I_{CCX}			Outputs Disabled			25	

Driver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	25	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V		35	50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 2*	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = +12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−50	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			28	mA
I_{CCX}			Outputs Disabled			25	

Receiver Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V C_L = 15 pF, *Figure 7*	14	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	19	24	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	ns
t_{LZ}	Output Disable Time from Low Level			12	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16F95 and across the 0°C to +70°C range for the DS36F95. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

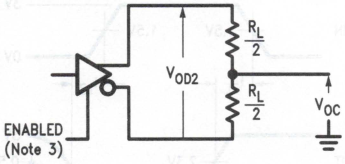
Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_T+, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standard RS-485 for exact conditions.

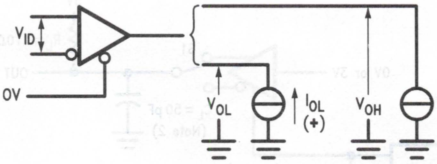
Note 9: Only one output at a time should be shorted.

Parameter Measurement Information



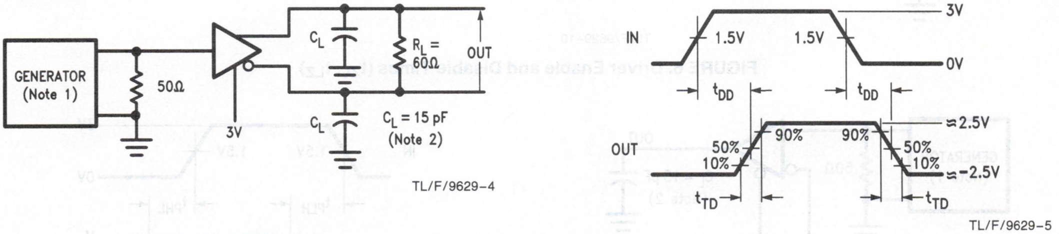
TL/F/9629–2

FIGURE 1. Driver V_{OD} and V_{OC}



TL/F/9629–3

FIGURE 2. Receiver V_{OH} and V_{OL}

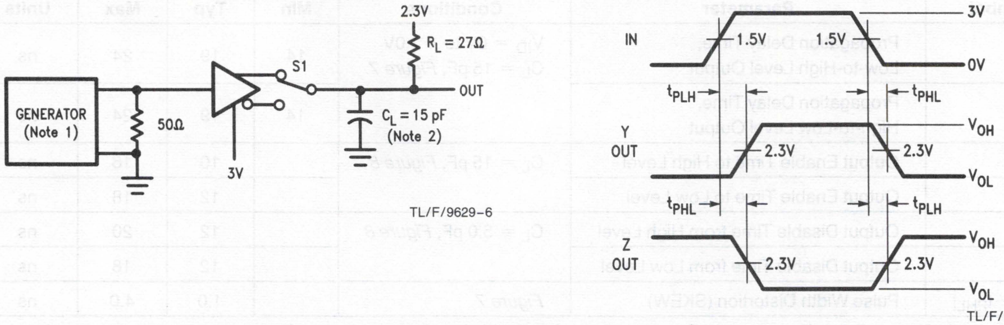


TL/F/9629–4

TL/F/9629–5

FIGURE 3. Driver Differential Output Delay and Transition Times

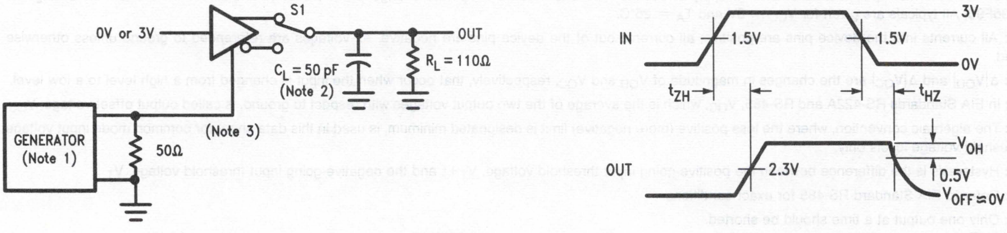
Parameter Measurement Information (Continued)


GENERATOR (Note 1)
50Ω
3V
S1
2.3V
R_L = 27Ω
OUT
C_L = 15 pF (Note 2)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
2.3V
2.3V
V_{OH}
V_{OL}

TL/F/9629-6

TL/F/9629-7

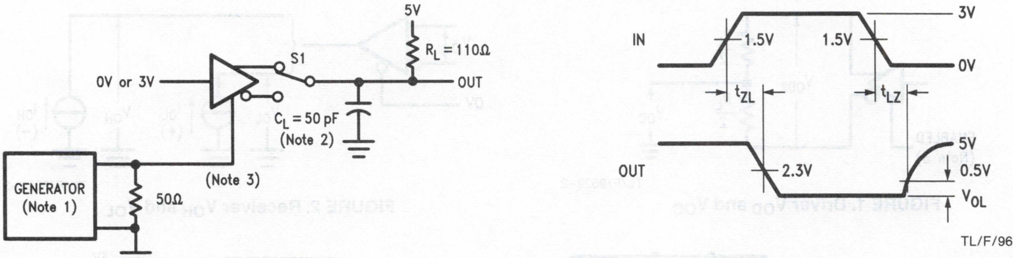
FIGURE 4. Driver Propagation Times


0V or 3V
S1
OUT
C_L = 50 pF (Note 2)
R_L = 110Ω
(Note 3)
GENERATOR (Note 1)
50Ω
IN
1.5V
1.5V
3V
0V
t_{ZH}
t_{HZ}
OUT
2.3V
V_{OH}
0.5V
$V_{OFF} \approx 0V$

TL/F/9629-8

TL/F/9629-9

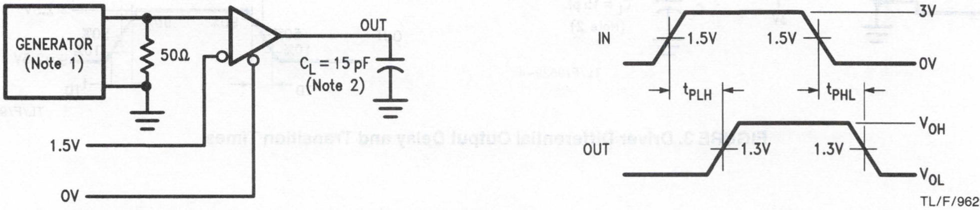
FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ})


5V
R_L = 110Ω
S1
0V or 3V
OUT
C_L = 50 pF (Note 2)
(Note 3)
GENERATOR (Note 1)
50Ω
IN
1.5V
1.5V
3V
0V
t_{ZL}
t_{LZ}
OUT
2.3V
5V
0.5V
V_{OL}

TL/F/9629-10

TL/F/9629-11

FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ})


GENERATOR (Note 1)
50Ω
OUT
C_L = 15 pF (Note 2)
1.5V
0V
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
OUT
1.3V
1.3V
V_{OH}
V_{OL}

TL/F/9629-12

TL/F/9629-13

FIGURE 7. Receiver Propagation Delay Times

Parameter Measurement Information (Continued)

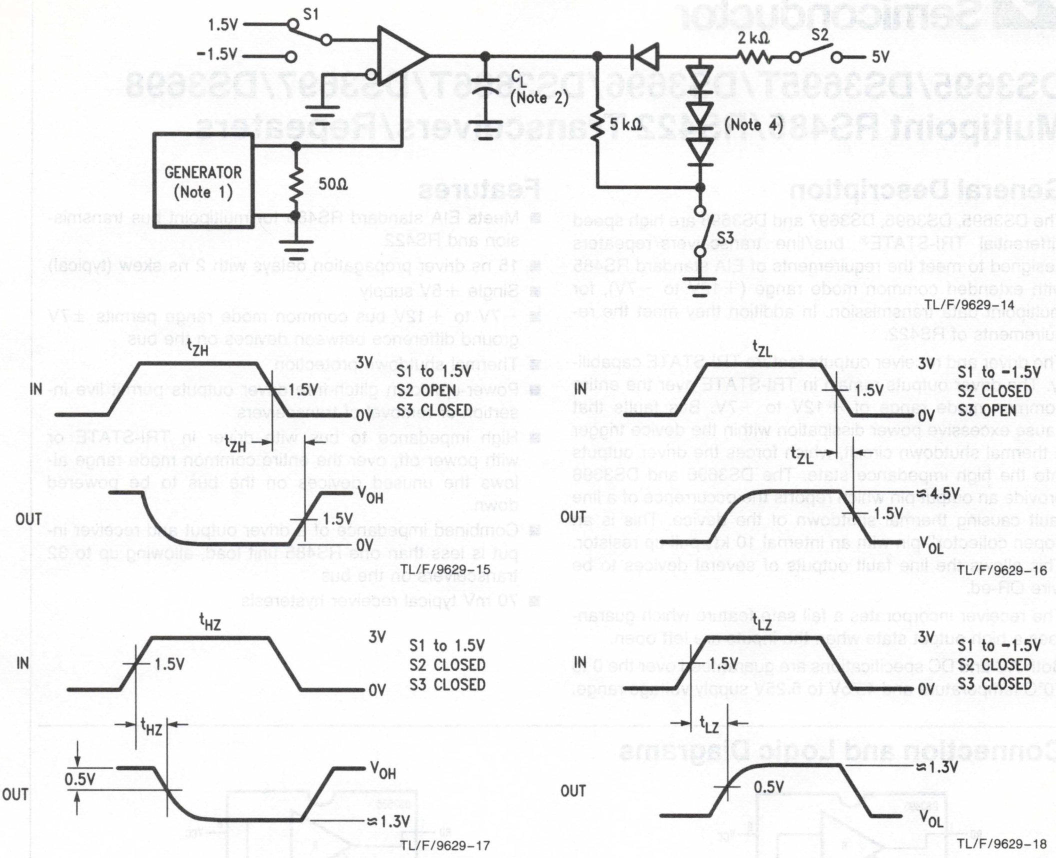

1.5V
S1
−1.5V
C
L
(Note 2)
2 kΩ
S2
5V
5 kΩ
(Note 4)
GENERATOR
(Note 1)
50Ω
S3
TL/F/9629–14
t
ZH
IN
3V
1.5V
0V
S1 to 1.5V
S2 OPEN
S3 CLOSED
t
ZH
OUT
V
OH
1.5V
0V
TL/F/9629–15
t
ZL
IN
3V
1.5V
0V
S1 to −1.5V
S2 CLOSED
S3 OPEN
t
ZL
OUT
≈4.5V
1.5V
V
OL
TL/F/9629–16
t
HZ
IN
1.5V
3V
0V
S1 to 1.5V
S2 CLOSED
S3 CLOSED
t
HZ
OUT
0.5V
V
OH
≈1.3V
TL/F/9629–17
t
LZ
IN
1.5V
3V
0V
S1 to −1.5V
S2 CLOSED
S3 CLOSED
t
LZ
OUT
0.5V
≈1.3V
V
OL
TL/F/9629–18

FIGURE 8. Receiver Enable and Disable Times

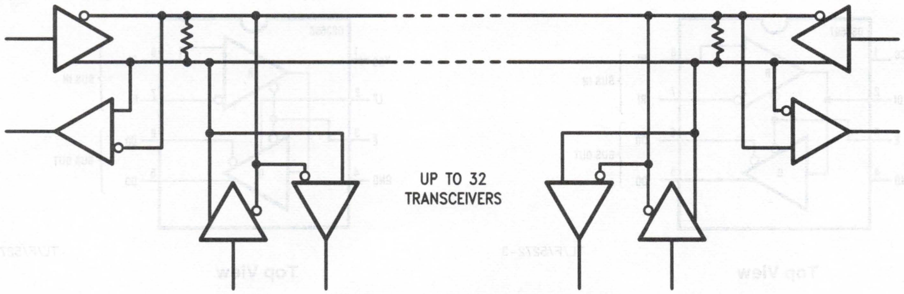
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS16F95/DS36F95 Driver enable is Active-High.

Note 4: All diodes are 1N916 or equivalent.

Typical Application


UP TO 32
TRANSCEIVERS
TL/F/9629–19

Note:

The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS3695/DS3695T/DS3696/DS3696T/DS3697/DS3698 Multipoint RS485/RS422 Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition they meet the requirements of RS422.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin which reports the occurrence of a line fault causing thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

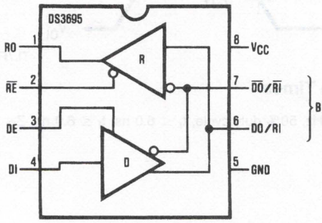
The receiver incorporates a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

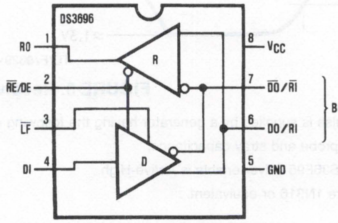
- Meets EIA standard RS485 for multipoint bus transmission and RS422
- 15 ns driver propagation delays with 2 ns skew (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- Power-up/down glitch-free driver outputs permit live insertion or removal of transceivers
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis

Connection and Logic Diagrams



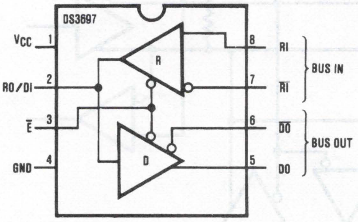
TL/F/5272-1

Top View



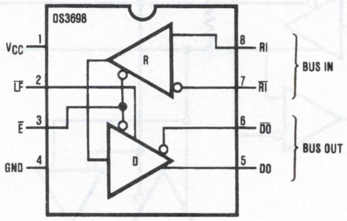
TL/F/5272-2

Top View



TL/F/5272-3

Top View



TL/F/5272-4

Top View

Molded Dual-In-Line Package (N)
Order Number DS3695J, DS3696J, DS3697J, DS3698J, DS3695M, DS3696M, DS3695N, DS3696N, DS3697N, DS3698N, DS3695TN, DS3696TN, DS3695TJ or DS3696TJ
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages (DS3695, DS3696)	+15V/−10V
Receiver Common Mode Voltage (DS3697, DS3698)	±25V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
N Package	1.07W (Note 4)
M Package	630 mW (Note 5)
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. (T_A)			
Commercial	0	+70	°C
Industrial	−40	+85	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 6)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States						0.2	V
V_{OC}	Driver Common Mode Output Voltage		*(Figure 1)*	R = 27Ω			3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$ RI, $\overline{RI}$	$V_{CC} = 0V$ or 5.25V DE/E = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
I_{OZD}	TRI-STATE Current DS3697 & DS3698	DO, $\overline{DO}$	$V_{CC} = 0V$ or 5.25V, E = 0V $-7V < V_0 < +12V$				±100	μA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400\ \mu A$		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 6)				0.5	V
		$\overline{LF}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 6)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified (Notes 2 & 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	V_O = −7V (Note 6)			−250	mA
		V_O = 0V (Note 6)			−150	mA
		V_O = +12V (Note 6)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	V_O = 0V	−15		−85	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: Derate linearly at 11.1 mW/°C to 570 mW at 70°C.

Note 5: Derate linearly at 6.5 mW/°C to 337 mW at 70°C.

Note 6: All limits for which Note 6 is applied must be derated by 10% for DS3695T and DS3696T. Other parameters remain the same for these extended temperature range devices (−40°C ≤ T_A ≤ +85°C).

Receiver Switching Characteristics *(Figures 1, 2* and *3)*

Symbol	Conditions	Min	Typ	Max	Units
t_{PLH}	C_L = 15 pF S1 and S2 Closed	15	25	37	ns
t_{PHL}		15	25	37	ns
$\|t_{PLH}-t_{PHL}\|$		0			ns
t_{PLZ}	C_L = 15 pF, S2 Open	5	12	16	ns
t_{PHZ}	C_L = 15 pF, S1 Open	5	12	16	ns
t_{PZL}	C_L = 15 pF, S2 Open	7	15	20	ns
t_{PZH}	C_L = 15 pF, S1 Open	7	15	20	ns

Driver Switching Characteristics *(Figures 4, 5* and *6)*

Symbol	Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS					
t_{PLH}	$R_{L_{DIFF}}$ = 60Ω C_{L1} = C_{L2} = 100 pF	9	15	22	ns
t_{PHL}		9	15	22	ns
$t_{SKEW}\|t_{PLH}-t_{PHL}\|$		0	2	8	ns
t_{PLZ}	C_L = 15 pF, S2 Open	7	15	30	ns
t_{PHZ}	C_L = 15 pF, S1 Open	7	15	30	ns
t_{PZL}	C_L = 100 pF, S2 Open	30	35	50	ns
t_{PZH}	C_L = 100 pF, S1 Open	30	35	50	ns

Differential Switching Characteristics (Note 7, *Figure 7*)

Symbol	Conditions	Min	Typ	Max	Units
t_r, t_f	$R_{L_{DIFF}}$ = 60Ω C_{L1} = C_{L2} = 100 pF	6	10	18	ns
t_{PLHD}					ns
t_{PHLD}					ns
$\|t_{PLHD}-t_{PHLD}\|$					ns

Note 7: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

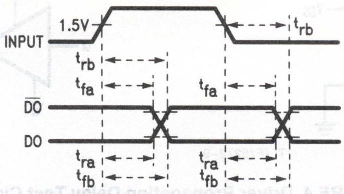
$$Tcr = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

Where: Tcr = Crossing Point

Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

See figure following page.

Switching Time Waveforms


1.5V
INPUT
t_{rb}
t_{fa}
t_{rb}
t_{fa}
$\overline{DO}$
DO
t_{ra}
t_{fb}
t_{ra}
t_{fb}

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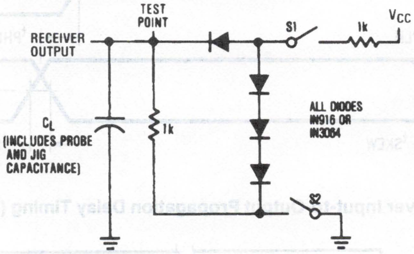
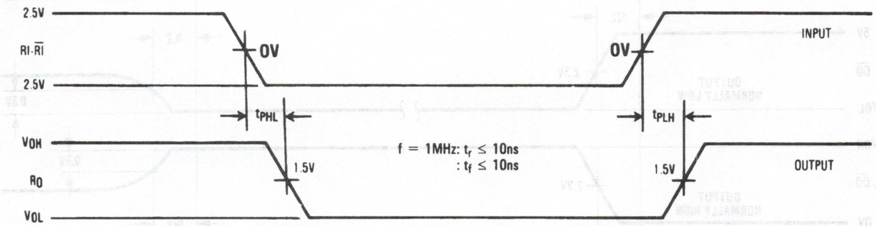
AC Test Circuits and Switching Waveforms


TEST POINT
RECEIVER OUTPUT
S1
1k
V_{CC}
C_L (INCLUDES PROBE AND JIG CAPACITANCE)
1k
ALL DIODES 1N916 OR 1N3064
S2

TL/F/5272-6

FIGURE 1. Receiver Propagation Delay Test Circuit


2.5V
RI-$\overline{RI}$
2.5V
0V
0V
INPUT
t_{PHL}
t_{PLH}
V_{OH}
RO
V_{OL}
f = 1MHz: $t_r \leq 10ns$
: $t_f \leq 10ns$
1.5V
1.5V
OUTPUT

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Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 2. Receiver Input-to-Output Propagation Delay Timing

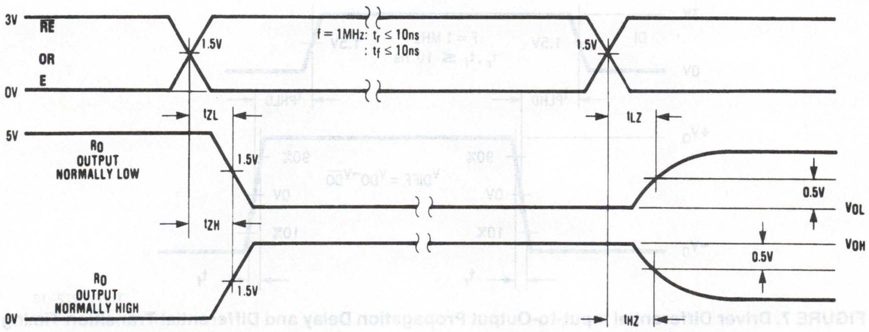
3V
$\overline{RE}$
OR
E
0V
1.5V
f = 1MHz: $t_r \leq 10ns$
: $t_f \leq 10ns$
1.5V
t_{ZL}
t_{LZ}
5V
RO OUTPUT NORMALLY LOW
1.5V
0.5V
V_{OL}
t_{ZH}
V_{OH}
0.5V
RO OUTPUT NORMALLY HIGH
1.5V
0V
t_{HZ}

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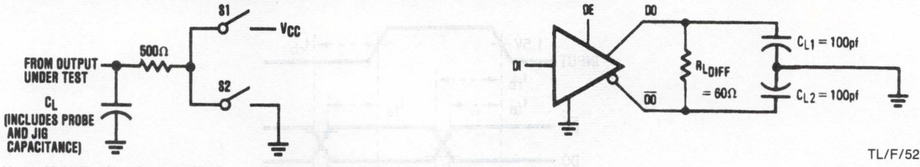
FIGURE 3. Receiver Enable/Disable Propagation Delay Timing

AC Test Circuits and Switching Waveforms (Continued)


S1
VCC
500Ω
FROM OUTPUT UNDER TEST
S2
CL (INCLUDES PROBE AND JIG CAPACITANCE)
DE
DO
DI
DO
RLDIFF = 60Ω
CL1 = 100pf
CL2 = 100pf

Note: Unless otherwise specified the switches are closed.

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TL/F/5272-10

FIGURE 4. Driver Propagation Delay Test Circuits

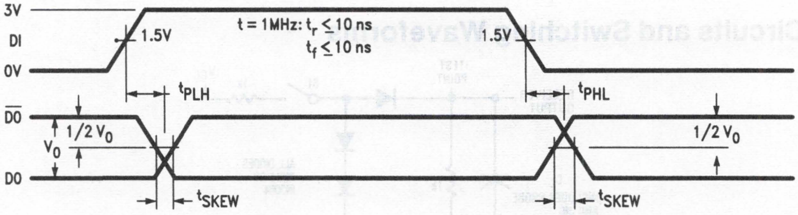
3V
DI
0V
1.5V
t = 1MHz: tr ≤ 10 ns
tf ≤ 10 ns
1.5V
tPLH
tPHL
DO
1/2 VO
VO
DO
tSKEW
1/2 VO
tSKEW

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FIGURE 5. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

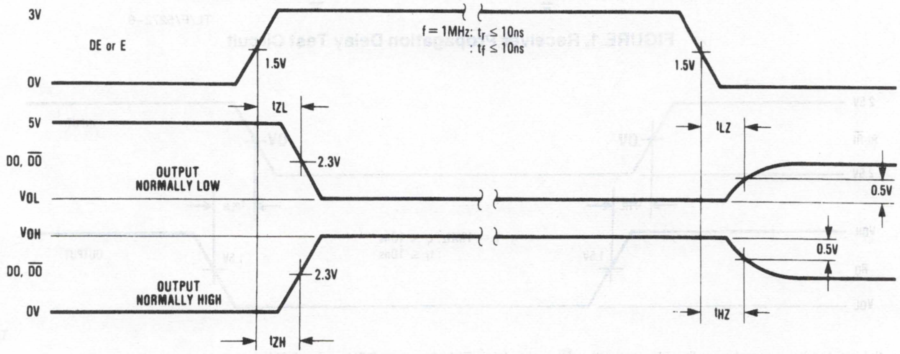
3V
DE or E
0V
f = 1MHz: tr ≤ 10ns
: tf ≤ 10ns
1.5V
1.5V
tZL
tLZ
5V
DO, DO
OUTPUT NORMALLY LOW
2.3V
VOL
0.5V
VOH
DO, DO
OUTPUT NORMALLY HIGH
2.3V
0.5V
0V
tZH
tHZ

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FIGURE 6. Driver Enable/Disable Propagation Delay Timing

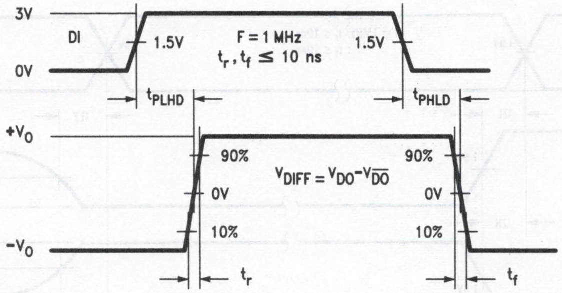
3V
DI
0V
1.5V
F = 1 MHz
tr, tf ≤ 10 ns
1.5V
tPLHD
tPHLD
+VO
90%
90%
VDIFF = VDO−VDO
0V
0V
10%
10%
−VO
tr
tf

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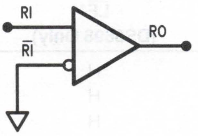
FIGURE 7. Driver Differential Input-to-Output Propagation Delay and Differential Transition Timing

DS3695/DS3696 Channel Distortion (Note 8, *Figures 8, 9*)

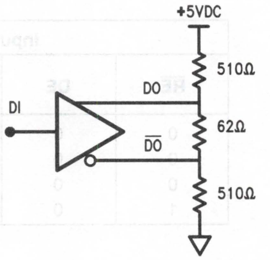
Symbol	Parameter	Conditons	Max	Units
t_{PRR}	The difference of any two input to output propagation delays between any two receivers.	$\Delta T_A \leq 25°C$ $\Delta V_{CC} \leq 200$ mV ($4.75V \leq V_{CC} \leq 5.25V$)	9	ns
t_{PDD}	The difference of any two differential input to output propagation delays between any two drivers.	Measured between any two parts on the same interface channel.	6	ns



RI
$\overline{RI}$
RO

TL/F/5272–14

25 MBS Receiver Propagation Delay Test Circuit



+5VDC
510Ω
DO
DI
62Ω
$\overline{DO}$
510Ω

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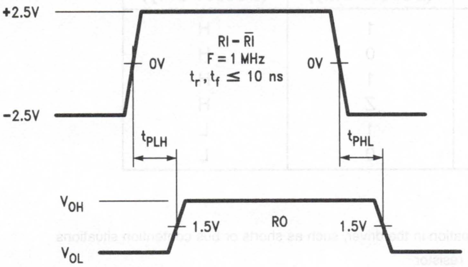
25 MBS Driver Propagation Delay Test Circuit



+2.5V
$RI - \overline{RI}$
F = 1 MHz
$t_r, t_f \leq 10$ ns
OV
OV
−2.5V
t_{PLH}
t_{PHL}
V_{OH}
1.5V
RO
1.5V
V_{OL}

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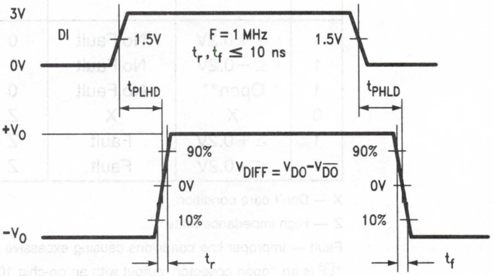
FIGURE 8. 25 MBS Receiver Propagation Delay Timing



3V
DI
1.5V
F = 1 MHz
$t_r, t_f \leq 10$ ns
1.5V
OV
t_{PLHD}
t_{PHLD}
$+V_O$
90%
$V_{DIFF} = V_{DO} - V_{\overline{DO}}$
90%
OV
OV
10%
10%
$-V_O$
t_r
t_f

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FIGURE 9. 25 MBS Driver Propagation Delay Timing

Note 8: Specified to meet the 25 Mbyte Intelligent Peripheral Interface (IPI) requirements.

Function Tables

DS3695/DS3696 Transmitting

Inputs			Line Condition	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{LF}$* (DS3696 Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

DS3695/DS3696 Receiving

Inputs			Outputs	
$\overline{RE}$	DE	RI−$\overline{RI}$	RO	$\overline{LF}$* (DS3696 Only)
0	0	≥ +0.2V	1	H
0	0	≤ −0.2V	0	H
0	0	Inputs Open**	1	H
1	0	X	Z	H

DS3697/DS3698

Inputs		Line Condition	Outputs			
E	RI−$\overline{RI}$		$\overline{DO}$	DO	RO/DI (DS3697 Only)	$\overline{LF}$* (DS3698 Only)
1	≥ +0.2V	No Fault	0	1	1	H
1	≤ −0.2V	No Fault	1	0	0	H
1	Open**	No Fault	0	1	1	H
0	X	X	Z	Z	Z	H
1	≥ +0.2V	Fault	Z	Z	1	L
1	≤ −0.2V	Fault	Z	Z	0	L

X — Don't care condition

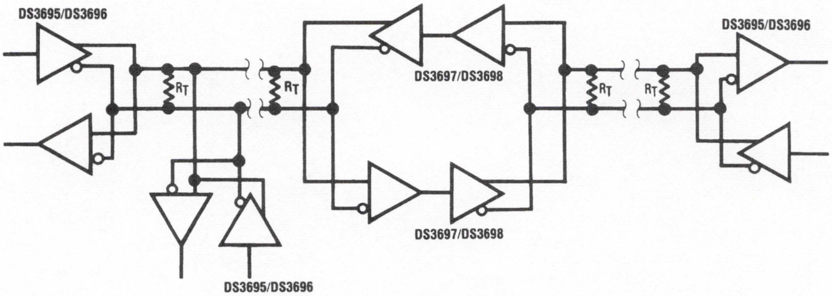
Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

*$\overline{LF}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor

**** This is a fail safe condition**

Typical Application



TL/F/5272–18

National Semiconductor

DS55107/DS55108/DS75107/DS75108/DS75208 Dual Line Receivers

General Description

The products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers of MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the SN55109/SN75109 and μA75110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75208 make it ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators.

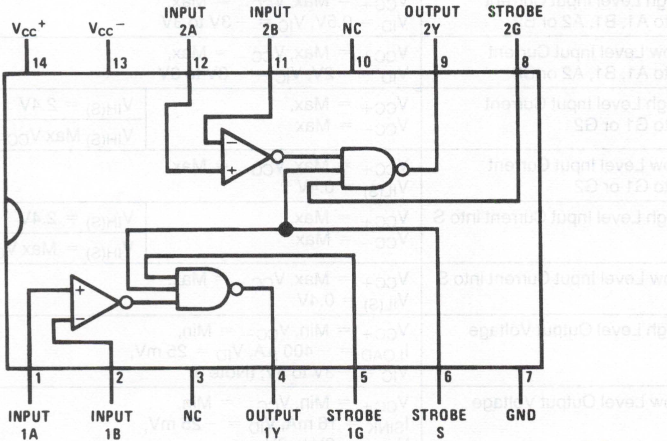
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or $V_{CC} = 0V$
- Strobes for channel selection
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagram

Dual-In-Line Package



TL/F/9446-1

Top View

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75208J, DS75107N, DS75108N or DS75208N
See NS Package Number J14A or N14A

Selection Guide

Temperature → Package →	−55°C ≤ T_A ≤ +125°C Cavity Dip	0°C ≤ T_A ≤ +70°C Cavity or Molded Dip	
Input Sensitivity → Output Logic ↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-Up	DS55107	DS75107	
TTL Open Collector	DS55108	DS75108	DS75208

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, $V_{CC}+$	7V
Supply Voltage, $V_{CC}-$	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS55107, DS55108			DS75107, DS75108, DS75208		
	Min	Nom	Max	Min	Nom	Max
Supply Voltage $V_{CC}+$	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage $V_{CC}-$	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55107 and DS55108 and across the 0°C to +70°C range for the DS75107, DS75108 and DS75208. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

DS55107/DS75107, DS55108/DS75108

Electrical Characteristics $T_{MIN} \le T_A \le T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	µA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	µA
I_{IH}	High Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			40	mA
			$V_{IH(S)}$ Max $V_{CC}+$			1	mA
I_{IL}	Low Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			80	µA
			$V_{IH(S)}$ = Max $V_{CC}+$			2	mA
I_{IL}	Low Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{LOAD} = −400 µA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	$V_{CC}+$ = Min, $V_{CC}-$ = Min V_{OH} = Max $V_{CC}+$, (Note 4)				250	µA
I_{OS}	Short Circuit Output Current	$V_{CC}+$ = Max, $V_{CC}-$ = Max, (Notes 2 and 3)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics $V_{CC+} = 5V$, $V_{CC-} = -5V$, $T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega$, $C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega$, $C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, from Strobe Input G or S to Output	$R_L = 390\Omega$, $C_L = 50$ pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, from Strobe Input G or S to Output	$R_L = 390\Omega$, $C_L = 50$ pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

Note 3: DS55107/DS75107 only.

Note 4: DS55108/DS75108 only.

DS75208

Electrical Characteristics $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{ID} = 0.5V$, $V_{IC} = -3V$ to $3V$			30	75	µA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{ID} = -2V$, $V_{IC} = -3V$ to $3V$				−10	µA
I_{IH}	High Level Input Current into G1 or G2	$V_{CC+} = $ Max, $V_{CC-} = $ Max	$V_{IH(S)} = 2.4V$			40	µA
			$V_{IH(S)} = $ Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current into G1 or G2	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{IL(S)} = 0.4V$				−1.6	mA
I_{IH}	High Level Input Current into S	$V_{CC+} = $ Max, $V_{CC-} = $ Max	$V_{IH(S)} = 2.4V$			80	µA
			$V_{IH(S)} = $ Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current into S	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{IL(S)} = 0.4V$				−3.2	mA
V_{OL}	Low Level Output Voltage	$V_{CC+} = $ Min, $V_{CC-} = $ Min, $I_{SINK} = 16$ mA, $V_{ID} = -10$ mV, $V_{IC} = -3V$ to $3V$				0.4	V
I_{OH}	High Level Output Current	$V_{CC+} = $ Min, $V_{CC-} = $ Min, $V_{OH} = $ Max V_{CC+}				250	µA
I_{CCH+}	High Logic Level Supply Current from V_{CC+}	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{ID} = 10$ mV, $T_A = 25°C$			18	30	mA
I_{CCH-}	High Logic Level Supply Current from V_{CC-}	$V_{CC+} = $ Max, $V_{CC-} = $ Max, $V_{ID} = 10$ mV, $T_A = 25°C$			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	$V_{CC+} = $ Min, $V_{CC-} = $ Min, $I_{IN} = -12$ mA, $T_A = 25°C$			−1	−1.5	V

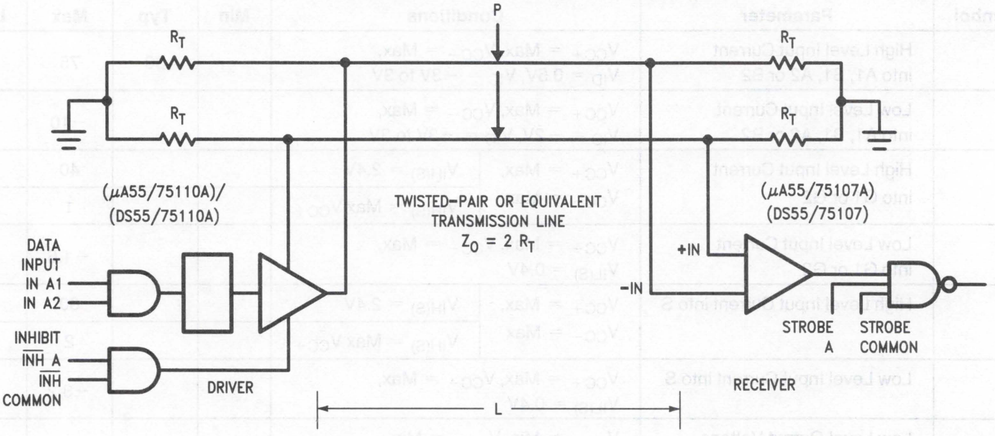
Switching Characteristics $V_{CC+} = 5V, V_{CC-} = -5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 470\Omega, C_L = 15$ pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 470\Omega, C_L = 15$ pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G or S to Output	$R_L = 470\Omega, C_L = 15$ pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G or S to Output	$R_L = 470\Omega, C_L = 15$ pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Typical Applications

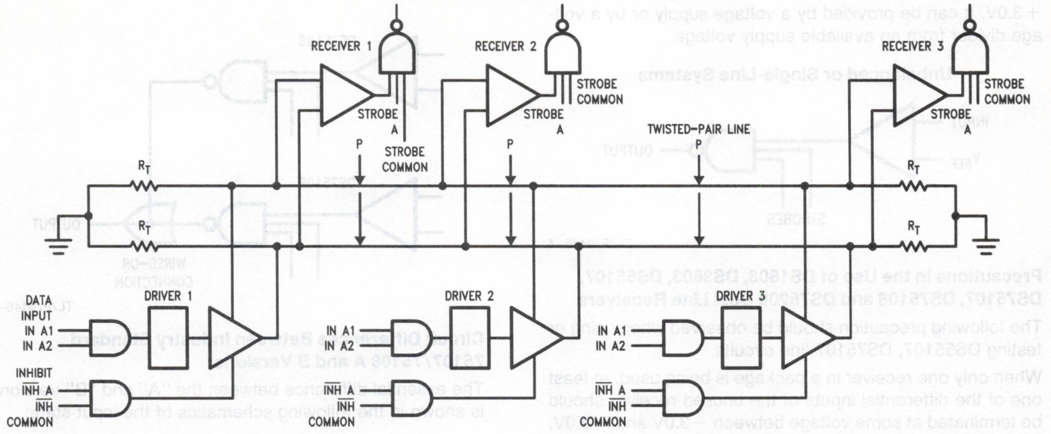
Basic Balanced-Line Transmission System


P
R_T
R_T
R_T
R_T
(μA55/75110A)/
(DS55/75110A)
TWISTED-PAIR OR EQUIVALENT
TRANSMISSION LINE
$Z_0 = 2\ R_T$
(μA55/75107A)
(DS55/75107)
DATA
INPUT
IN A1
IN A2
INHIBIT
$\overline{INH}$ A
$\overline{INH}$
COMMON
DRIVER
+IN
−IN
STROBE
A
STROBE
COMMON
RECEIVER
L

TL/F/9446–2

Typical Applications (Continued)

Data-Bus or Party-Line System



TL/F/9446-3

APPLICATION

The DS55107, DS75107 dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver input logic levels. The voltage difference is approximately:

$$V_{DIFF} \cong \tfrac{1}{2} I_{O(on)} \times R_T \qquad (1)$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \cong I_{O(on)} \times R_T \qquad (2)$$

The strobe feature of the receivers and the inhibit feature of the drivers allow the DS55107, DS75107 dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The DS55107, DS75107 device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

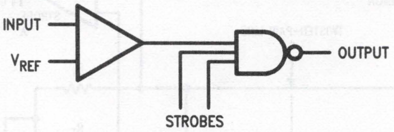
The DS55107, DS75107 dual line circuits may also be used in unbalanced or single line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

The receiver threshold level is established by applying a DC reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal

Typical Applications (Continued)

swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0V to +3.0V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



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Precautions in the Use of DS1603, DS3603, DS55107, DS75107, DS75108 and DS75208 Dual Line Receivers

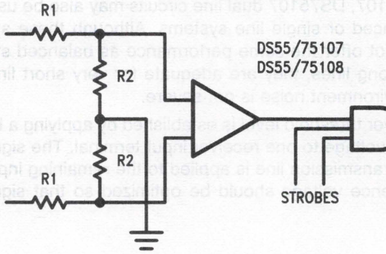
The following precaution should be observed when using or testing DS55107, DS75107 line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0V and +3.0V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

The DS55107, DS75107 and DS75108 line receivers feature a common mode input voltage range of ±3.0V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common mode range can be extended by the use of external input attenuators. Common mode input voltages can in this way be reduced to ±3.0V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

The DS75108 line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other DS75108 outputs. This allows a level of logic to be implemented without addtional logic delay.

Increasing Common Mode Input Voltage Range of Receiver



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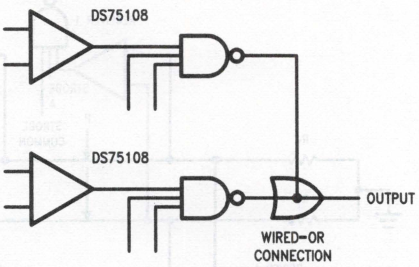
DS75108 Wired-OR Output Connections



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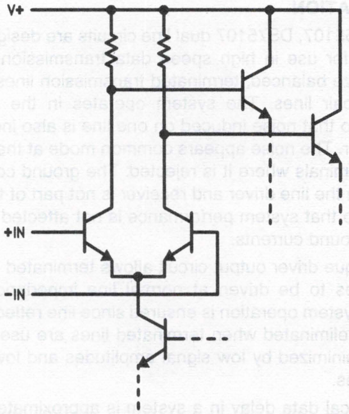
Circuit Differences Between Industry Standard 75107/75108 A and B Versions

The essential difference between the "A" and "B" versions is shown in the following schematics of the input state:

A Version



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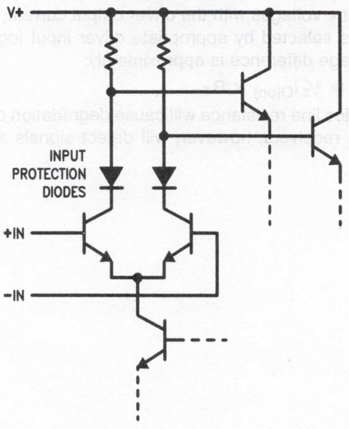
B Version



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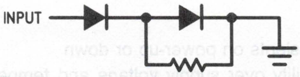
Typical Applications (Continued)

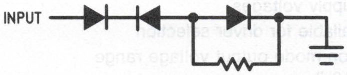
The input protection diodes are useful in certain party-line systems which may have multiple V+ power supplies and, in which case, may be operated with some of the V+ supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

A Version



TL/F/9446-9

B Version



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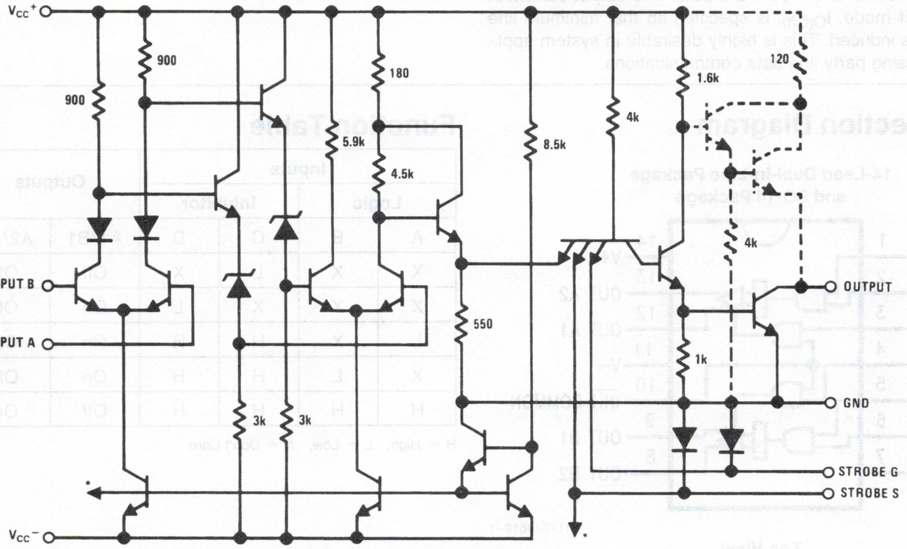
This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions.

The DS75107/DS75108/DS75208 feature the protective diodes shown in the B version below. The μA55107A/DS55107A feature the A version input stage.

Schematic Diagrams

DS55107/DS75107, DS55108/DS75108, DS75208



TL/F/9446-11

Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

Note 3: Components shown with dash lines are applicable to the DS55107, DS75207 and DS75107 only.

National Semiconductor

DS55110A/μA55110A/DS75110A/μA75110A Dual Line Drivers

General Description

The DS55110A/μA55110A, DS75110A/μA75110A are dual line drivers with independent channels, common supply and ground terminals featuring constant current outputs. These drivers are designed for optimum performance when used with the DS55107/DS75107, DS55108/DS75108 line receivers.

The output current of the DS55110A/μA55110A, DS75110A/μA75110A is nominally 12 mA and may be switched to either of two output terminals with the appropriate logic levels at the driver input.

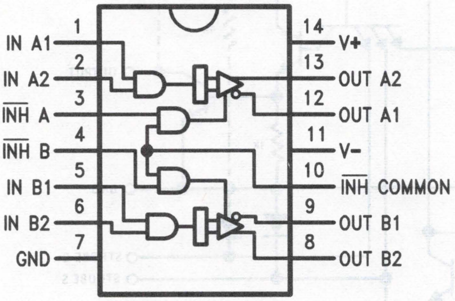
Separate or common control inputs are provided for increased logic versatility. These control or inhibit inputs allow the output current to be switched off (inhibited) by applying low logic levels to the control inputs. The output current in the inhibit mode, $I_{O(Off)}$, is specified so that minimum line loading is induced. This is highly desirable in system applications using party line data communications.

Features

- No output transients on power-up or down
- Improved stability over supply voltage and temperature ranges
- Constant current, high impedance outputs
- High speed 15 ns
- Standard supply voltages
- Inhibitor available for driver selection
- High common mode output voltage range (−3.0V to 10V)
- TTL input compatibility
- Extended temperature range

Connection Diagram

14-Lead Dual-In-Line Package and SO-14 Package



TL/F/9619–1

Top View

Order Number DS55110AJ, DS75110AJ, μA55110ADM, μA75110ADC
See NS Package Number J14A*

Order Number DS75110AM or μA75110ASC
See NS Package Number M14A

Order Number DS75110AN or μA75110APC
See NS Package Number N14A

Function Table

Inputs				Outputs	
Logic		Inhibitor			
A	B	C	D	A1/B1	A2/B2
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	On	Off
X	L	H	H	On	Off
H	H	H	H	Off	On

H = High, L = Low, X = Don't Care

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*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-14 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1360 mW
Molded Package	1040 mW
SO Package	930 mW

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.5 mW/°C above 25°C.

Suppy Voltage	±7.0V
Input Voltage (Any Input)	5.5V
Output Voltage (Any Output)	−5.0V to +12V

Recommended Operating Conditions

	DS55110A/μA55110A			DS75110A/μA75110A			Units
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V^+)	4.5	5.0	5.5	4.75	5.0	5.25	V
Negative Supply Voltage (V^-)	−4.5	−5.0	−5.5	−4.75	−5.0	−5.25	V
Positive Common Mode Voltage ($V_{CM}{}^+$)	0		10	0		10	V
Negative Common Mode Voltage ($V_{CM}{}^-$)	0		−3.0	0		−3.0	V
Operating Temperature (T_A)	−55	25	125	0	25	70	°C

Electrical Characteristics

Over recommended operating temperature range, unless otherwise specified. (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA		−0.9	−1.5	V
$I_{O(On)}$	On-State Output Current		V_{CC} = Max, V_O = 10V		12	15	mA
			V_{CC} = Min, V_O = −3.0V	6.5	12		
$I_{O(Off)}$	Off-State Output Current		V_{CC} = Min, V_O = 10V			100	μA
I_I	Input Current At Maximum Input Voltage	A, B or C Inputs	V_{CC} = Max, V_I = 5.5V			1.0	mA
		D Input				2.0	
I_{IH}	Input Current HIGH	A, B or C Input	V_{CC} = Max, V_I = 2.4V			40	μA
		D Input				80	
I_{IL}	Input Current LOW	A, B or C Input	V_{CC} = Max, V_I = 0.4V			−3.0	mA
		D Input				−6.0	
$I_{+(On)}$	Positive Supply Current with Driver Enabled		V_{CC} = Max, A & B Inputs at 0.4V, C & D Inputs at 2.0V		23	35	mA
$I_{-(On)}$	Negative Supply Current with Driver Enabled				−34	−50	mA
$I_{+(Off)}$	Positive Supply Current with Driver Inhibited		V_{CC} = Max, A, B, C & D Inputs at 0.4V		21		mA
$I_{-(Off)}$	Negative Supply Current with Driver Inhibited				−17		mA

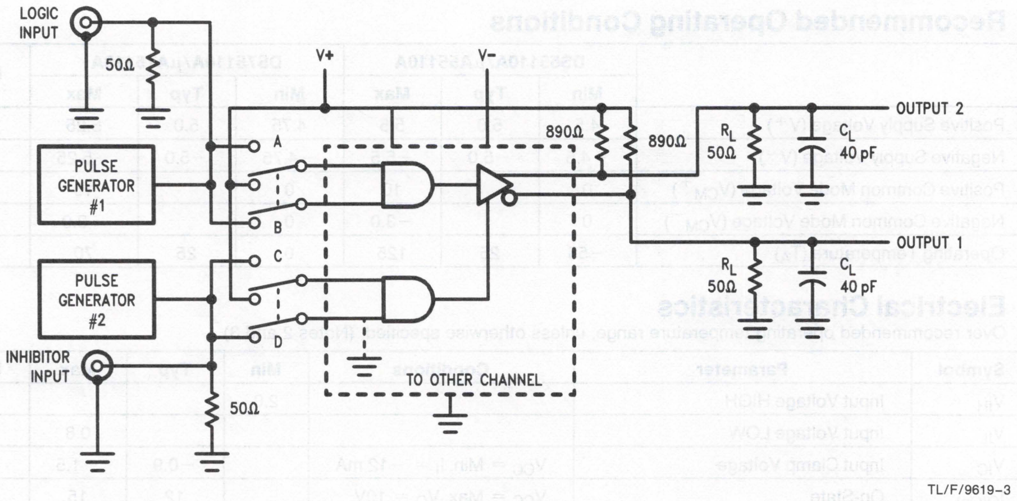
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55110 and across the 0°C to +70°C range for the DS75110. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

Switching Characteristics $V_{CC} = \pm 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, LOW to HIGH	$C_L = 40$ pF, $R_L = 50\Omega$ See Test Circuit	A or B	1 or 2		9.0	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9.0	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH		C or D	1 or 2		16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns


LOGIC INPUT
50Ω
V+
V−
A
B
C
D
PULSE GENERATOR #1
PULSE GENERATOR #2
INHIBITOR INPUT
50Ω
890Ω
890Ω
TO OTHER CHANNEL
OUTPUT 2
OUTPUT 1
R_L 50Ω
C_L 40 pF
R_L 50Ω
C_L 40 pF
TL/F/9619-3

Note 1: The pulse generators have the following characteristics:
$t_r = t_f = 10$ ns ±5.0 ns, $t_{w1} = 500$ ns, PRR = 1.0 MHz, $t_{W2} = 1.0$ μs, PRR = 500 kHz, $Z_O = 50\Omega$.

Note 2: C_L includes probe and jib capacitance.

Note 3: For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 2. AC Test Circuit

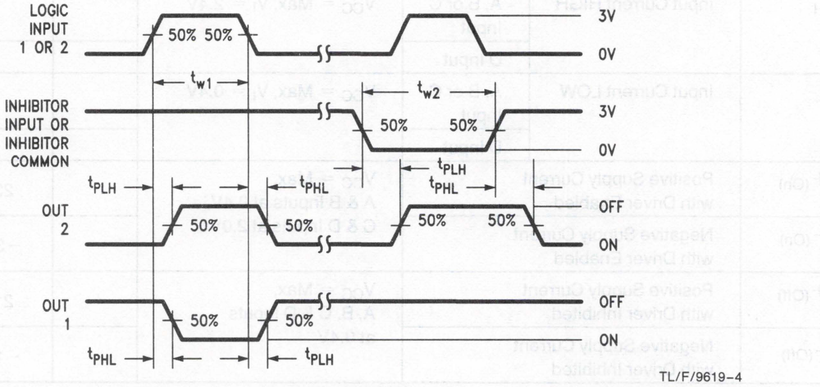
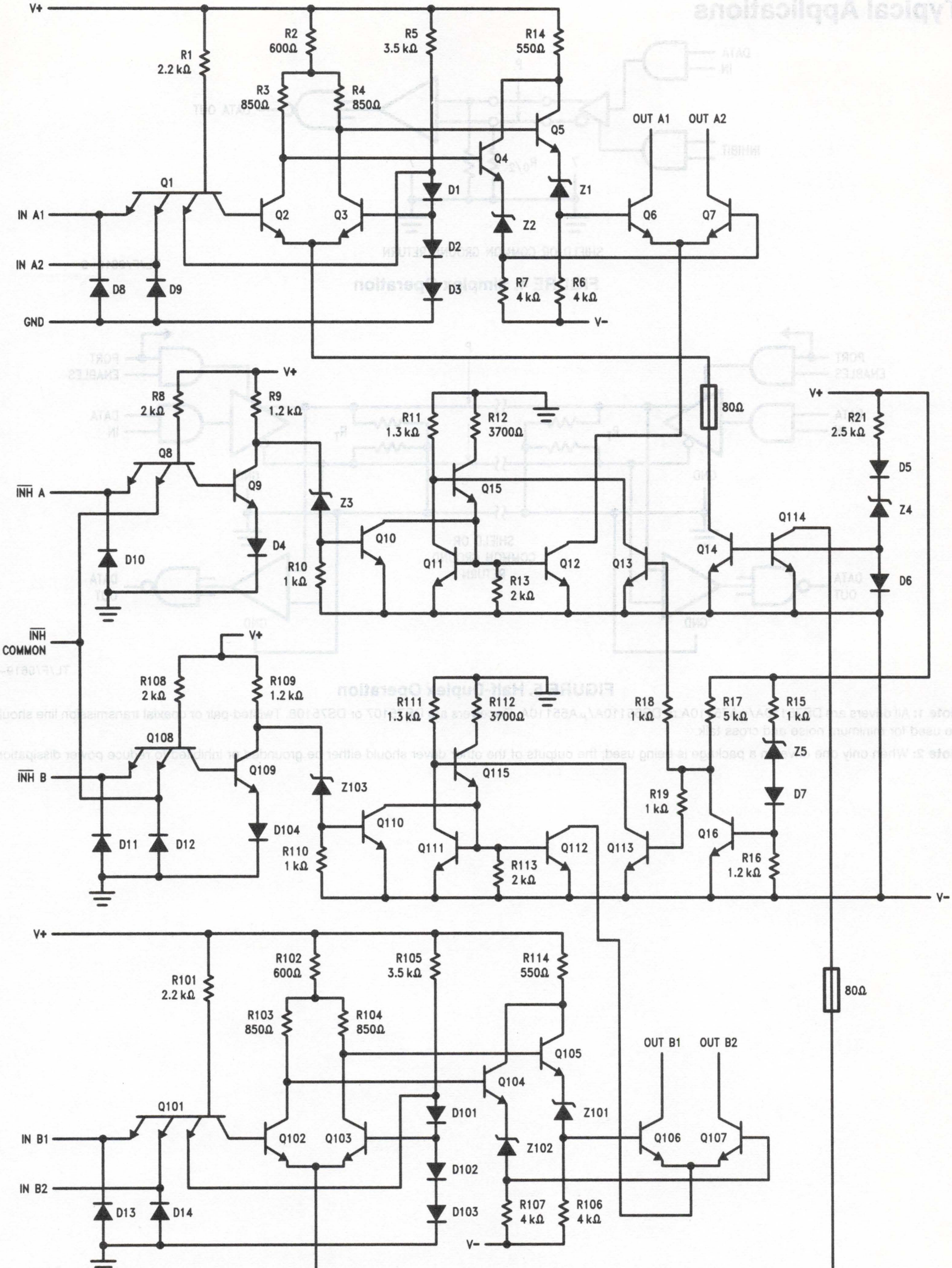

LOGIC INPUT 1 OR 2
50% 50%
3V
0V
t_{w1}
t_{w2}
INHIBITOR INPUT OR INHIBITOR COMMON
50% 50%
3V
0V
t_{PLH}
t_{PHL}
t_{PLH}
t_{PHL}
OUT 2
50% 50% 50% 50%
OFF
ON
OUT 1
50% 50%
OFF
ON
t_{PHL}
t_{PLH}
TL/F/9619-4

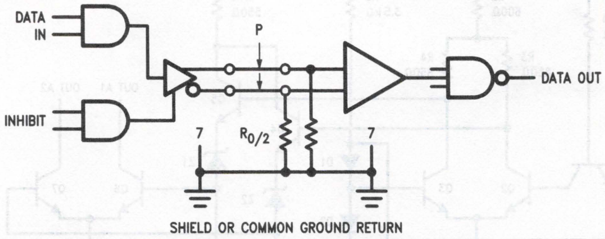
FIGURE 3. AC Waveforms


V+
R1
2.2 kΩ
R2
600Ω
R3
850Ω
R4
850Ω
R5
3.5 kΩ
R14
550Ω
Q5
Q4
OUT A1
OUT A2
Q1
D1
Z1
IN A1
Q2
Q3
Z2
Q6
Q7
D2
IN A2
D8
D9
D3
R7
4 kΩ
R6
4 kΩ
GND
V−
V+
R8
2 kΩ
R9
1.2 kΩ
R11
1.3 kΩ
R12
3700Ω
80Ω
V+
R21
2.5 kΩ
Q8
D5
INH A
Q9
Q15
Z4
Z3
Q114
D10
Q10
D4
Q11
Q12
Q13
Q14
R10
1 kΩ
R13
2 kΩ
D6
INH COMMON
V+
R108
2 kΩ
R109
1.2 kΩ
R111
1.3 kΩ
R112
3700Ω
R18
1 kΩ
R17
5 kΩ
R15
1 kΩ
Q108
Z5
INH B
Q109
Q115
Z103
D7
R19
1 kΩ
D104
Q110
Q16
D11
D12
Q111
Q112
Q113
R110
1 kΩ
R16
1.2 kΩ
R113
2 kΩ
V−
V+
R101
2.2 kΩ
R102
600Ω
R105
3.5 kΩ
R114
550Ω
80Ω
R103
850Ω
R104
850Ω
Q105
OUT B1
OUT B2
Q104
Q101
D101
Z101
IN B1
Q102
Q103
Z102
Q106
Q107
D102
IN B2
D13
D14
D103
R107
4 kΩ
R106
4 kΩ
V−
= CROSSUNDER

TL/F/9619-2

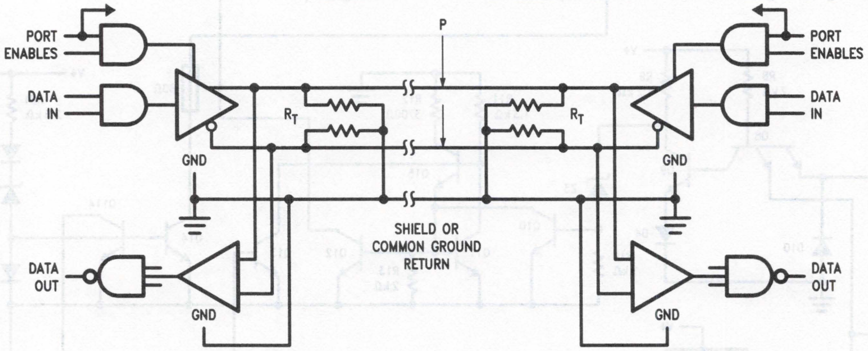
FIGURE 1. Equivalent Circuit

Typical Applications


DATA
IN
INHIBIT
P
7
$R_{0/2}$
7
DATA OUT
SHIELD OR COMMON GROUND RETURN

TL/F/9619-5

FIGURE 4. Simplex Operation


PORT
ENABLES
DATA
IN
GND
DATA
OUT
GND
P
R_T
R_T
SHIELD OR
COMMON GROUND
RETURN
PORT
ENABLES
DATA
IN
GND
DATA
OUT
GND

TL/F/9619-6

FIGURE 5. Half-Duplex Operation

Note 1: All drivers are DS75110A/μA75110A or DS55110A/μA55110A. Receivers are DS75107 or DS75108. Twisted-pair or coaxial transmission line should be used for minimum noise and cross talk.

Note 2: When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

National Semiconductor

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

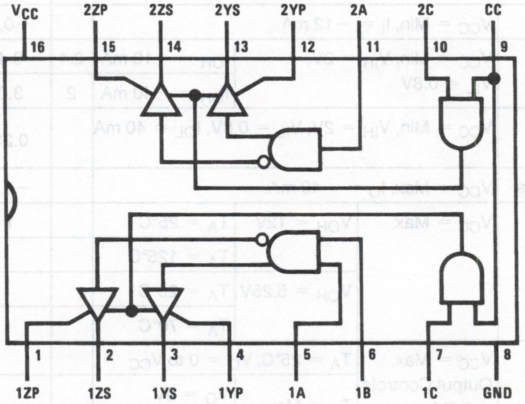
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = AB$
$Z = \overline{AB}$

Output is OFF when
C or CC is low

TL/F/5785–1

Top View

Order Number DS55113J, DS75113J, DS75113M or DS75113N
See NS Package Number J16A, M16A or N16A

Truth Table

Inputs				Outputs	
Output Control		Data		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H*
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 1)	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Operating Free-Air Temperature Range	
DS55113	−55°C to +125°C
DS75113	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16″ from case for 60 seconds): J Package	300 °C
Lead Temperature (1/16″ from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions (Note 3)			DS55113			DS75113			Units
						Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA		2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage		V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-State Open-Collector Output Current		V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				µA
					T_A = 125°C			200				
				V_{OH} = 5.25V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-State (High-Impedance-State) Output Current		V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	µA
				T_A = Max	V_O = 0V			−150			−20	
					V_O = 0.4V			±80			±20	
					V_O = 2.4V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V					1			1	mA
		CC						2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V					40			40	µA
		CC						80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V					−1.6			−1.6	mA
		CC						−3.2			−3.2	

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions (Note 3)		DS55113			DS75113			Units
				Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, $V_O = 0V$		−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	All Inputs at 0V, No Load $T_A = 25°C$	V_{CC} = Max		47	65		47	65	mA
			$V_{CC} = 7V$		65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

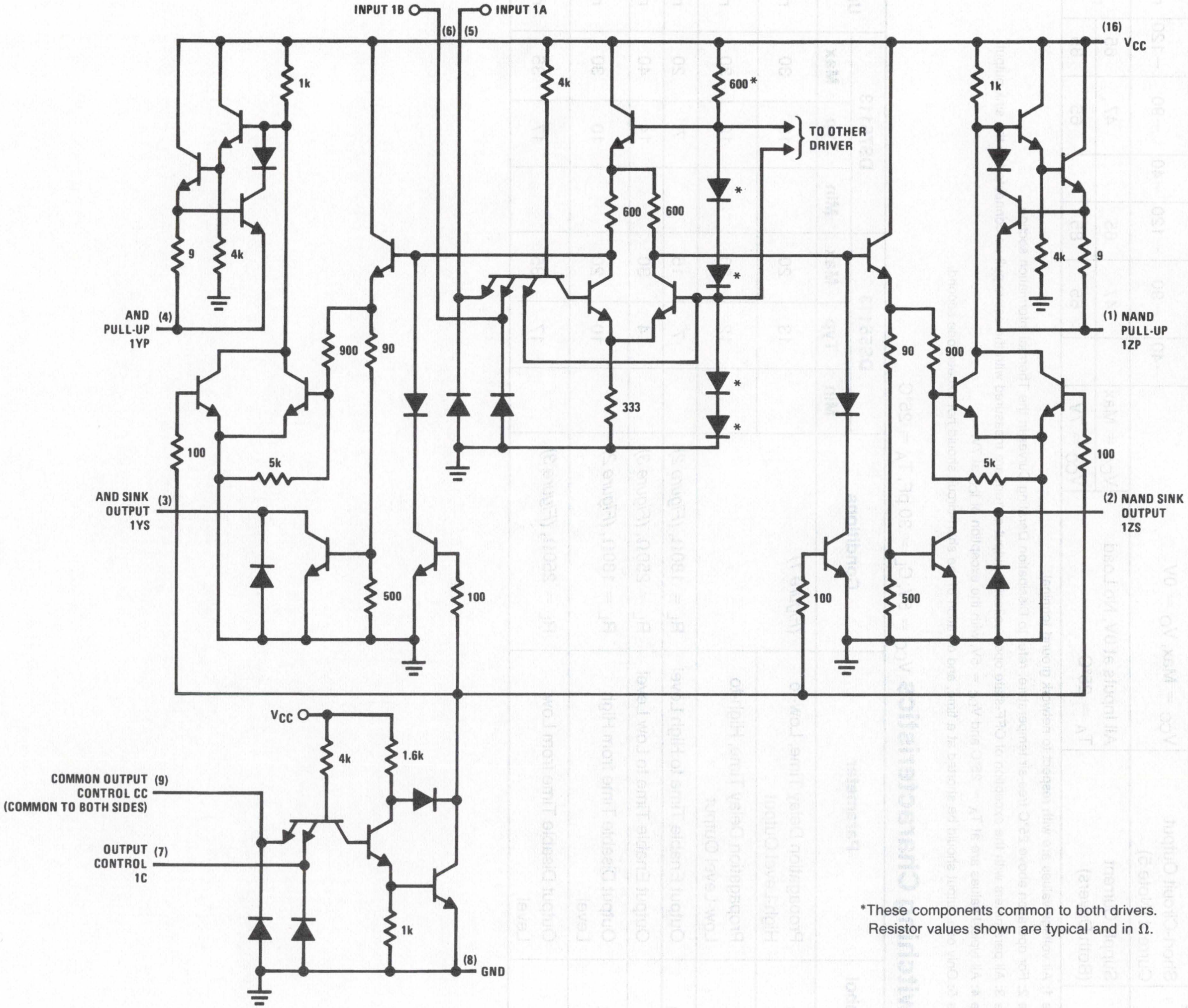
Note 4: All typical values are at $T_A = 25°C$ and $V_{CC} = 5V$, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $C_L = 30\ pF$, $T_A = 25°C$

Symbol	Parameter	Conditions	DS55113			DS75113			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 180\Omega$, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 250\Omega$, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 180\Omega$, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 250\Omega$, *(Figure 3)*		17	35		17	35	ns

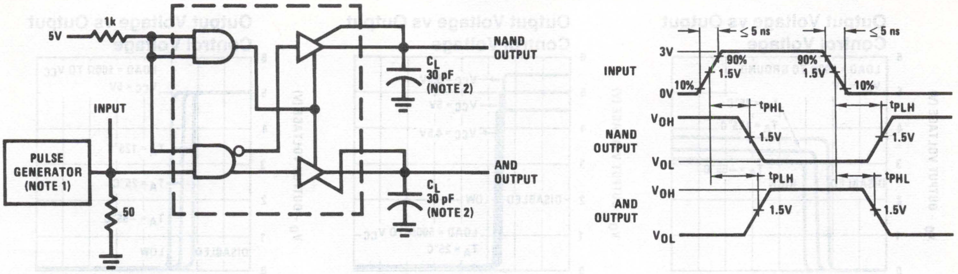
Schematic Diagram (One side shown only)


INPUT 1B
INPUT 1A
(6)
(5)
(16)
VCC
1k
4k
600*
TO OTHER DRIVER
*
600
600
*
333
*
*
1k
9
4k
4k
9
AND PULL-UP 1YP (4)
(1) NAND PULL-UP 1ZP
900
90
90
900
100
5k
5k
100
AND SINK OUTPUT 1YS (3)
(2) NAND SINK OUTPUT 1ZS
500
100
100
500
VCC
4k
1.6k
COMMON OUTPUT CONTROL CC (COMMON TO BOTH SIDES) (9)
OUTPUT CONTROL 1C (7)
1k
(8) GND

*These components common to both drivers.
Resistor values shown are typical and in Ω.

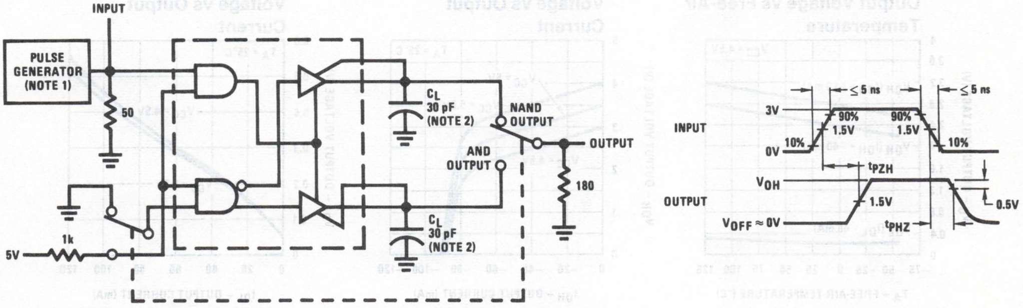
TL/F/5785–2

AC Test Circuits and Switching Time Waveforms


5V
1k
INPUT
PULSE GENERATOR (NOTE 1)
50
NAND OUTPUT
C_L 30 pF (NOTE 2)
AND OUTPUT
C_L 30 pF (NOTE 2)
≤ 5 ns
≤ 5 ns
3V
90%
1.5V
90%
1.5V
INPUT
0V
10%
10%
V_{OH}
t_{PHL}
t_{PLH}
NAND OUTPUT
1.5V
1.5V
V_{OL}
V_{OH}
t_{PLH}
t_{PHL}
AND OUTPUT
1.5V
1.5V
V_{OL}

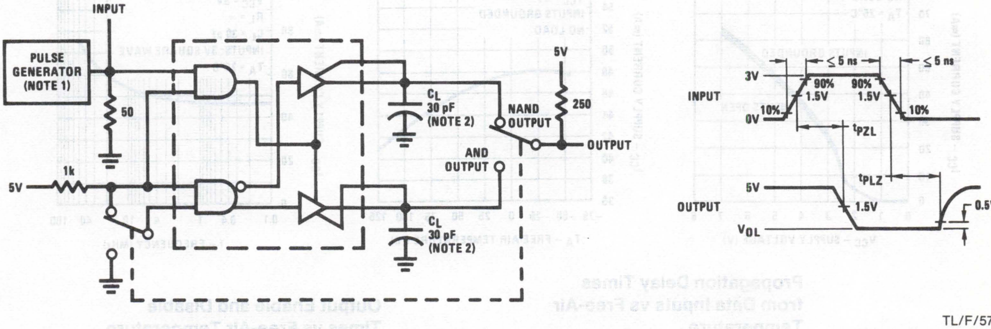
TL/F/5785-3

FIGURE 1. t_{PLH} and t_{PHL}


INPUT
PULSE GENERATOR (NOTE 1)
50
5V
1k
C_L 30 pF (NOTE 2)
NAND OUTPUT
AND OUTPUT
OUTPUT
180
C_L 30 pF (NOTE 2)
≤ 5 ns
≤ 5 ns
3V
90%
1.5V
90%
1.5V
INPUT
0V
10%
10%
t_{PZH}
V_{OH}
OUTPUT
1.5V
V_{OFF} ≈ 0V
t_{PHZ}
0.5V

TL/F/5785-4

FIGURE 2. t_{PZH} and t_{PHZ}


INPUT
PULSE GENERATOR (NOTE 1)
50
5V
1k
C_L 30 pF (NOTE 2)
5V
250
NAND OUTPUT
OUTPUT
AND OUTPUT
C_L 30 pF (NOTE 2)
≤ 5 ns
≤ 5 ns
3V
90%
1.5V
90%
1.5V
INPUT
0V
10%
10%
t_{PZL}
t_{PLZ}
5V
OUTPUT
1.5V
0.5V
V_{OL}

TL/F/5785-5

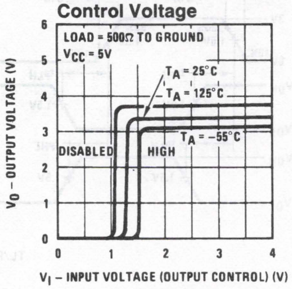
FIGURE 3. t_{PZL} and t_{PLZ}

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz, $t_W = 100$ ns.

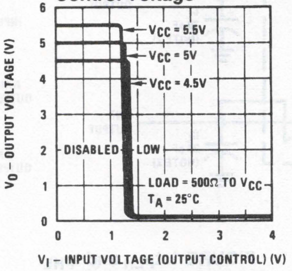
Note 2: C_L includes probe and jig capacitance.

Typical Performance Characteristics*

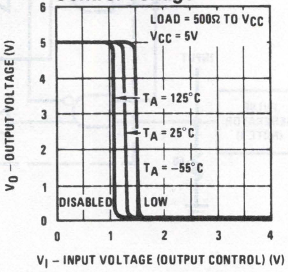
Output Voltage vs Output Control Voltage



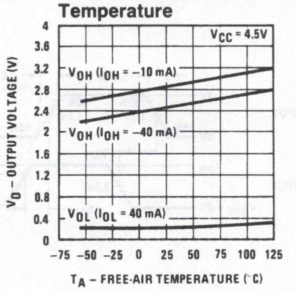
Output Voltage vs Output Control Voltage



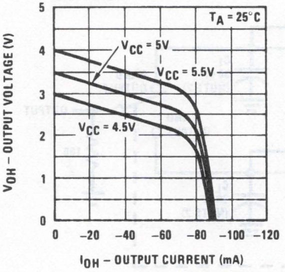
Output Voltage vs Output Control Voltage



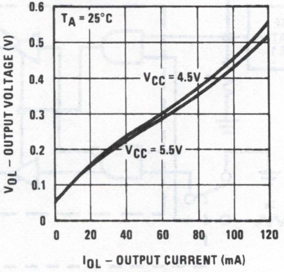
Output Voltage vs Free-Air Temperature



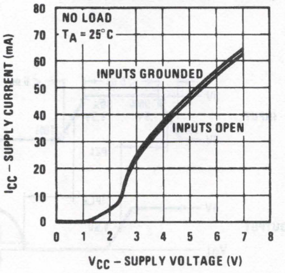
High Level Output Voltage vs Output Current



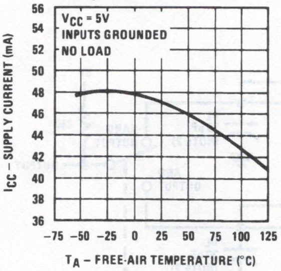
Low Level Output Voltage vs Output Current



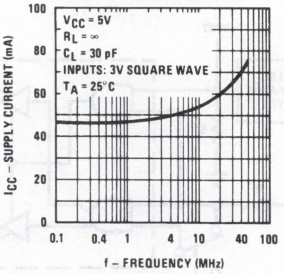
Supply Current (Both Drivers) vs Supply Voltage



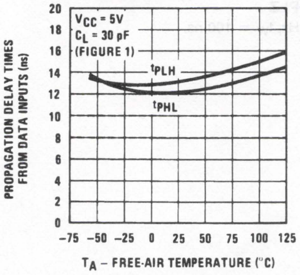
Supply Current (Both Drivers) vs Free-Air Temperature



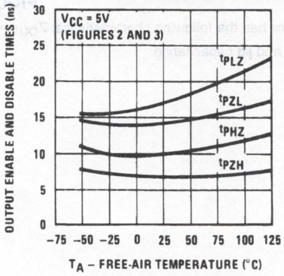
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



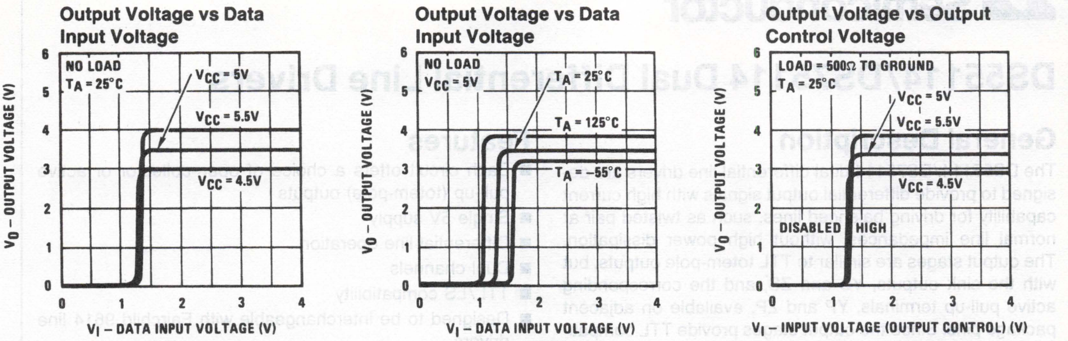
Output Enable and Disable Times vs Free-Air Temperature



TL/F/5785–7

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)



TL/F/5785-6

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

DS55114/DS75114 Dual Differential Line Drivers

General Description

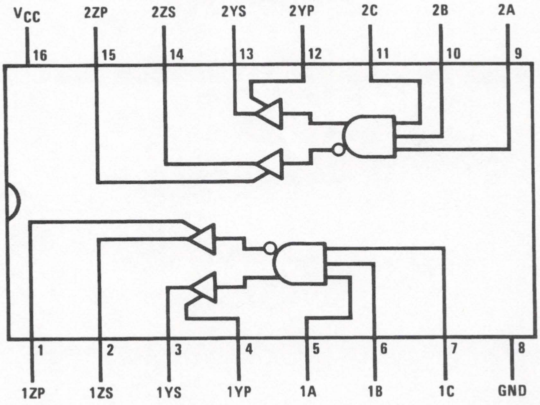
The DS55114/DS75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- Designed to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



TL/F/5786-1

Top View

Positive logic: $Y = ABC$

$Z = \overline{ABC}$

Order Number DS55114J, DS75114J, or DS75114N
See NS Package Number J16A or N16A

Truth Table

Inputs			Outputs	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level

L = low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16″ from case for 60 seconds): J Package	300°C
Lead Temperature (1/16″ from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55114	4.5	5.5	V
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55114	−55	125	°C
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)			DS55114			DS75114			Units
					Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5		6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V			−40	−90	120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C		V_{CC} = Max		37	50		37	50	mA
				V_{CC} = 7V		47	65		47	70	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

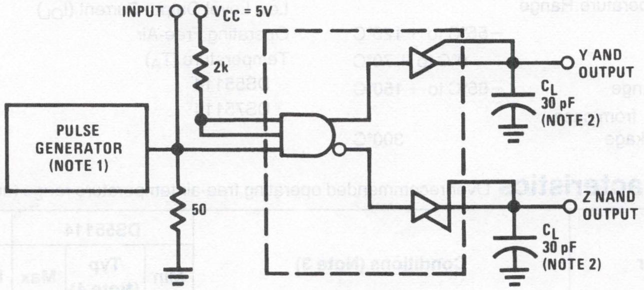
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	DS55114			DS75114			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$C_L = 30$ pF, *(Figure 1)*		15	20		15	30	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Output			11	20		11	30	ns

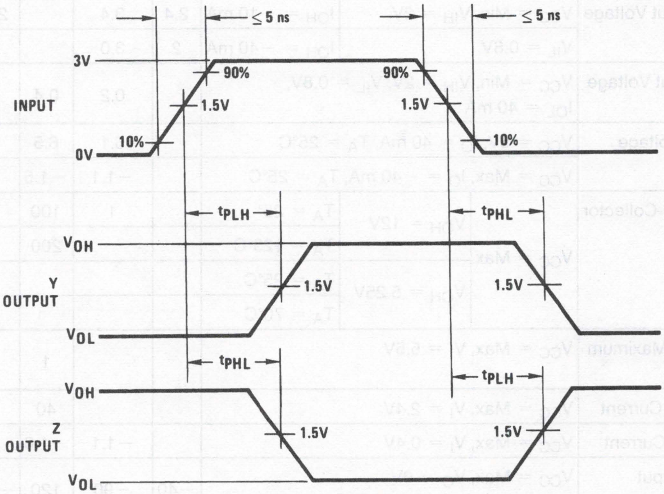
AC Test Circuit and Switching Time Waveforms


INPUT
V_{CC} = 5V
2k
PULSE GENERATOR (NOTE 1)
50
Y AND OUTPUT
C_L 30 pF (NOTE 2)
Z NAND OUTPUT
C_L 30 pF (NOTE 2)

TL/F/5786-3

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_w = 100$ ns, PRR = 500 kHz.

Note 2: C_L includes probe and jig-capacitance.

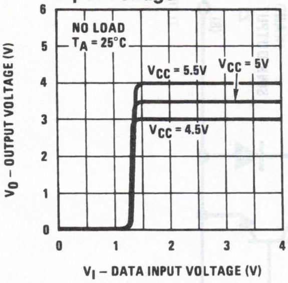

≤ 5 ns
≤ 5 ns
3V
90%
90%
INPUT
1.5V
1.5V
10%
10%
0V
t_{PLH}
t_{PHL}
V_{OH}
Y OUTPUT
1.5V
1.5V
V_{OL}
t_{PHL}
t_{PLH}
V_{OH}
Z OUTPUT
1.5V
1.5V
V_{OL}

TL/F/5786-4

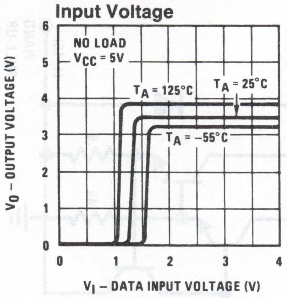
FIGURE 1

Typical Performance Characteristics*

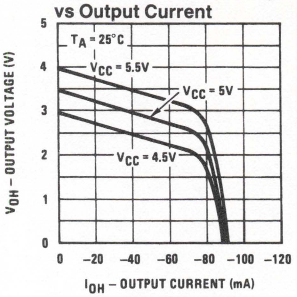
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage

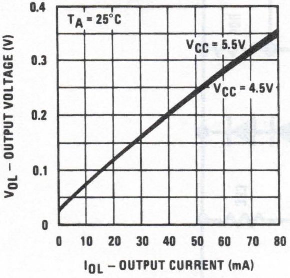


High Level Output Voltage vs Output Current

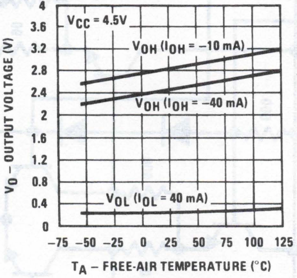


TL/F/5786–5

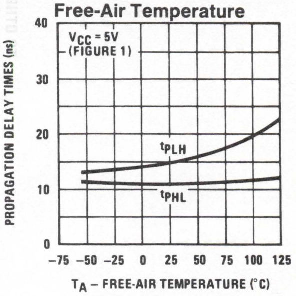
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature

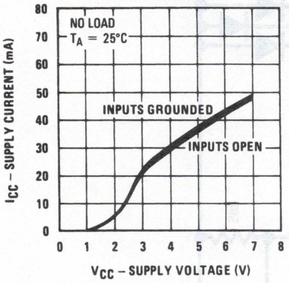


Propagation Delay Times vs Free-Air Temperature

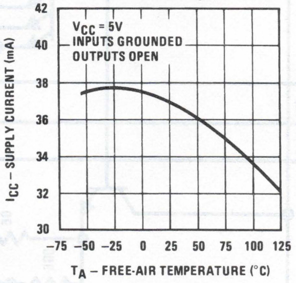


TL/F/5786–6

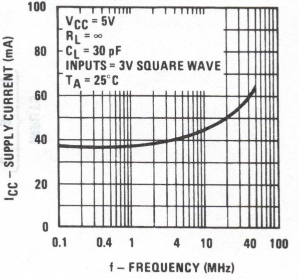
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



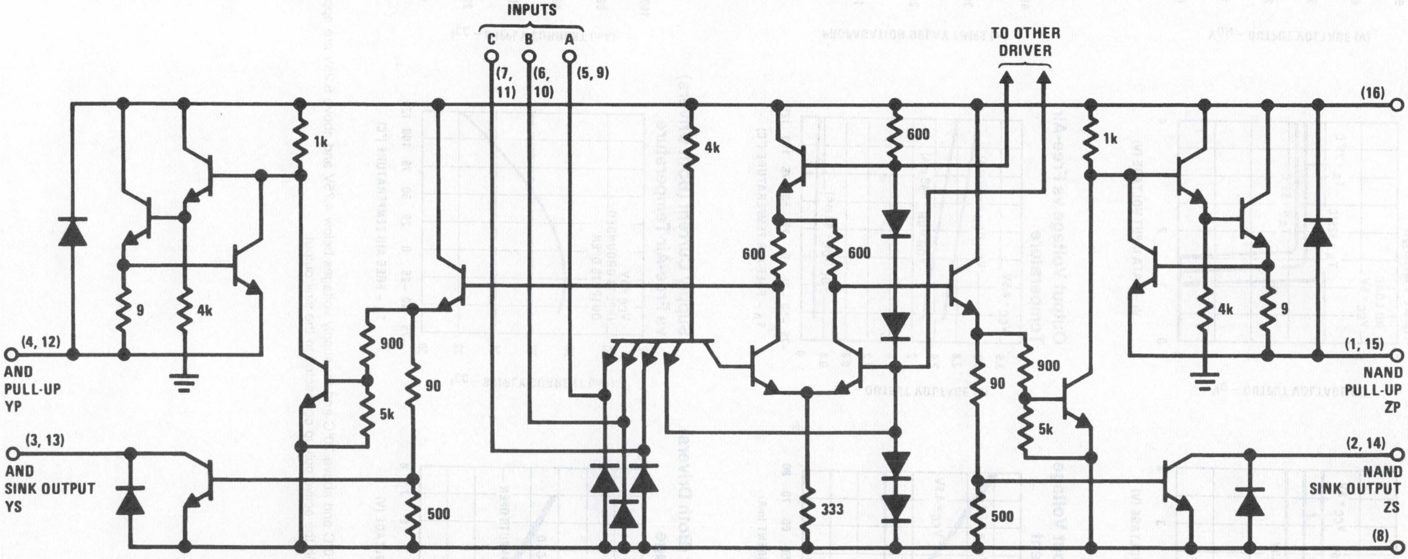
Supply Current (Both Drivers) vs Frequency



TL/F/5786–7

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Schematic Diagram (Each Driver)


INPUTS
C
B
A
(7, 11)
(6, 10)
(5, 9)
TO OTHER DRIVER
(16)
VCC
1k
4k
600
600
600
1k
9
4k
900
90
5k
500
333
90
900
5k
500
4k
9
(4, 12)
AND PULL-UP YP
(3, 13)
AND SINK OUTPUT YS
(1, 15)
NAND PULL-UP ZP
(2, 14)
NAND SINK OUTPUT ZS
(8)
GND

Resistor values shown are typical and in ohms.

TL/F/5786-2

National Semiconductor

DS55115/DS75115 Dual Differential Line Receiver

General Description

The DS55115/DS75115 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS55115/DS75115 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

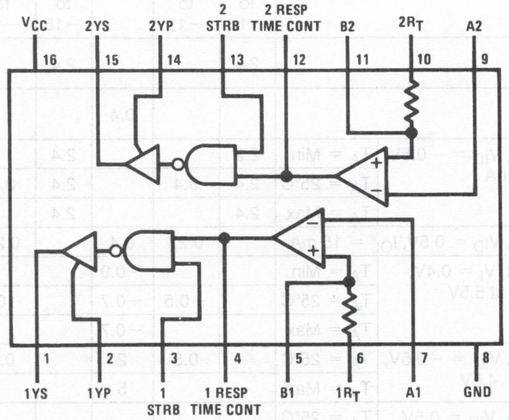
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



TL/F/5787–1

Top View

Order Number DS55115J, DS75115J or DS75115N
See NS Package Number J16A or N16A

Function Table

Strobe	Diff. Input	Output
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage at A, B and R_T Inputs	±25V
Input Voltage at Strobe Input	5.5V
Off-State Voltage Applied to Open-Collector Outputs	14V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55115	−55°C to +125°C
DS57115	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(1⁄16 inch from case for 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS55115	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current (I_{OH})		−5	mA
Low Level Output Current (I_{OL})		15	mA
Operating Temperature (T_A)			
DS55115	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
V_{TH}	Differential Input High-Threshold Voltage	$V_O = 0.4V$, $I_{OL} = 15$ mA, $V_{IC} = 0V$			200	500		200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	$V_O = 2.4V$, $I_{OH} = -5$ mA, $V_{IC} = 0V$			−200	−500		−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	$V_{ID} = \pm 1V$		15 to −15	24 to −19		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4			0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, $V_{ID} = -0.5V$, $I_{OH} = -5$ mA	T_A = Min	2.2			2.4			V
			$T_A = 25°C$	2.4	3.4		2.4	3.4		
			T_A = Max	2.4			2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, $V_{ID} = 0.5V$, $I_{OL} = 15$ mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, $V_I = 0.4V$, Other Input at 5.5V	T_A = Min			−0.9			−0.9	mA
			$T_A = 25°C$		−0.5	−0.7		−0.5	−0.7	
			T_A = Max			−0.7			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, $V_{ID} = -0.5V$, $V_{STROBE} = 4.5V$	$T_A = 25°C$		0.5	2		0.5	5	μA
			T_A = Max			5			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, $V_{ID} = 0.5V$, $V_{STROBE} = 0.4V$	$T_A = 25°C$		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max. $V_{ID} = 0.5V$, $V_{RC} = 0V$	$T_A = 25°C$	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, $V_{OH} = 12V$, $V_{ID} = -4.5V$	$T_A = 25°C$			100				μA
			T_A = Max			200				
		V_{CC} = Min, $V_{OH} = 5.25V$, $V_{ID} = -4.75V$	$T_A = 25°C$						100	
			T_A = Max						200	

Electrical Characteristics (Notes 2, 3 and 5) (Continued)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
R_T	Line Terminating Resistance	$V_{CC} = 5V$	$T_A = 25°C$	77	130	167	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, $V_O = 0V$, $V_{ID} = -0.5V$, (Note 4)	$T_A = 25°C$	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers)	V_{CC} = Max, $V_{ID} = 0.5V$, $V_{IC} = 0V$	$T_A = 25°C$		32	50		32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for the actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55115 and across the 0°C to +70°C range for the DS75115. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

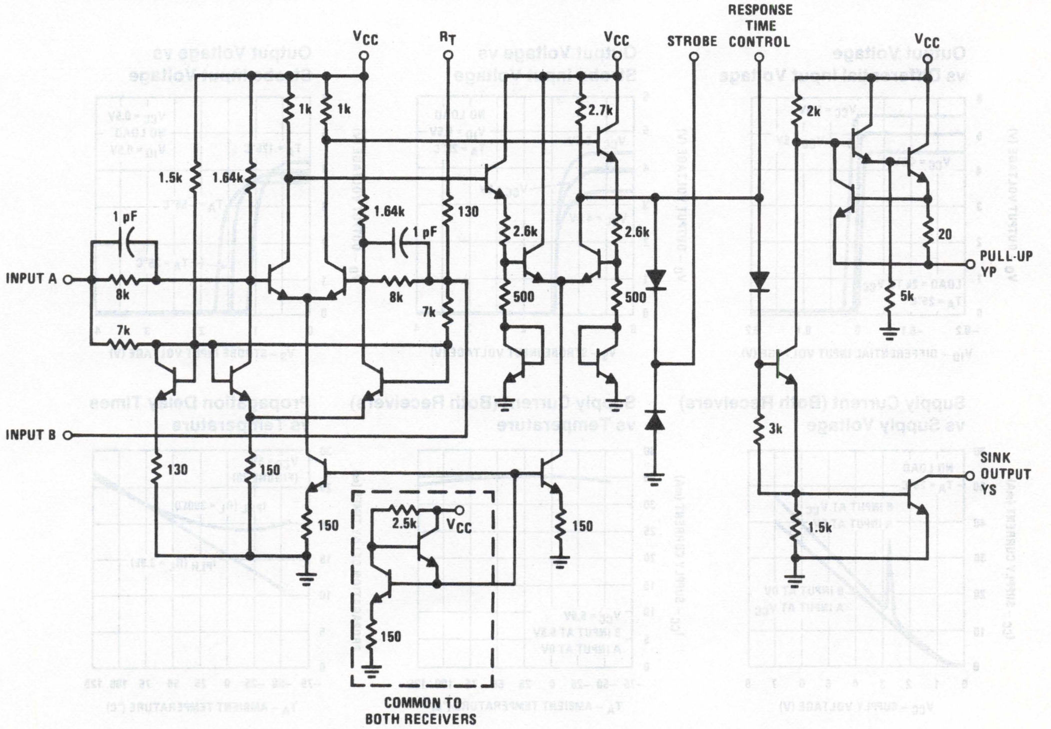
Note 4: Only one output at a time should be shorted.

Note 5: Unless otherwise noted, $V_{STROBE} = 2.4V$. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics $V_{CC} = 5V$, $C_L = 30\ pF$, $T_A = 25°C$

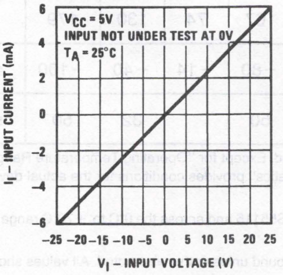
Symbol	Parameter	Conditions	DS55115			DS75115			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 3.9\ k\Omega$, *(Figure 1)*		18	50		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 390\Omega$, *(Figure 1)*		20	50		20	75	ns

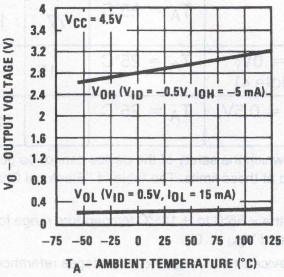
Schematic Diagram

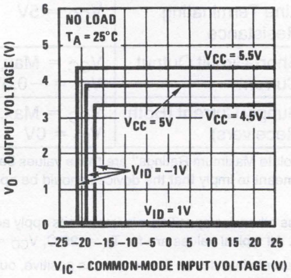

VCC
RT
VCC
STROBE
RESPONSE TIME CONTROL
VCC
1k
1k
2.7k
2k
1.5k
1.64k
1.64k
130
1 pF
1 pF
2.6k
2.6k
20
PULL-UP YP
INPUT A
8k
8k
7k
500
500
5k
7k
INPUT B
3k
130
150
150
150
2.5k
VCC
SINK OUTPUT YS
1.5k
150
COMMON TO BOTH RECEIVERS

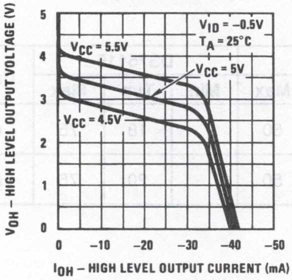
TL/F/5787-2

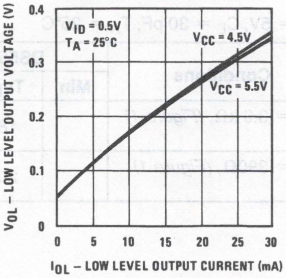
Typical Performance Characteristics (Note 3)

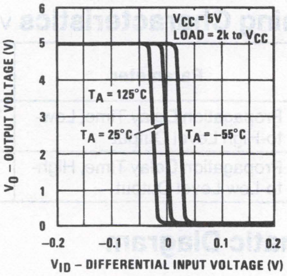

Input Current vs Input Voltage

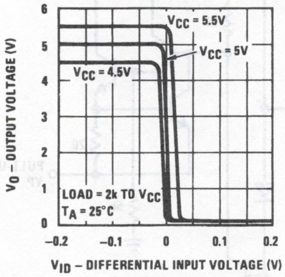

Output Voltage vs Temperature

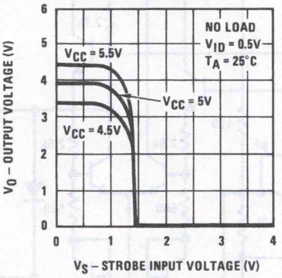

Output Voltage vs Common-Mode Input Voltage

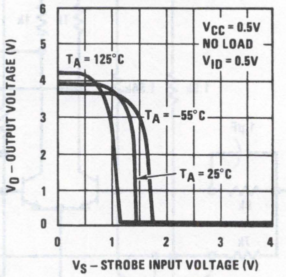

High Level Output Voltage vs Output Current

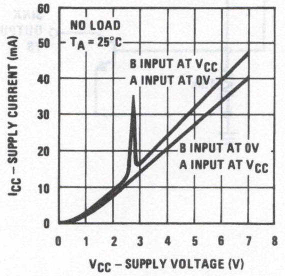

Low Level Output Voltage vs Output Current

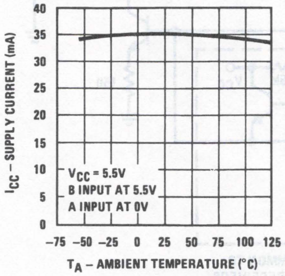

Output Voltage vs Differential Input Voltage

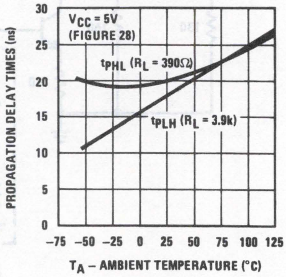

Output Voltage vs Differential Input Voltage


Output Voltage vs Strobe Input Voltage


Output Voltage vs Strobe Input Voltage

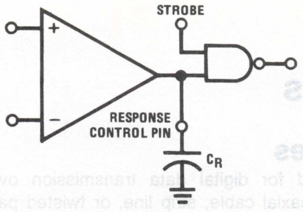

Supply Current (Both Receivers) vs Supply Voltage


Supply Current (Both Receivers) vs Temperature


Propagation Delay Times vs Temperature

TL/F/5787–4

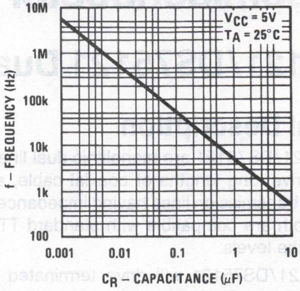
Frequency Response Control


STROBE
+
−
RESPONSE
CONTROL PIN
C_R

TL/F/5787-5

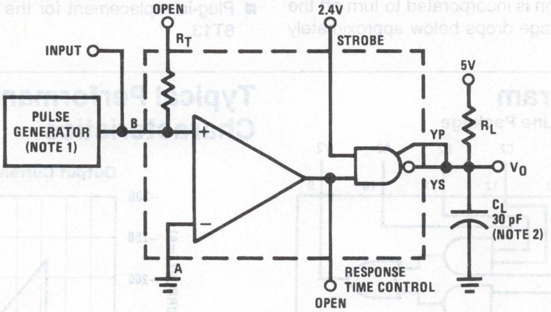
Note: C_R (response control) > 0.01 µF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



TL/F/5787-6

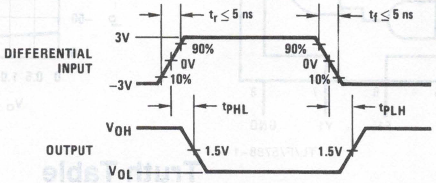
AC Test Circuit and Switching Time Waveforms


OPEN
R_T
INPUT
PULSE
GENERATOR
(NOTE 1)
B
+
−
A
2.4V
STROBE
5V
R_L
YP
YS
V_O
C_L
30 pF
(NOTE 2)
RESPONSE
TIME CONTROL
OPEN

TL/F/5787-7

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz/t_W = 100 ns

Note 2: C_L includes probe and test fixture capacitance

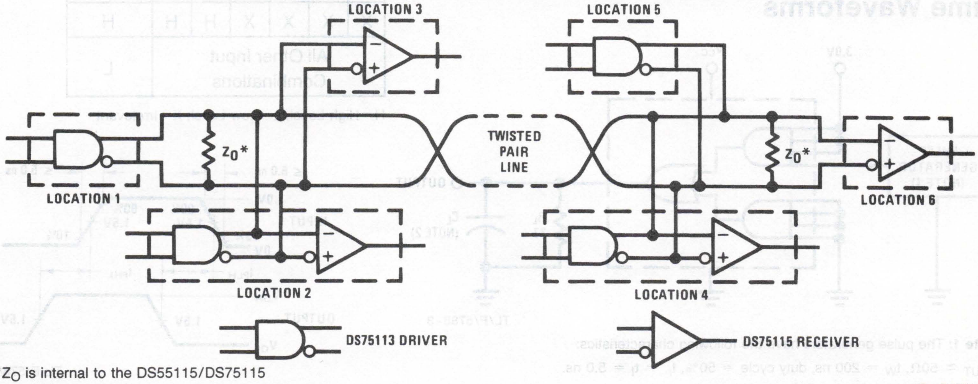

$t_r \leq 5$ ns
$t_f \leq 5$ ns
3V
DIFFERENTIAL
INPUT
−3V
90%
0V
10%
90%
0V
10%
t_{PHL}
t_{PLH}
V_{OH}
OUTPUT
V_{OL}
1.5V
1.5V

TL/F/5787-8

FIGURE 1. Propagation Delay Time

Typical Application

Basic Party-Line or Data-Bus Differential Data Transmission


LOCATION 3
LOCATION 5
LOCATION 1
Z_O*
TWISTED
PAIR
LINE
Z_O*
LOCATION 6
LOCATION 2
LOCATION 4
DS75113 DRIVER
DS75115 RECEIVER

*Z_O is internal to the DS55115/DS75115

A capacitor may be connected in series with Z_O to reduce power dissipation.

TL/F/5787-3

National Semiconductor

DS55121/DS75121 Dual Line Drivers

General Description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50Ω to 500Ω. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

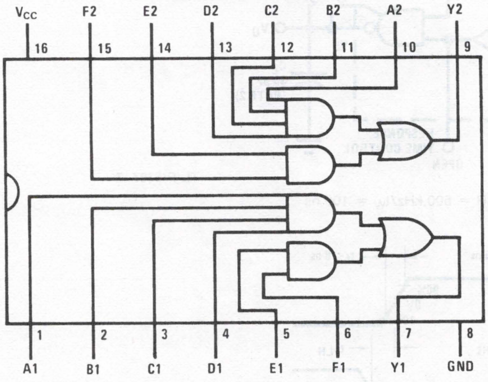
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package



V_{CC}
F2
E2
D2
C2
B2
A2
Y2
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A1
B1
C1
D1
E1
F1
Y1
GND

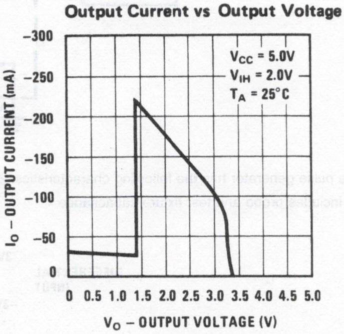
TL/F/5788-1

Top View

Order Number DS55121J, DS75121J or DS75121N

See NS Package Number J16A or N16A

Typical Performance Characteristics



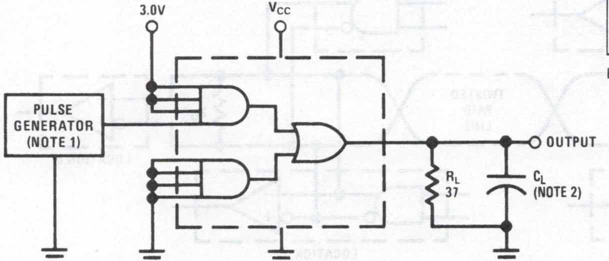
TL/F/5788-2

Truth Table

Inputs						Output
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

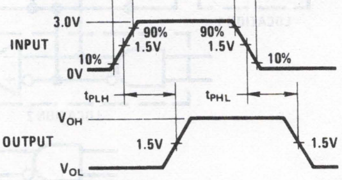
H = High Level, L = Low Level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



3.0V
V_{CC}
PULSE GENERATOR (NOTE 1)
OUTPUT
R_L 37
C_L (NOTE 2)

TL/F/5788-3



≤ 5.0 ns
≤ 5.0 ns
3.0V
INPUT
0V
90%
1.5V
10%
90%
1.5V
10%
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT
V_{OL}
1.5V
1.5V

TL/F/5788-4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, t_r, = t_f = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS55121	−55	+125	°C
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	µA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	µA
I_{IH}	High Level Input Current	V_I = 4.5V			40	µA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55121 and across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

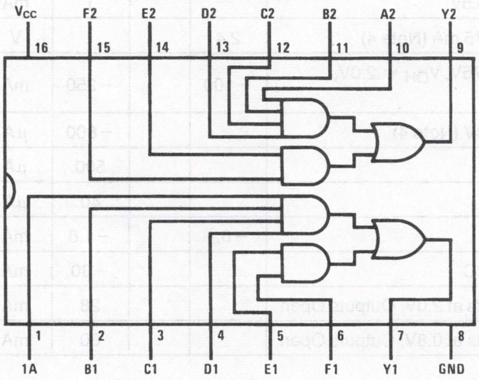
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at $I_{OH} = -59.3$ mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

Dual-In-Line Package



Vcc
16
F2
15
E2
14
D2
13
C2
12
B2
11
A2
10
Y2
9
1
1A
2
B1
3
C1
4
D1
5
E1
6
F1
7
Y1
8
GND

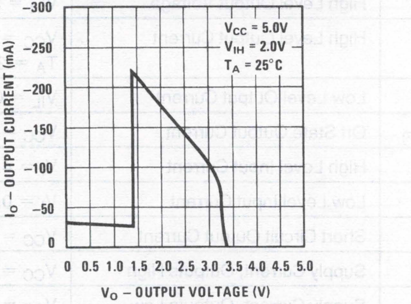
TL/F/5790-1

Top View

Order Number DS75123J or DS75123N
See NS Package Number J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage



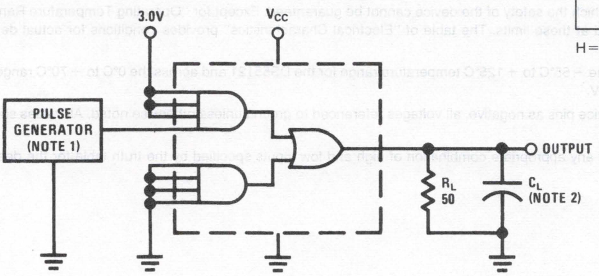
TL/F/5790-3

Truth Table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

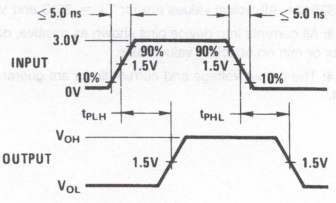
H = High level, L = Low level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



3.0V
V_{CC}
PULSE GENERATOR (NOTE 1)
OUTPUT
R_L 50
C_L (NOTE 2)

TL/F/5790-2



≤ 5.0 ns
≤ 5.0 ns
3.0V
INPUT
90%
90%
1.5V
1.5V
10%
10%
0V
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT
1.5V
1.5V
V_{OL}

TL/F/5790-4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$V_{CC} = 5.0V$, $I_I = -12$ mA				−1.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.25V$, $V_{IN} = 5.5V$				1	mA
V_{OH}	High Level Output Voltage	$V_{CC} = 5.0V$, $V_{IH} = 2.0V$, $I_{OH} = -59.3$ mA, (Note 4)	$T_A = 25°C$	3.11			V
			$T_A = 0°C$ to $+75°C$	2.9			V
I_{OH}	High Level Output Current	$V_{CC} = 5.0V$, $V_{IH} = 4.5V$, $T_A = 25°C$, $V_{OH} = 2.0V$, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	$V_{IL} = 0.8V$, $I_{OL} = -240\ \mu A$, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	$V_{CC} = 0$, $V_O = 3.0V$				40	µA
I_{IH}	High Level Input Current	$V_I = 4.5V$				40	µA
I_{IL}	Low Level Input Current	$V_I = 0.4V$		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = 5.0V$, $T_A = 25°C$				−30	mA
I_{CCH}	Supply Current, Outputs High	$V_{CC} = 5.25V$, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	$V_{CC} = 5.25V$, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 50\Omega$, (See AC Test Circuit and Switching Time Waveforms	$C_L = 15$ pF		12	20	ns
			$C_L = 100$ pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 50\Omega$, (See AC Test Circuit and Switching Time Waveforms	$C_L = 15$ pF		12	20	ns
			$C_L = 100$ pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for $V_{CC} = 5.0V$, $T_A = 25°C$. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS75124 Triple Line Receiver

General Description

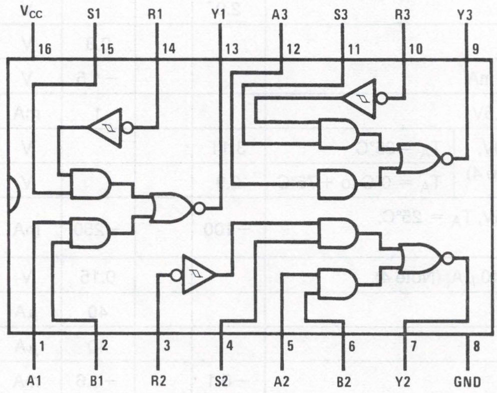
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package


VCC
S1
R1
Y1
A3
S3
R3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A1
B1
R2
S2
A2
B2
Y2
GND

TL/F/5792–1

Top View

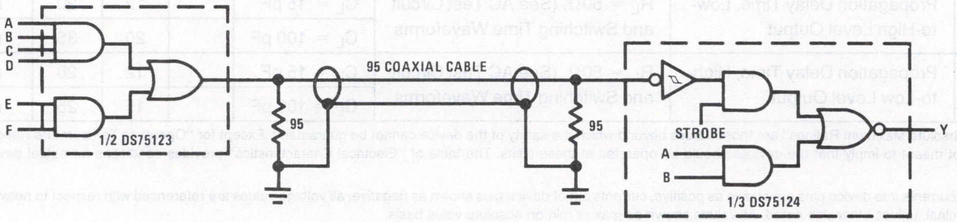
Order Number DS75124J or DS75124N
See NS Package Number J16A or N16A

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

Typical Application


A
B
C
D
E
F
1/2 DS75123
95 COAXIAL CABLE
95
95
STROBE
A
B
Y
1/3 DS75124

TL/F/5792–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, or S		2.0			V
		R		1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S				0.8	V
		R				0.8	V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5.0V$, $T_A = 25°C$, R, (Note 6)		0.2	0.4		V
V_I	Input Clamp Voltage	$V_{CC} = 5.0V$, $I_I = -12$ mA, A, B, or S				−1.5	V
I_I	Input Current at Maximum Input Voltage	$V_{CC} = 5.25V$, $V_{IN} = 5.5V$, A, B, or S				1	mA
		R	$V_I = 7.0V$			5.0	mA
			$V_I = 6.0V$, $V_{CC} = 0V$			5.0	mA
V_{OH}	High Level Output Voltage	$V_{IH} = V_{IHMIN}$, $V_{IL} = V_{ILMAX}$, $I_{OH} = -800$ μA, (Note 4)		2.6			V
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{IHMIN}$, $V_{IL} = V_{ILMAX}$, $I_{OL} = 16$ mA, (Note 4)				0.4	V
I_{IH}	High Level Input Current	$V_I = 4.5V$, A, B, or S				40	μA
		$V_I = 3.11V$, R				170	μA
I_{IL}	Low Level Input Current	$V_I = 0.4V$, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = 5.0V$, $T_A = 25°C$, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	$V_{CC} = 5.25V$				72	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

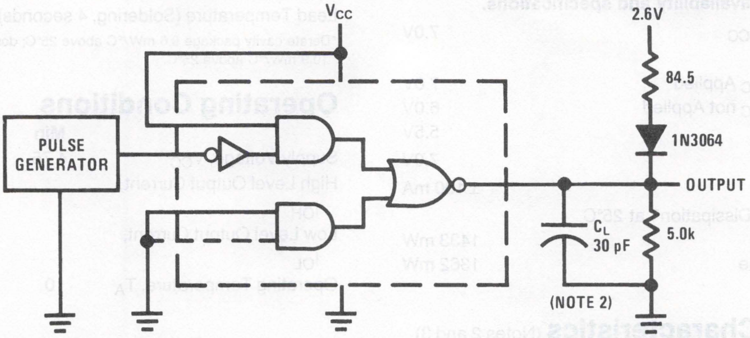
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for $V_{CC} = 5.0V$, $T_A = 25°C$. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

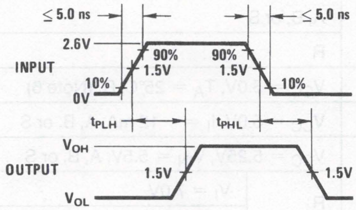
AC Test Circuit and Switching Time Waveforms


V_{CC}
PULSE GENERATOR
2.6V
84.5
1N3064
OUTPUT
C_L 30 pF
5.0k
(NOTE 2)

TL/F/5792-3

Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%

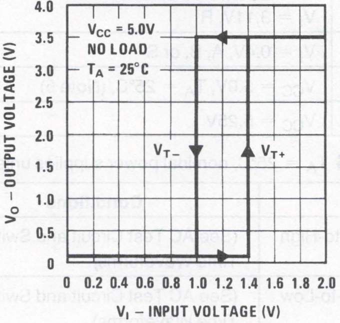
Note 2: C_L includes probe and jig capacitance.


≤ 5.0 ns
≤ 5.0 ns
2.6V
INPUT
90%
90%
1.5V
1.5V
10%
10%
0V
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT
1.5V
1.5V
V_{OL}

TL/F/5792-4

Typical Performance Characteristics

Output Voltage vs Receiver Input Voltage



TL/F/5792-5

National Semiconductor

DS75125/DS75127 Seven-Channel Line Receivers

General Description

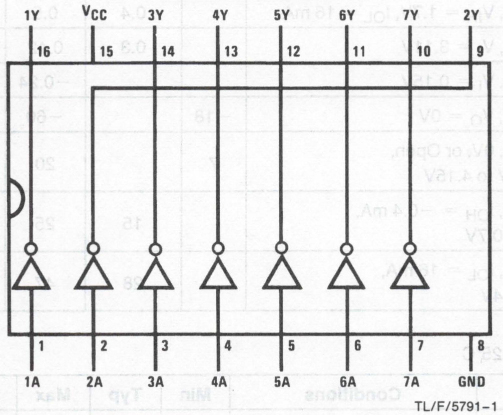
The DS75125 and DS75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply current requirements while maintaining fast switching speeds and high current TTL outputs. The DS75125 and DS75127 are characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from single 5V supply
- High speed—low propagation delay
- Ratio specification for propagation delay time, low-to-high/high-to-low
- Seven channels in one 16-pin package
- Standard V_{CC} and ground positioning on DS75127

Connection Diagrams

DS75125
Dual-In-Line Package

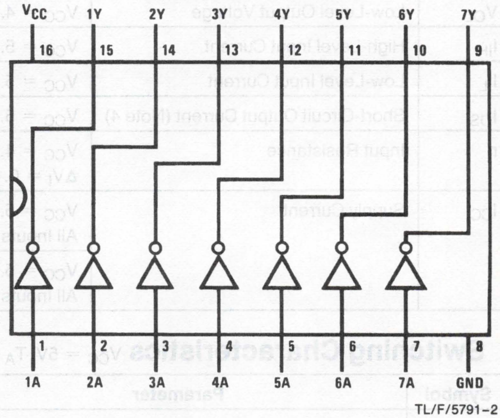

1Y
VCC
3Y
4Y
5Y
6Y
7Y
2Y
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1A
2A
3A
4A
5A
6A
7A
GND
TL/F/5791-1

Top View

logic: Y = A

Order Number DS75125J or DS75125N
See NS Package Number J16A or N16A

DS75127
Dual-In-Line Package


VCC
1Y
2Y
3Y
4Y
5Y
6Y
7Y
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1A
2A
3A
4A
5A
6A
7A
GND
TL/F/5791-2

Top View

logic: Y = A

Order Number DS75127J or DS75127N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage Range	
DS75125	−0.15V to 7V
DS75127	−2V to 7V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C (Note 2)	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage		1.7			V
V_{IL}	Low-Level Input Voltage				0.7	V
V_{OH}	High-Level Output Voltage	$V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = -0.4$ mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage	$V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16$ mA		0.4	0.5	V
I_{IH}	High-Level Input Current	$V_{CC} = 5.5V, V_I = 3.11V$		0.3	0.42	mA
I_{IL}	Low-Level Input Current	$V_{CC} = 5.5V, V_I = 0.15V$			−0.24	mA
I_{OS}	Short-Circuit Output Current (Note 4)	$V_{CC} = 5.5V, V_O = 0V$	−18		−60	mA
r_I	Input Resistance	$V_{CC} = 4.5V$, 0V, or Open, $\Delta V_I = 0.15V$ to $4.15V$	7		20	kΩ
I_{CC}	Supply Current	$V_{CC} = 5.5V, I_{OH} = -0.4$ mA, All Inputs at 0.7V		15	25	mA
		$V_{CC} = 5.5V, I_{OL} = 16$ mA, All Inputs at 4V		28	47	mA

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$R_L = 400\Omega, C_L = 50$ pF, (See *Figure 1*)	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of Propagation Delay Times		0.5	0.8	1.3	ns
t_{TLH}	Transition Time, Low-to-High-Level Output		1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output		1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

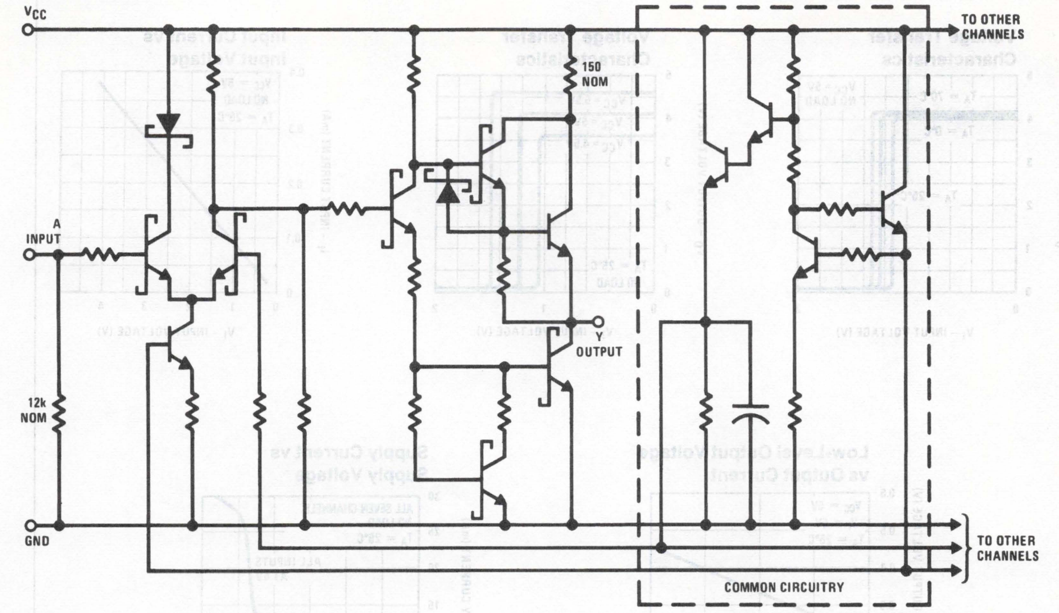
Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output should be shorted at a time.

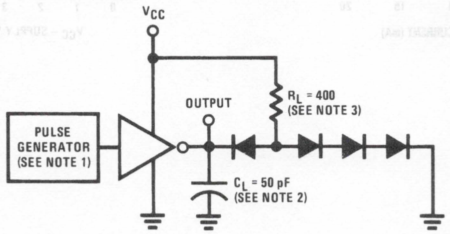
Note 5: All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

Schematic (each receiver)

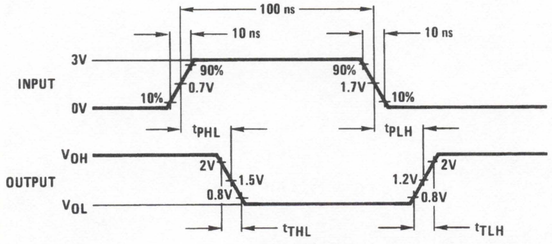

VCC
TO OTHER CHANNELS
150 NOM
A INPUT
12k NOM
Y OUTPUT
GND
TO OTHER CHANNELS
COMMON CIRCUITRY

TL/F/5791-3

AC Test Circuit and Switching Time Waveforms


VCC
OUTPUT
R_L = 400 (SEE NOTE 3)
PULSE GENERATOR (SEE NOTE 1)
C_L = 50 pF (SEE NOTE 2)

TL/F/5791-4


100 ns
10 ns
10 ns
3V
INPUT
0V
90%
0.7V
10%
90%
1.7V
10%
t_{PHL}
t_{PLH}
V_{OH}
OUTPUT
V_{OL}
2V
1.5V
0.8V
1.2V
2V
0.8V
t_{THL}
t_{TLH}

TL/F/5791-5

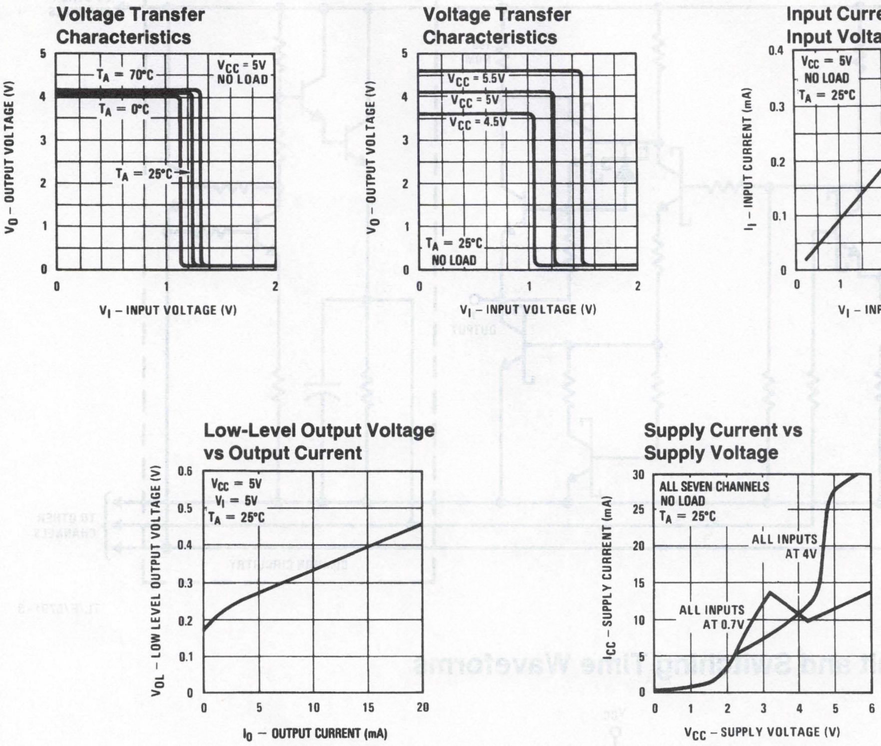
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 5 MHz.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

FIGURE 1

Typical Performance Characteristics


Voltage Transfer Characteristics

Voltage Transfer Characteristics

Input Current vs Input Voltage

Low-Level Output Voltage vs Output Current

Supply Current vs Supply Voltage

TL/F/5791-6

National Semiconductor

DS75128/DS75129 Eight-Channel Line Receivers

General Description

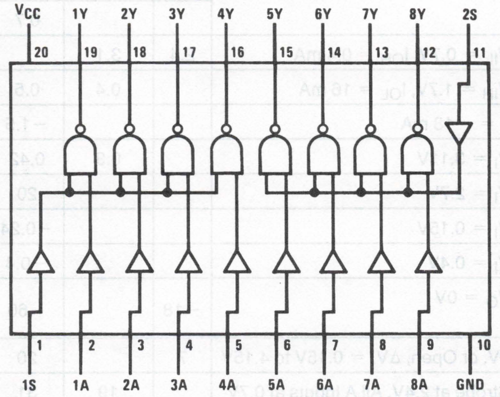
The DS75128 and DS75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The DS75128 has an active-high strobe; the DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75128 and DS75129 are characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed—low propagation delay
- Ratio specification—t_{PLH}/t_{PLH}
- Common strobe for each group of four receivers
- DS75128 strobe—active-high
  DS75129 strobe—active-low

Connection Diagrams

DS75128
Dual-In-Line Package


VCC 1Y 2Y 3Y 4Y 5Y 6Y 7Y 8Y 2S
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
1S 1A 2A 3A 4A 5A 6A 7A 8A GND

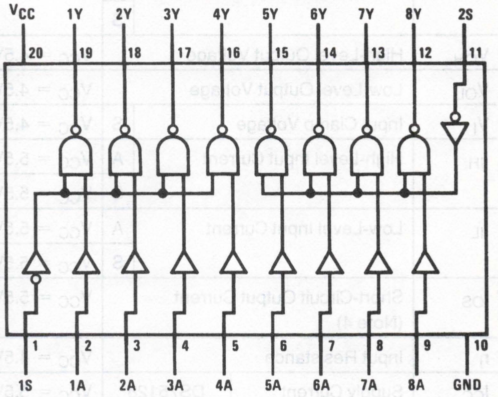
positive logic: Y = $\overline{AS}$

TL/F/5793-1

Top View

Order Number DS75128J or DS75128N
See NS Package Number J20A or N20A

DS75129
Dual-In-Line Package


VCC 1Y 2Y 3Y 4Y 5Y 6Y 7Y 8Y 2S
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
1S 1A 2A 3A 4A 5A 6A 7A 8A GND

positive logic: Y = $\overline{AS}$

TL/F/5793-2

Top View

Order Number DS75129J or DS75129N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Maximum Power Dissipation* at 25°C (Note 2)	
Cavity Package	1564 mW
Molded Package	1687 mW
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature 1/16 Inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 Inch from Case for 4 Seconds: N Package	260°C

*Derate cavity package 10.4 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter		Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage	A		1.7			V
		S		2			
V_{IL}	Low-Level Input Voltage	A				0.7	V
		S				0.7	
V_{OH}	High-Level Output Voltage		V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = 0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I	Input Clamp Voltage	S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH}	High-Level Input Current	A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low-Level Input Current	A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS}	Short-Circuit Output Current (Note 4)		V_{CC} = 5.5V, V_O = 0V	−18		−60	mA
r_I	Input Resistance		V_{CC} = 4.5V, 0V, or Open, ΔV, = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current	DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 0.7V		19	31	mA
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	
		DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 4V		32	53	
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

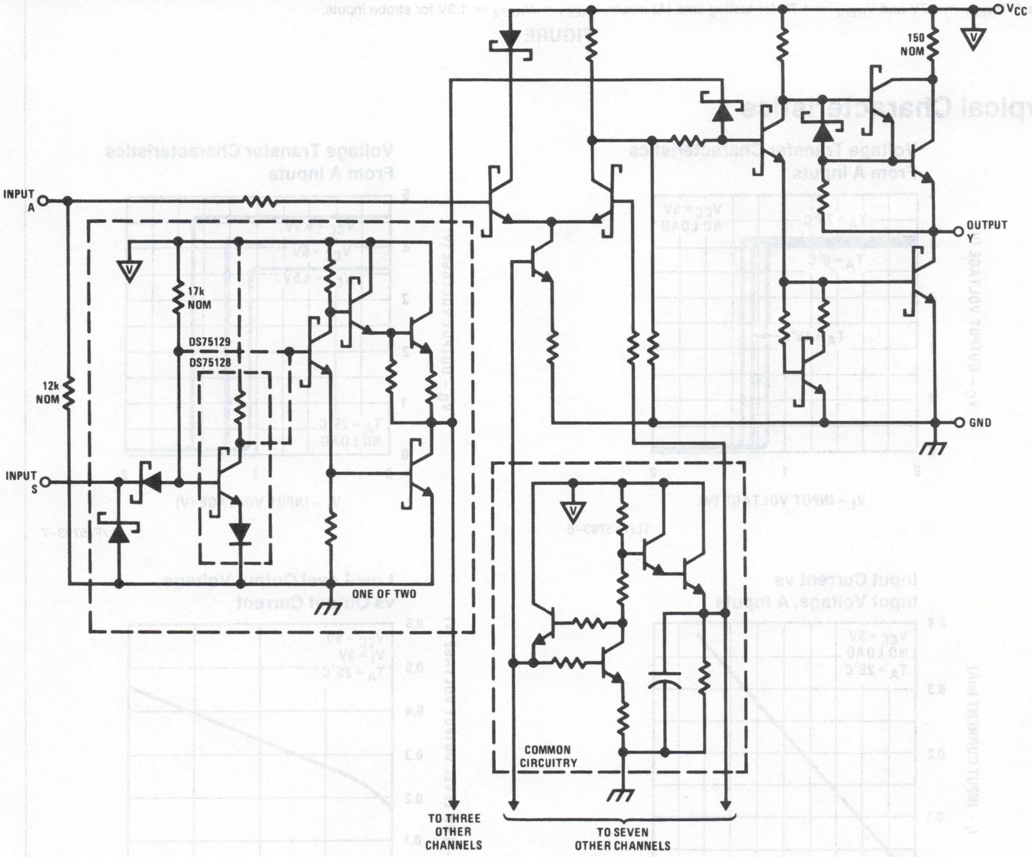
Note 4: Only one output should be shorted at a time.

Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter		Conditions	DS75128 Min	DS75128 Typ	DS75128 Max	DS75129 Min	DS75129 Typ	DS75129 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	$R_L = 400\Omega$, $C_L = 50$ pF, See *Figure 1*	7	14	25	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			10	18	30	10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			26	40		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output			1	3	12	1	3	12	ns

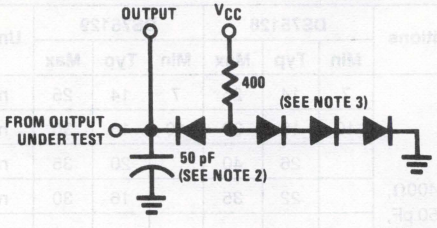
Schematic Diagram (each receiver)



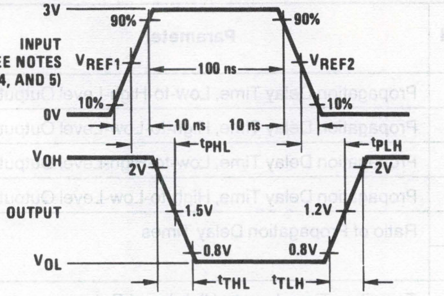
V_{CC}
150 NOM
INPUT A
17k NOM
DS75129
DS75128
12k NOM
INPUT S
ONE OF TWO
OUTPUT Y
GND
COMMON CIRCUITRY
TO THREE OTHER CHANNELS
TO SEVEN OTHER CHANNELS

TL/F/5793-3

AC Test Circuit and Switching Time Waveforms


OUTPUT
V_{CC}
400
(SEE NOTE 3)
FROM OUTPUT UNDER TEST
50 pF (SEE NOTE 2)

TL/F/5793-4


3V
90%
90%
INPUT (SEE NOTES 1, 4, AND 5)
V_{REF1}
100 ns
V_{REF2}
10%
10%
0V
10 ns
10 ns
t_{PHL}
t_{PLH}
V_{OH}
2V
2V
OUTPUT
1.5V
1.2V
0.8V
0.8V
V_{OL}
t_{THL}
t_{TLH}

TL/F/5793-5

Note 1: Input pulses are supplied by a generator having the following characteristics: $Z_O = 50\Omega$, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

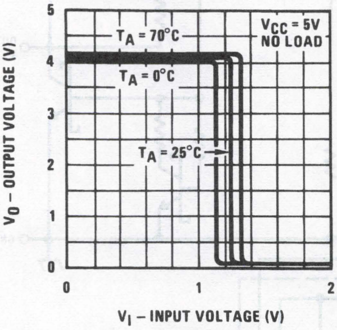
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: $V_{REF1} = 0.7V$ and $V_{REF2} = 1.7V$ for testing data (A) inputs, $V_{REF1} = V_{REF2} = 1.3V$ for strobe inputs.

FIGURE 1

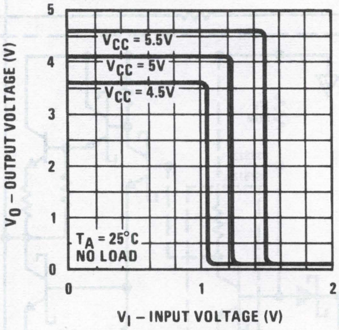
Typical Characteristics

Voltage Transfer Characteristics From A Inputs



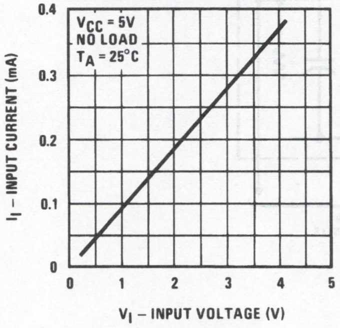
TL/F/5793-6

Voltage Transfer Characteristics From A Inputs



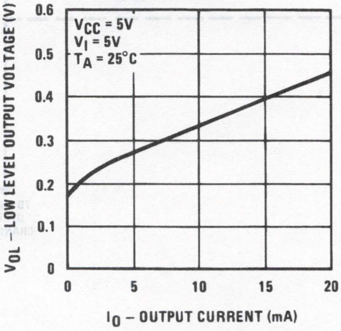
TL/F/5793-7

Input Current vs Input Voltage, A Inputs



TL/F/5793-8

Low-Level Output Voltage vs Output Current



TL/F/5793-9

National Semiconductor

DS75150 Dual Line Driver

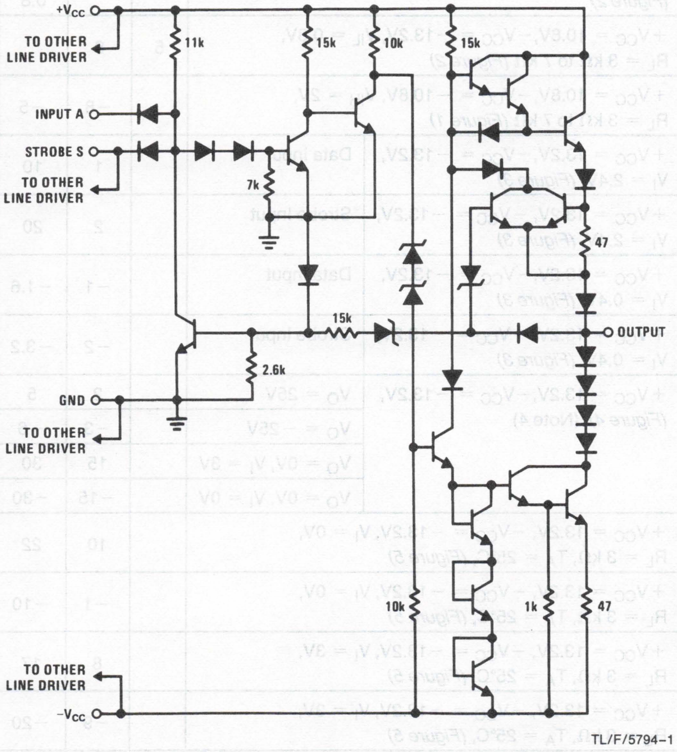
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

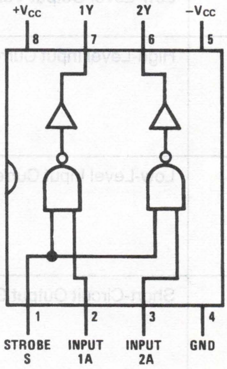
- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2 μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

Schematic and Connection Diagrams


+VCC
TO OTHER LINE DRIVER
11k
15k
10k
15k
INPUT A
STROBE S
TO OTHER LINE DRIVER
7k
47
15k
OUTPUT
2.6k
GND
TO OTHER LINE DRIVER
10k
1k
47
TO OTHER LINE DRIVER
-VCC
TL/F/5794-1

Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package


+VCC
1Y
2Y
−VCC
8
7
6
5
1
2
3
4
STROBE S
INPUT 1A
INPUT 2A
GND

TL/F/5794-2

Top View

Positive Logic C = $\overline{AS}$

Order Number DS75150J-8, DS75150M or DS75150N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	15V
Input Voltage	15V
Applied Output Voltage	+25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded DIP Package	1022 mW
SO Package	655 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded DIP package 8.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC} = 10.8V, -V_{CC} = -13.2V, V_{IL} = 0.8V,$ $R_L = 3\ k\Omega$ to $7\ k\Omega$ *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC} = 10.8V, -V_{CC} = -10.8V, V_{IH} = 2V,$ $R_L = 3\ k\Omega$ to $7\ k\Omega$ *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ $V_I = 2.4V$, *(Figure 3)*	Data Input		1	10	µA
		$+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ $V_I = 2.4V$, *(Figure 3)*	Strobe Input		2	20	µA
I_{IL}	Low-Level Input Current	$+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ $V_I = 0.4V$, *(Figure 3)*	Data Input		−1	−1.6	mA
		$+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ $V_I = 0.4V$, *(Figure 3)*	Strobe Input		−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ *(Figure 4)*, (Note 4)	$V_O = 25V$		2	5	mA
			$V_O = -25V$		−3	−6	mA
			$V_O = 0V, V_I = 3V$		15	30	mA
			$V_O = 0V, V_I = 0V$		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_I = 0V,$ $R_L = 3\ k\Omega, T_A = 25°C$, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_I = 0V,$ $R_L = 3\ k\Omega, T_A = 25°C$, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_I = 3V,$ $R_L = 3\ k\Omega, T_A = 25°C$, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_I = 3V,$ $R_L = 3\ k\Omega, T_A = 25°C$, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are $T_A = 25°C$ and $+V_{CC} = 12V$, $-V_{CC} = -12V$.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

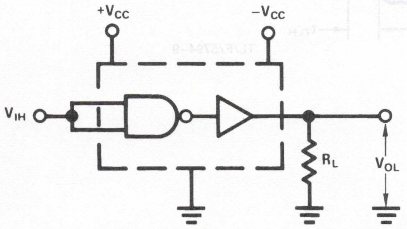
Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is more-negative voltage.

AC Electrical Characteristics (+V_{CC} = 12V, −V_{CC} = −12V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

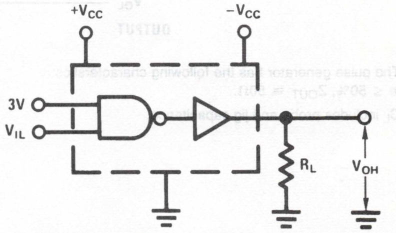
DC Test Circuits



+VCC
−VCC
VIH
RL
VOL

TL/F/5794–3

FIGURE 1. V_{IH}, V_{OL}

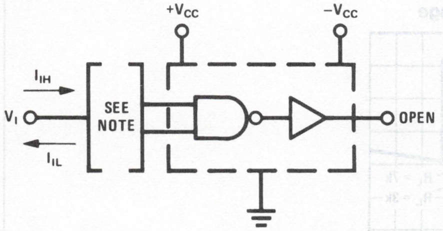


+VCC
−VCC
3V
VIL
RL
VOH

TL/F/5794–4

Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}

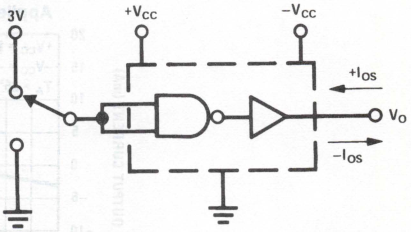


+VCC
−VCC
IIH
VI
IIL
SEE NOTE
OPEN

TL/F/5794–5

Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

FIGURE 3. I_{IH}, I_{IL}

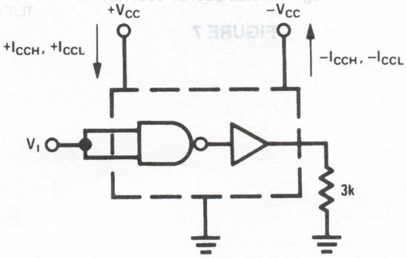


3V
+VCC
−VCC
+IOS
VO
−IOS

TL/F/5794–6

I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4. I_{OS}

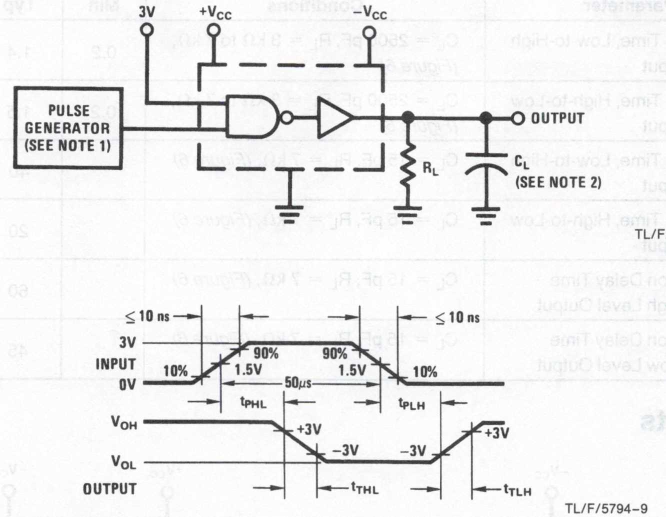


+VCC
−VCC
+ICCH, +ICCL
−ICCH, −ICCL
VI
3k

TL/F/5794–7

FIGURE 5. $I_{CCH}+$, $I_{CCH}-$, $I_{CCL}+$, $I_{CCL}-$

AC Test Circuit and Switching Waveforms


3V
+V_{CC}
−V_{CC}
PULSE GENERATOR (SEE NOTE 1)
OUTPUT
R_L
C_L (SEE NOTE 2)
≤ 10 ns
≤ 10 ns
3V
INPUT
0V
10%
90%
1.5V
90%
1.5V
10%
50μs
t_{PHL}
t_{PLH}
V_{OH}
V_{OL}
OUTPUT
+3V
−3V
−3V
+3V
t_{THL}
t_{TLH}

TL/F/5794-8

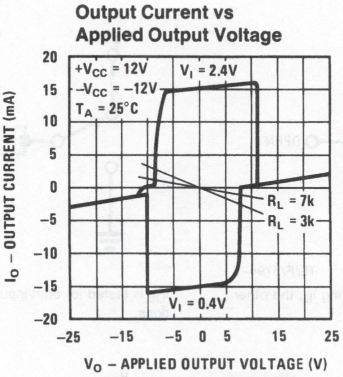
TL/F/5794-9

Note 1: The pulse generator has the following characterstics: duty cycle ≤ 50%, $Z_{OUT} \cong 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

Typical Performance Characteristics


Output Current vs Applied Output Voltage

TL/F/5794-10

FIGURE 7

National Semiconductor

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

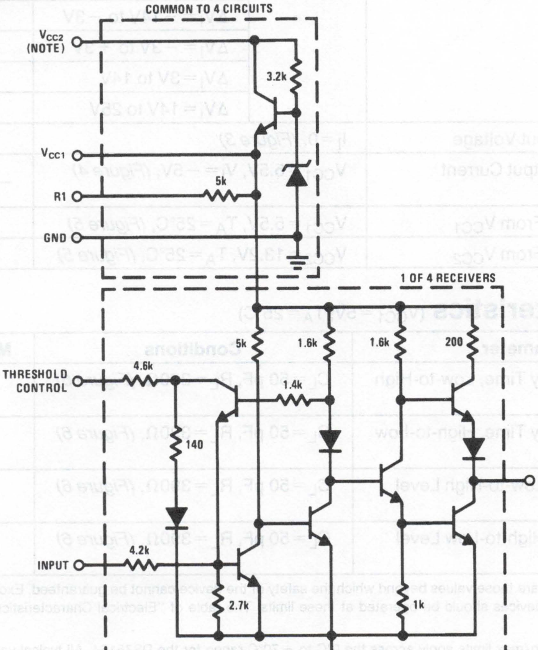
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic Diagram



TL/F/5795–1

Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16), (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	$I_{OH} = -400\ \mu A$, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 16$ mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	$\Delta V_I = -25V$ to $-14V$	3	5	7	kΩ
			$\Delta V_I = -14V$ to $-3V$	3	5	7	kΩ
			$\Delta V_I = -3V$ to $+3V$	3	6		kΩ
			$\Delta V_I = 3V$ to $14V$	3	5	7	kΩ
			$\Delta V_I = 14V$ to $25V$	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	$I_I = 0$, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	$V_{CC1} = 5.5V$, $V_I = -5V$, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	$V_{CC1} = 5.5V$, $T_A = 25°C$, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	$V_{CC2} = 13.2V$, $T_A = 25°C$, *(Figure 5)*			23	40	mA

Switching Characteristics ($V_{CC1} = 5V$, $T_A = 25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 50$ pF, $R_L = 390\Omega$, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 50$ pF, $R_L = 390\Omega$, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 50$ pF, $R_L = 390\Omega$, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 50$ pF, $R_L = 390\Omega$, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

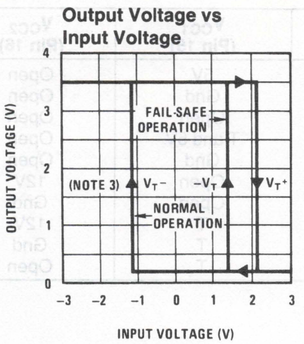
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

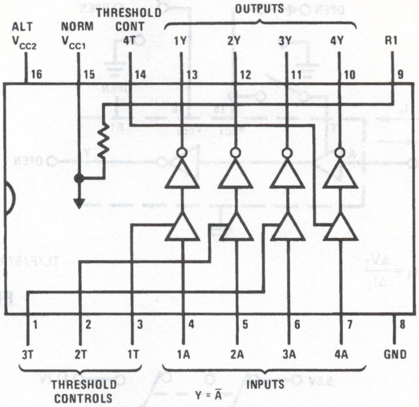
Typical Performance Characteristics



TL/F/5795-10

Connection Diagram

Dual-In-Line Package

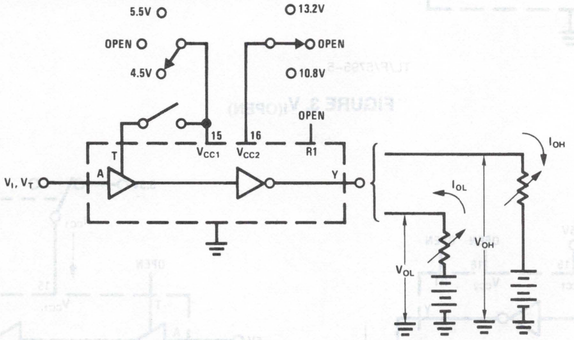

ALT V_{CC2}
NORM V_{CC1}
THRESHOLD CONT 4T
OUTPUTS
1Y
2Y
3Y
4Y
R1
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
3T
2T
1T
1A
2A
3A
4A
GND
THRESHOLD CONTROLS
INPUTS
$Y = \bar{A}$

TL/F/5795-2

Top View

Order Number DS75154J, DS75154M or DS75154N
See NS Package Number J16A, M16A or N16A

DC Test Circuits and Truth Tables


5.5V
OPEN
4.5V
13.2V
OPEN
10.8V
OPEN
15
16
V_{CC1}
V_{CC2}
R1
T
A
V_I, V_T
Y
I_{OH}
I_{OL}
V_{OH}
V_{OL}

TL/F/5795-3

Test	Measure	A	T	Y	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-Circuit Input (Fail-Safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (Fail-Safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	(Note 1) (Note 1)	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (Fail-Safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max, (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	(Note 2) (Note 2)	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

Note 1: Momentarily apply −5V, then 0.8V.

Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

DC Test Circuits and Truth Tables (Continued)

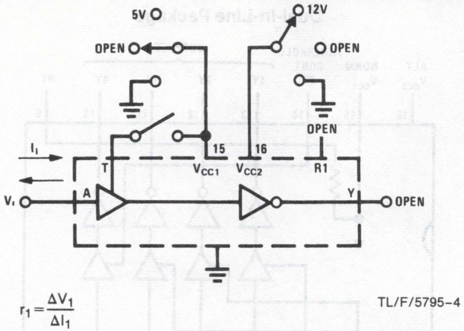

5V
12V
OPEN
OPEN
OPEN
I_I
15
16
T
V_{CC1}
V_{CC2}
R1
V_I
A
Y
OPEN
$r_1 = \frac{\Delta V_1}{\Delta I_1}$

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FIGURE 2. r_I

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

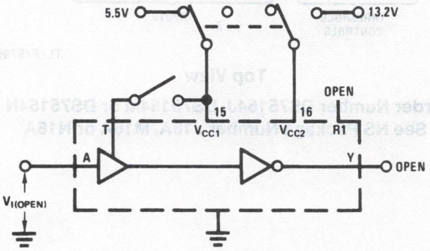
5.5V
13.2V
OPEN
15
16
T
V_{CC1}
V_{CC2}
R1
A
Y
OPEN
$V_{I(OPEN)}$

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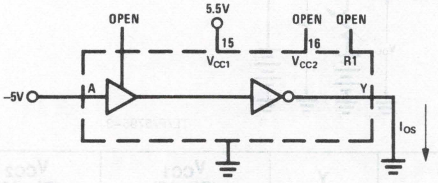
FIGURE 3. $V_{I(OPEN)}$

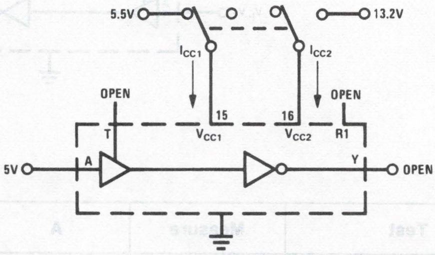
T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V


OPEN
5.5V
OPEN
OPEN
15
16
V_{CC1}
V_{CC2}
R1
−5V
A
Y
I_{OS}

TL/F/5795-6

Each output is tested separately.

FIGURE 4. I_{OS}

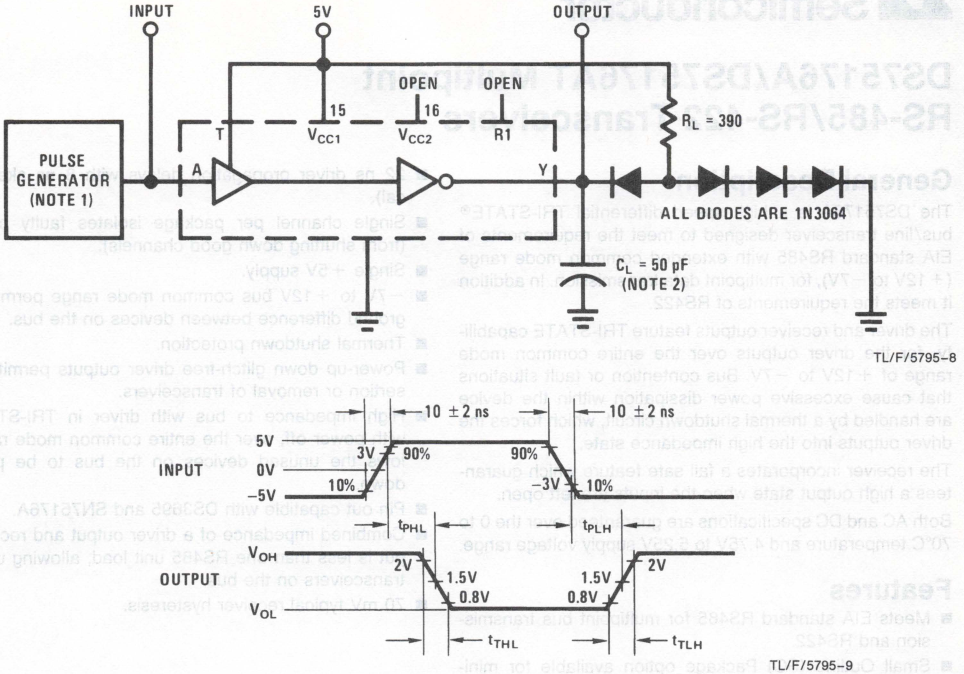

5.5V
13.2V
I_{CC1}
I_{CC2}
OPEN
OPEN
15
16
T
V_{CC1}
V_{CC2}
R1
5V
A
Y
OPEN

TL/F/5795-7

All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms


INPUT
5V
OUTPUT
OPEN
OPEN
15
16
T
V_{CC1}
V_{CC2}
R1
R_L = 390
PULSE
GENERATOR
(NOTE 1)
A
Y
ALL DIODES ARE 1N3064
C_L = 50 pF
(NOTE 2)
10 ±2 ns
10 ±2 ns
5V
3V
90%
90%
INPUT
0V
−3V
10%
10%
−5V
t_{PHL}
t_{PLH}
V_{OH}
2V
2V
OUTPUT
1.5V
1.5V
0.8V
0.8V
V_{OL}
t_{THL}
t_{TLH}

TL/F/5795-8

TL/F/5795-9

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_W = 200$ ns, duty cycle ≤ 20%.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

National Semiconductor

PRELIMINARY

DS75176A/DS75176AT Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176A is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition it meets the requirements of RS422.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

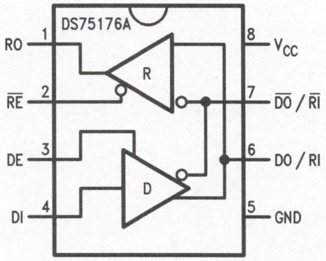
The receiver incorporates a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and RS422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays with 8 ns skew (typical).
- Single channel per package isolates faulty channels (from shutting down good channels).
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power-up down glitch-free driver outputs permit live insertion or removal of transceivers.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out capatible with DS3695 and SN75176A.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



TL/F/8759-1

Top View

Order Number DS75176AN, DS75176AM, DS75176AJ-8, DS75176ATN
See NS Package Number N08E, M08A or J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/ −10V
Receiver Input Voltages (DS75176A)	+15V/ −10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @25°C for M Package	675 mW (Note 5)
Continuous Power Dissipation @25°C (for N Package)	900 mW (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A			
DS75176A	0	+70	°C
DS75176AT	−40	+85	°C
Differential Input Voltage, VID (Note 6)		+12	V

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 4)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States						0.2	V
V_{OC}	Driver Common Mode Output Voltage		*(Figure 1)*	R = 27Ω			3.0	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$	$V_{CC} = 0V$ or 5.25V DE = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400\ \mu A$		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 7)				0.5	V
		$\overline{LF}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 7)	Driver Outputs Enabled		35	50	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics (Notes 2 and 3)

0°C $\leq T_A \leq$ 70°C, 4.75V $< V_{CC} <$ 5.25V unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 7)			−250	mA
		$V_O = +12V$ (Note 7)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5: Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.

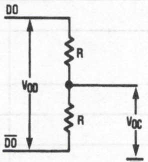
Note 6: Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Note 7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75176AT. The other parameters remain valid for −40°C $< T_A <$ +85°C.

Switching Characteristics 4.75V $\leq V_{CC} \leq$ 5.25V; 0°C $< T_A <$ 70°C

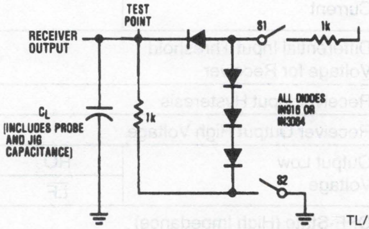
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	R_{LDIFF} = 60Ω $C_{L1} = C_{L2}$ = 100 pF *(Figures 3* and *5)*		22		ns
t_{PHL}	Driver Input to Output			22		ns
t_{SKEW}	Driver Output to Output			8		ns
t_r	Driver Rise Time	R_{LDIFF} = 60Ω $C_{L1} = C_{L2}$ = 100 pF *(Figures 3* and *5)*		10		ns
t_f	Driver Fall Time			10		ns
t_{ZH}	Driver Enable to Output High	C_L = 100 pF *(Figures 4* and *6)* S1 Open		35		ns
t_{ZL}	Driver Enable to Output Low	C_L = 100 pF *(Figures 4* and *6)* S2 Open		35		ns
t_{LZ}	Driver Disable Time from Low	C_L = 15 pF *(Figures 4* and *6)* S2 Open		15		ns
t_{HZ}	Driver Disable Time from High	C_L = 15 pF *(Figures 4* and *6)* S1 Open		15		ns
t_{PLH}	Receiver Input to Output	C_L = 15 pF *(Figures 2* and *7)* S1 and S2 Closed		25		ns
t_{PHL}	Receiver Input to Output			25		ns
t_{ZL}	Receiver Enable to Output Low	C_L = 15 pF *(Figures 2* and *8)* S2 Open		15		ns
t_{ZH}	Receiver Enable to Output High	C_L = 15 pF *(Figures 2* and *8)* S1 Open		15		ns
t_{LZ}	Receiver Disable from Low	C_L = 15 pF *(Figures 2* and *8)* S2 Open		12		ns
t_{HZ}	Receiver Disable from High	C_L = 15 pF *(Figures 2* and *8)* S1 Open		12		ns

AC Test Circuits



TL/F/8759-2

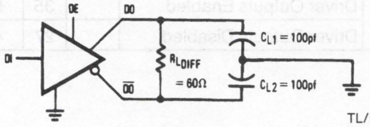
FIGURE 1


TEST POINT
RECEIVER OUTPUT
S1
1k
C_L (INCLUDES PROBE AND JIG CAPACITANCE)
1k
ALL DIODES 1N916 OR 1N3064
S2

TL/F/8759-3

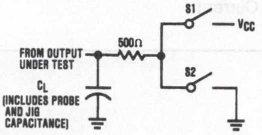
Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2



TL/F/8759-4

FIGURE 3

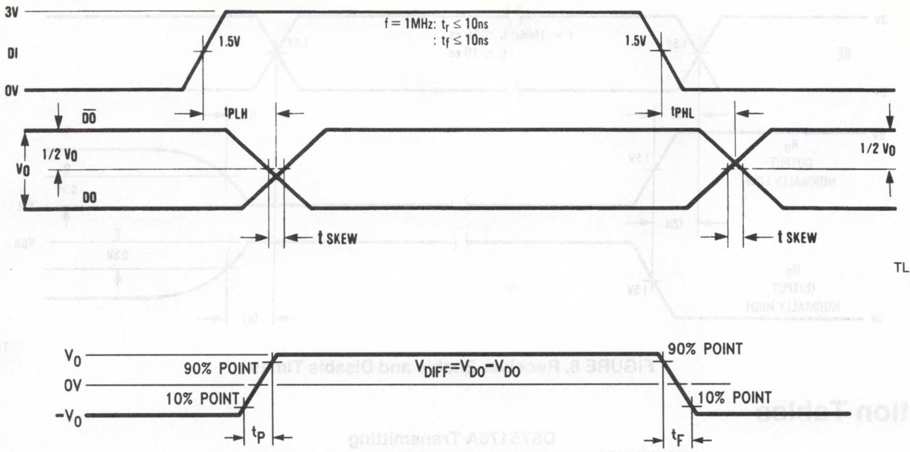


TL/F/8759-5

Note: Unless otherwise specified the switches are closed.

FIGURE 4

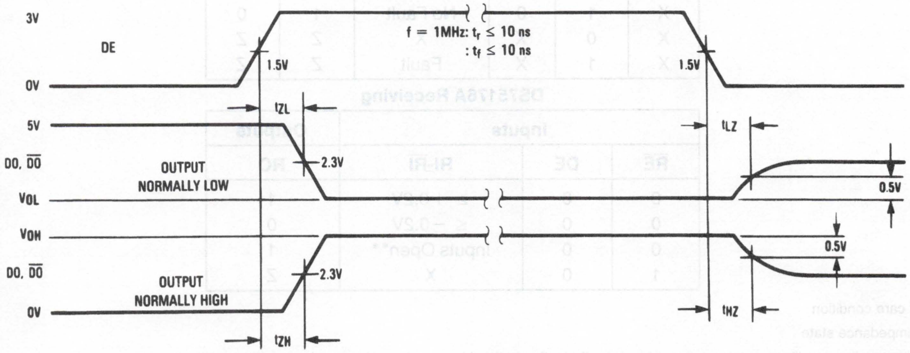
Switching Time Waveforms


3V
DI
0V
f = 1MHz: $t_r \leq 10ns$
: $t_f \leq 10ns$
1.5V
1.5V
$\overline{DO}$
t_{PLH}
t_{PHL}
1/2 V_O
V_O
DO
1/2 V_O
t SKEW
t SKEW
V_O
0V
$-V_O$
90% POINT
10% POINT
$V_{DIFF}=V_{DO}-V_{\overline{DO}}$
90% POINT
10% POINT
t_P
t_F

TL/F/8759-6

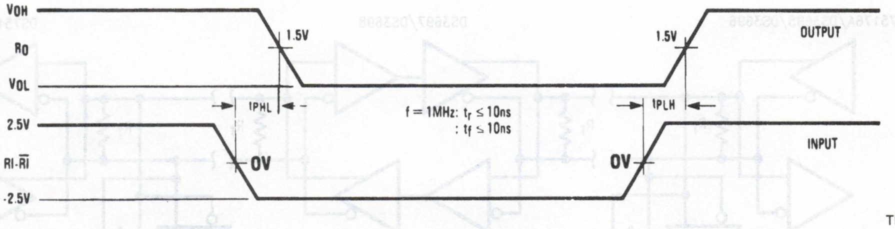
TL/F/8759-10

FIGURE 5. Driver Propagation Delays


3V
DE
0V
f = 1MHz: $t_r \leq 10$ ns
: $t_f \leq 10$ ns
1.5V
1.5V
t_{ZL}
t_{LZ}
5V
DO, $\overline{DO}$
OUTPUT
NORMALLY LOW
2.3V
V_{OL}
0.5V
V_{OH}
0.5V
DO, $\overline{DO}$
OUTPUT
NORMALLY HIGH
2.3V
0V
t_{HZ}
t_{ZH}

TL/F/8759-7

FIGURE 6. Driver Enable and Disable Times

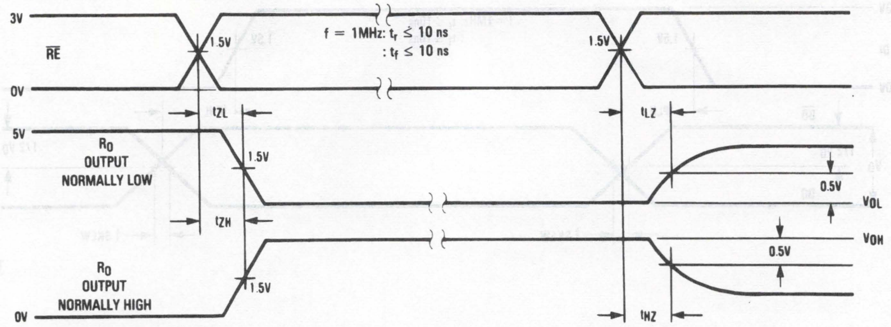

V_{OH}
RO
V_{OL}
1.5V
1.5V
OUTPUT
t_{PHL}
t_{PLH}
f = 1MHz: $t_r \leq 10ns$
: $t_f \leq 10ns$
2.5V
RI-$\overline{RI}$
0V
0V
INPUT
-2.5V

TL/F/8759-8

Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)



TL/F/8759-9

FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS75176A Transmitting

Inputs			Line Condition	Outputs	
$\overline{\text{RE}}$	DE	DI		$\overline{\text{DO}}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176A Receiving

Inputs			Outputs
$\overline{\text{RE}}$	DE	RI-$\overline{\text{RI}}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
0	0	Inputs Open**	1
1	0	X	Z

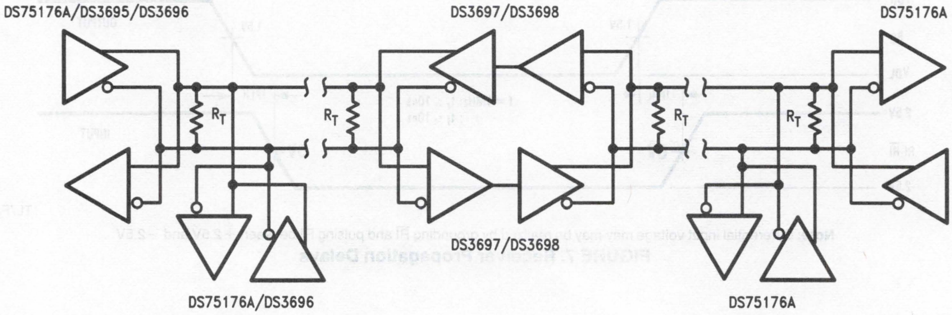
X — Don't care condition

Z — High impedance state

Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations

**This is a fail safe condition

Typical Application


DS75176A/DS3695/DS3696
DS3697/DS3698
DS75176A
R_T
R_T
R_T
R_T
DS3697/DS3698
DS75176A/DS3696
DS75176A

TL/F/8759-11

National Semiconductor

DS7820/DS8820 Dual Line Receiver

General Description

The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

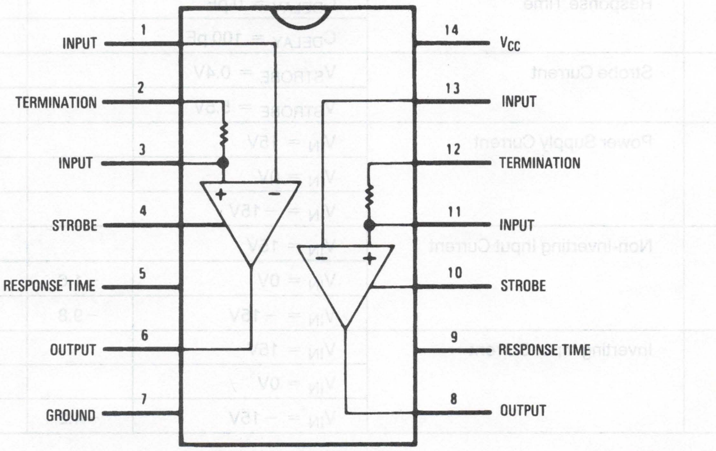
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fan out of two with TTL integrated circuits
- Strobe low forces output to "1" state

Connection Diagram

Dual-In-Line Package


INPUT
1
TERMINATION
2
INPUT
3
STROBE
4
RESPONSE TIME
5
OUTPUT
6
GROUND
7
14
V_{CC}
13
INPUT
12
TERMINATION
11
INPUT
10
STROBE
9
RESPONSE TIME
8
OUTPUT
+
−
TL/F/5796-2

Top View

Order Number DS7820J, DS8820J or DS8820N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input Threshold Voltage	$V_{CM} = 0V$	−0.5	0	0.5	V
		$-15V \leq V_{CM} \leq 15V$	−1.0	0	1.0	V
V_{OH}	High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
V_{OL}	Low Output Level	$I_{SINK} \leq 3.5$ mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
t_r	Response Time	$C_{DELAY} = 0$ pF		40		ns
		$C_{DELAY} = 100$ pF		150		ns
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		−1.0	−1.4	mA
		$V_{STROBE} = 5.5V$			5.0	μA
I_{CC}	Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
		$V_{IN} = 0V$		5.8	10.2	mA
		$V_{IN} = -15V$		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
		$V_{IN} = 0V$	−1.6	−1.0		mA
		$V_{IN} = -15V$	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
		$V_{IN} = 0V$		0	−0.5	mA
		$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

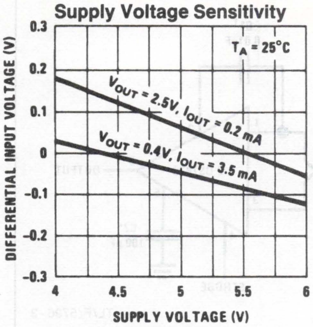
Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820 or $0°C \leq T_A \leq +70°C$ for the DS8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

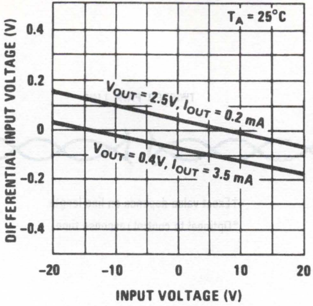
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

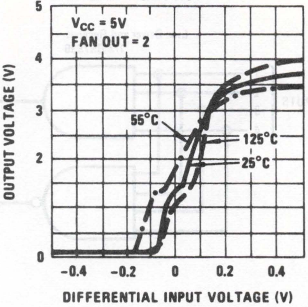
Supply Voltage Sensitivity



Common Mode Rejection

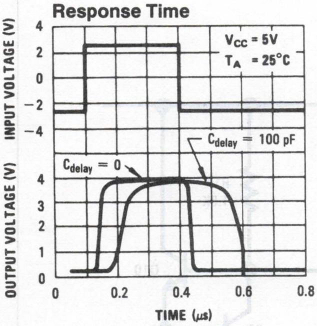


Transfer Function

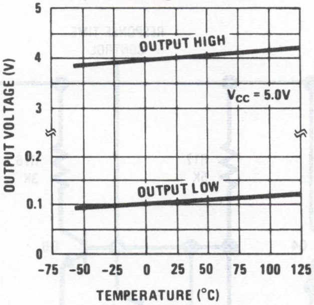


TL/F/5796-4

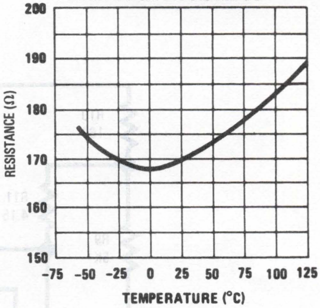
Response Time



Output Voltage Levels

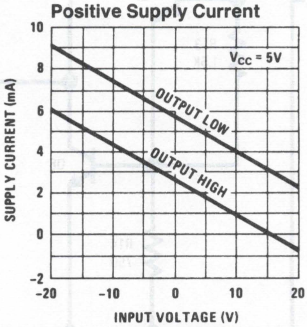


Termination Resistance

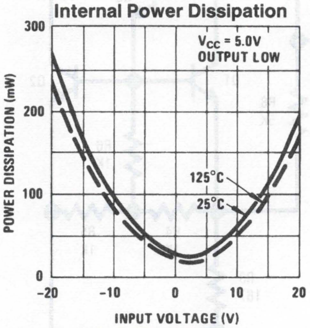


TL/F/5796-5

Positive Supply Current

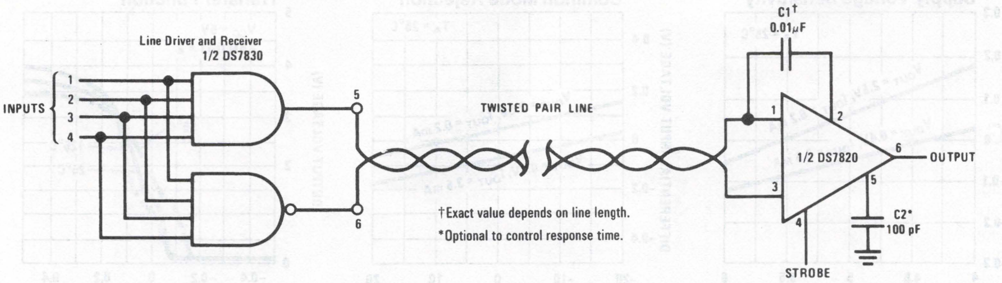


Internal Power Dissipation



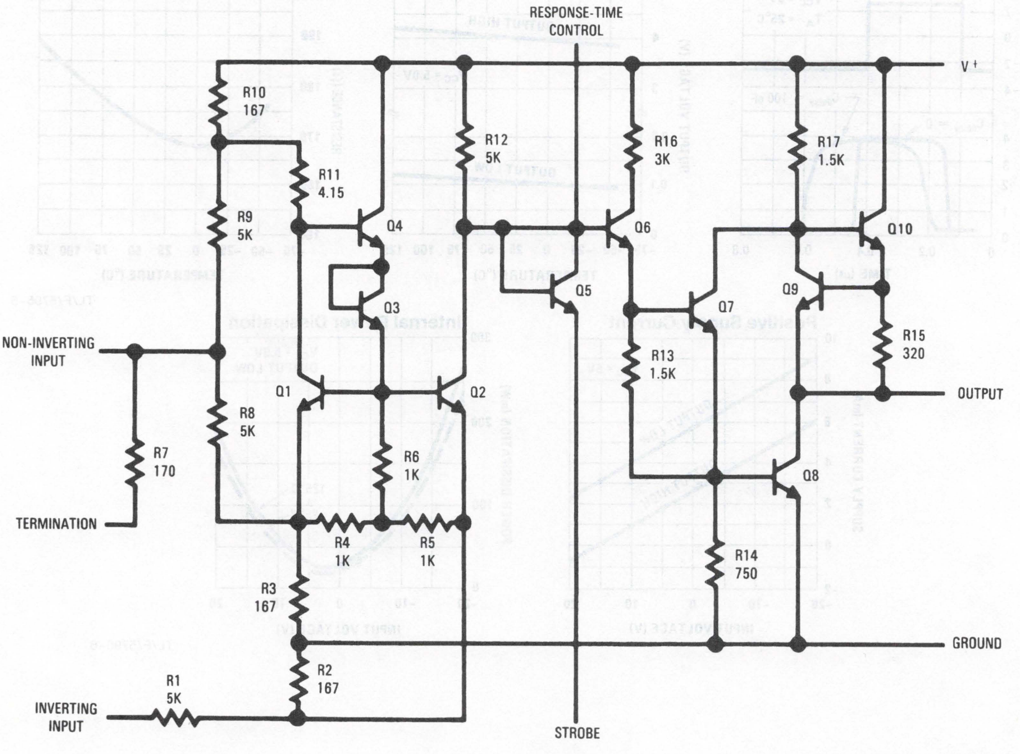
TL/F/5796-6

Typical Application


Line Driver and Receiver
1/2 DS7830
INPUTS
1
2
3
4
5
6
TWISTED PAIR LINE
†Exact value depends on line length.
*Optional to control response time.
C1†
0.01μF
1
2
3
4
5
6
1/2 DS7820
OUTPUT
C2*
100 pF
STROBE

TL/F/5796–3

Schematic Diagram


RESPONSE-TIME
CONTROL
V+
R10
167
R11
4.15
R9
5K
Q4
Q3
R12
5K
Q5
R16
3K
Q6
R17
1.5K
Q10
Q9
Q7
R15
320
NON-INVERTING
INPUT
Q1
Q2
R8
5K
R7
170
R6
1K
R13
1.5K
OUTPUT
Q8
TERMINATION
R4
1K
R5
1K
R3
167
R14
750
GROUND
R2
167
R1
5K
INVERTING
INPUT
STROBE

TL/F/5796–1

National Semiconductor

DS7820A/DS8820A Dual Line Receiver

General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

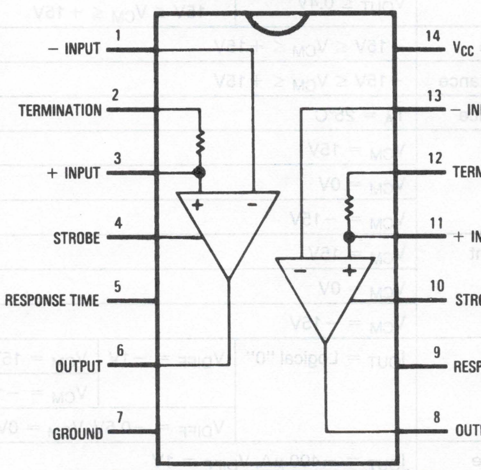
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to +125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

Connection Diagram

Dual-In-Line Package



Note: Pin 7 connected to bottom of cavity package.

TL/F/5797–2

Top View

Order Number DS7820AJ, DS8820AJ or DS8820AN
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$	$-3V \leq V_{CM} \leq +3V$			0.06	0.5	V
			$-15V \leq V_{CM} \leq +15V$			0.06	1.0	V
		$I_{OUT} = +16\ mA$, $V_{OUT} \leq 0.4V$	$-3V \leq V_{CM} \leq +3V$			−0.08	−0.5	V
			$-15V \leq V_{CM} \leq +15V$			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$			120	170	250	Ω
I_I^-	Inverting Input Current	$V_{CM} = 15V$				3.0	4.2	mA
		$V_{CM} = 0V$				0	−0.5	mA
		$V_{CM} = -15V$				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	$V_{CM} = 15V$				5.0	7.0	mA
		$V_{CM} = 0V$				−1.0	−1.6	mA
		$V_{CM} = -15V$				−7.0	−9.8	mA
I_{CC}	Power Supply Current One Side Only	I_{OUT} = Logical "0"	$V_{DIFF} = -1V$	$V_{CM} = 15V$		3.9	6.0	mA
				$V_{CM} = -15V$		9.2	14.0	mA
			$V_{DIFF} = -0.5V$, $V_{CM} = 0V$			6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\ \mu A$, $V_{DIFF} = 1V$			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = +16\ mA$, $V_{DIFF} = -1V$			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	$I_{OUT} = +16\ mA$, $V_{OUT} \leq 0.4V$, $V_{DIFF} = -3V$			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$, $V_{DIFF} = -3V$					0.9	V
I_{SH}	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$			−2.8	−4.5	−6.7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820A or $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq +70°C$ for the DS8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

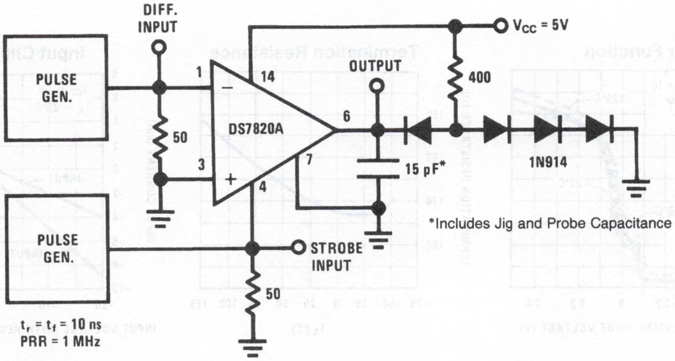
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

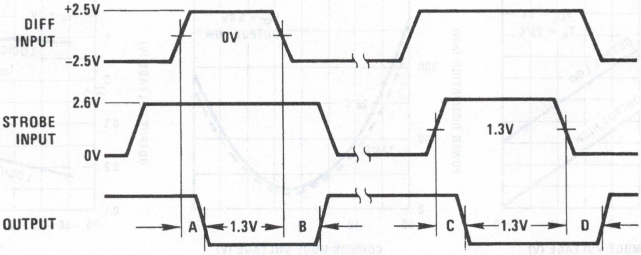
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay, Differential Input to "0" Output	$R_L = 400\ \Omega$, $C_L = 15\ pF$, see *Figure 1*		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

AC Test Circuit and Waveforms


DIFF. INPUT
PULSE GEN.
1
14
−
50
DS7820A
3
+
4
7
6
OUTPUT
400
V_{CC} = 5V
15 pF*
1N914
STROBE INPUT
PULSE GEN.
50
$t_r = t_f = 10\ ns$
PRR = 1 MHz

*Includes Jig and Probe Capacitance

TL/F/5797-7


+2.5V
DIFF INPUT
−2.5V
0V
2.6V
STROBE INPUT
0V
1.3V
OUTPUT
A
1.3V
B
C
1.3V
D

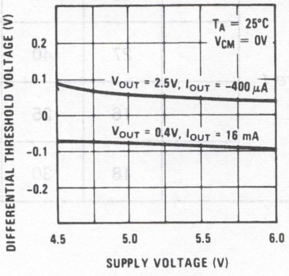
TL/F/5797-8

A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

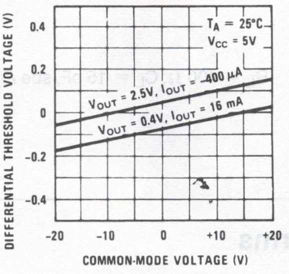
FIGURE 1

Typical Performance Characteristics (Note 3)

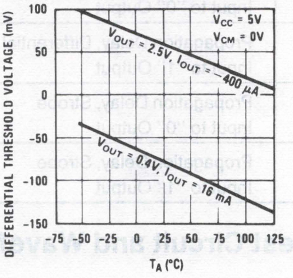
Supply Voltage Sensitivity



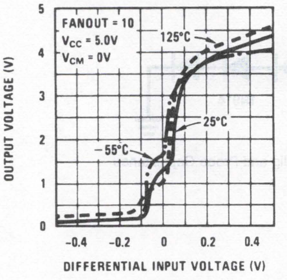
Common-Mode Voltage Sensitivity



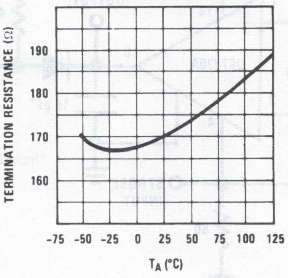
Temperature Sensitivity



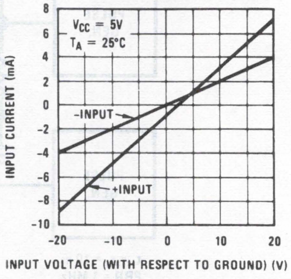
Transfer Function



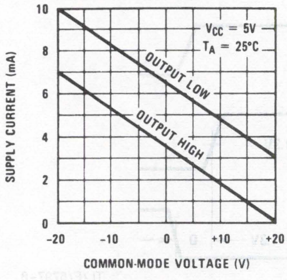
Termination Resistance



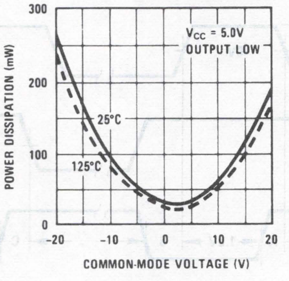
Input Characteristics



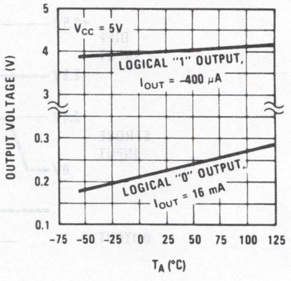
Power Supply Current



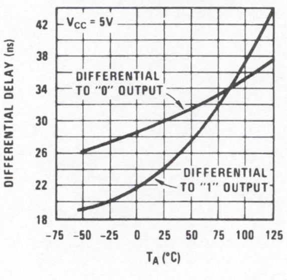
Internal Power Dissipation



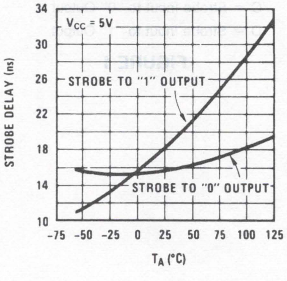
Output Voltage Levels



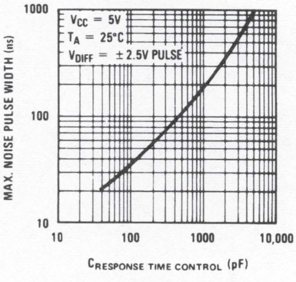
Differential Input Delays



Strobe Delays

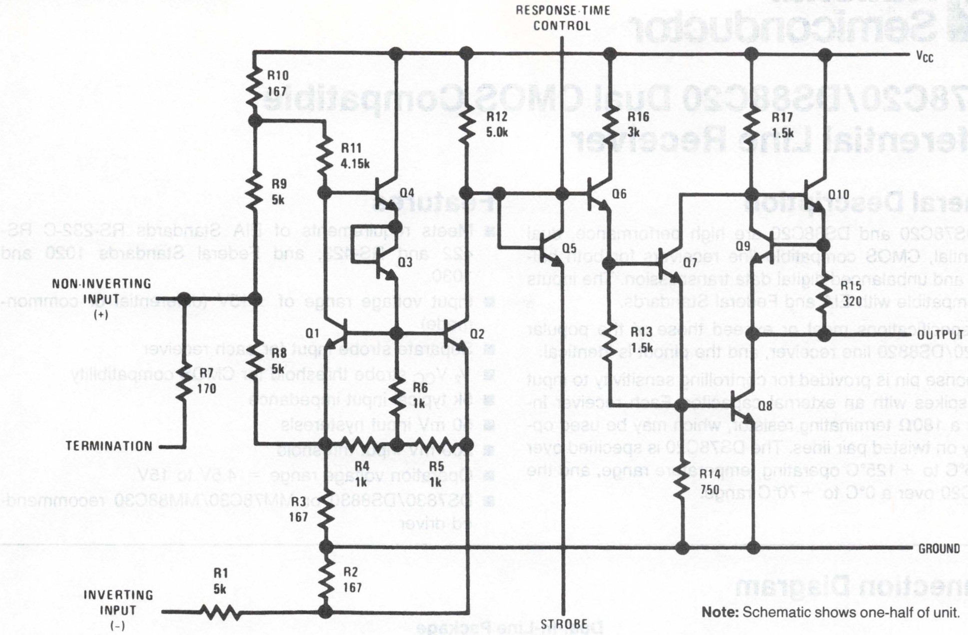


Noise Rejection



TL/F/5797-6

Schematic Diagram

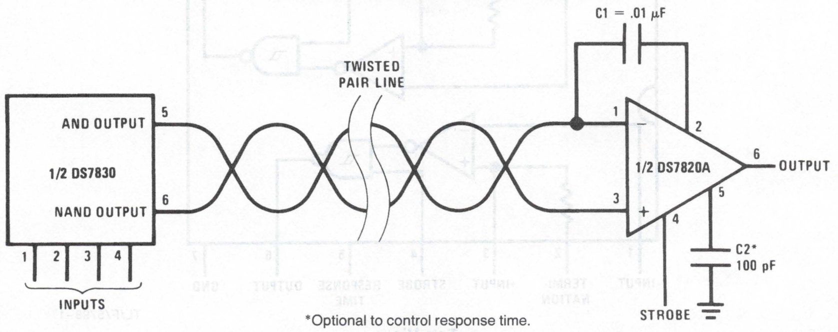

RESPONSE-TIME
CONTROL
V$_{CC}$
R10
167
R11
4.15k
R12
5.0k
R16
3k
R17
1.5k
R9
5k
Q4
Q6
Q10
Q5
Q3
Q9
Q7
NON-INVERTING
INPUT
(+)
R15
320
Q1
Q2
R13
1.5k
OUTPUT
R8
5k
R7
170
R6
1k
Q8
TERMINATION
R4
1k
R5
1k
R14
750
R3
167
GROUND
R1
5k
R2
167
INVERTING
INPUT
(−)
STROBE

Note: Schematic shows one-half of unit.

TL/F/5797-1

Typical Applications

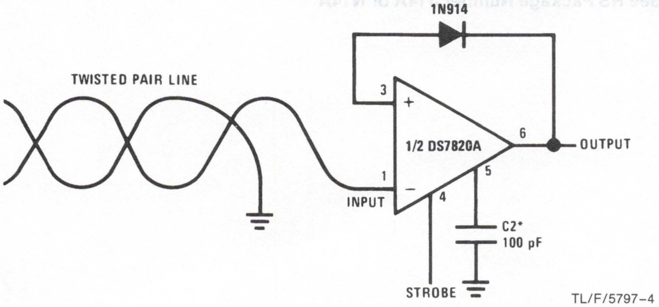
Differential Line Driver and Receiver


C1 = .01 μF
TWISTED
PAIR LINE
AND OUTPUT
5
1/2 DS7830
NAND OUTPUT
6
1
2
3
4
INPUTS
1
−
2
1/2 DS7820A
6
OUTPUT
3
+
5
4
C2*
100 pF
STROBE

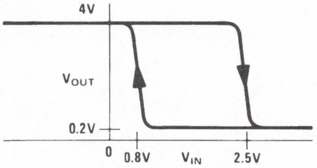
*Optional to control response time.

TL/F/5797-3

Single Ended (EIA-RS232C) Receiver with Hysteresis


1N914
TWISTED PAIR LINE
3
+
1/2 DS7820A
6
OUTPUT
1
5
INPUT
−
4
C2*
100 pF
STROBE

TL/F/5797-4



TL/F/5797-5

(Output = "1" for Open Input)

National Semiconductor

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

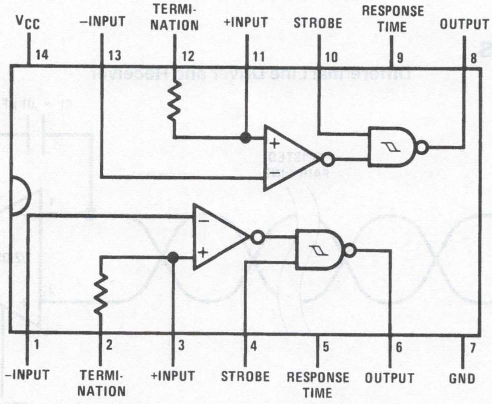
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package



TL/F/5798–1

Top View

Order Number DS78C20J, DS88C20J or DS88C20N

See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-10V \leq V_{CM} \leq 10V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$	$-10V \leq V_{CM} \leq 10V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$			5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$			2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA$, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq 15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$	$V_{CC} = 15V$		15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$	$V_{CC} = 15V$		−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$I_{OUT} = 1.6\ mA$, $V_{OL} \leq 0.5V$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -200\ \mu A$, $V_{OH} = V_{CC} - 1.2V$	$V_{CC} = 5V$		2.5	1.5	V
			$V_{CC} = 10V$		5.0	2.0	V
			$V_{CC} = 15V$		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 15V$, $V_{STROBE} = 0V$, (Note 4)		−5	−20	−40	mA

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	$C_L = 50\ pF$		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	$C_L = 50\ pF$		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$C_L = 50\ pF$		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$C_L = 50\ pF$		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

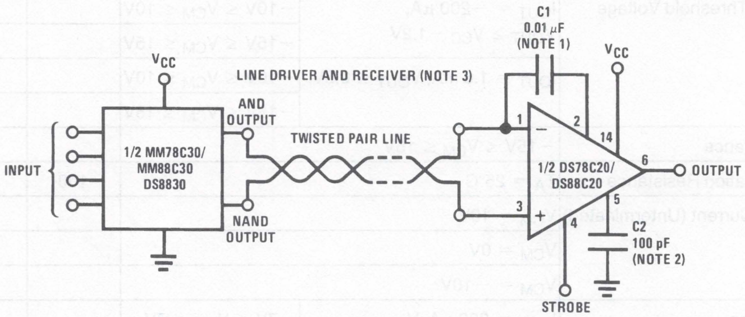
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

Typical Applications

RS-422/RS-423 Application


C1
0.01 µF
(NOTE 1)
VCC
LINE DRIVER AND RECEIVER (NOTE 3)
VCC
AND OUTPUT
INPUT
1/2 MM78C30/ MM88C30 DS8830
TWISTED PAIR LINE
NAND OUTPUT
1
2
14
1/2 DS78C20/ DS88C20
6
OUTPUT
3
5
4
C2
100 pF
(NOTE 2)
STROBE

TL/F/5798-2

Note 1: (Optional internal termination resistor.)

a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

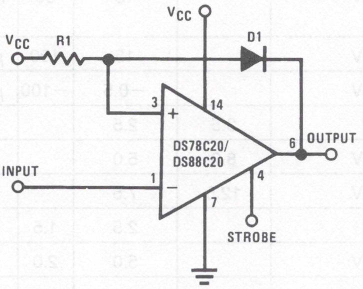
c) Pin 2 open; no internal line termination.

d) Transmission line may be terminated elsewhere or not at all.

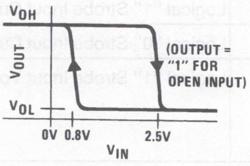
Note 2: Optional to control response time.

Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to applicaton notes AN-22, AN-83 and AN-108.

RS-232-C Application with Hysteresis


VCC
VCC
R1
D1
3
+
14
DS78C20/ DS88C20
6
OUTPUT
INPUT
1
−
4
7
STROBE

V_{CC}	R1 ±5%
5V	4,3 kΩ
10V	15 kΩ
15V	24 kΩ

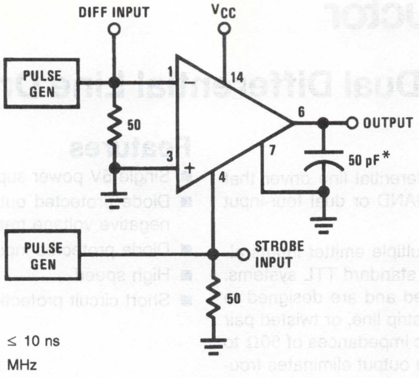


TL/F/5798-4

TL/F/5798-3

For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

AC Test Circuit

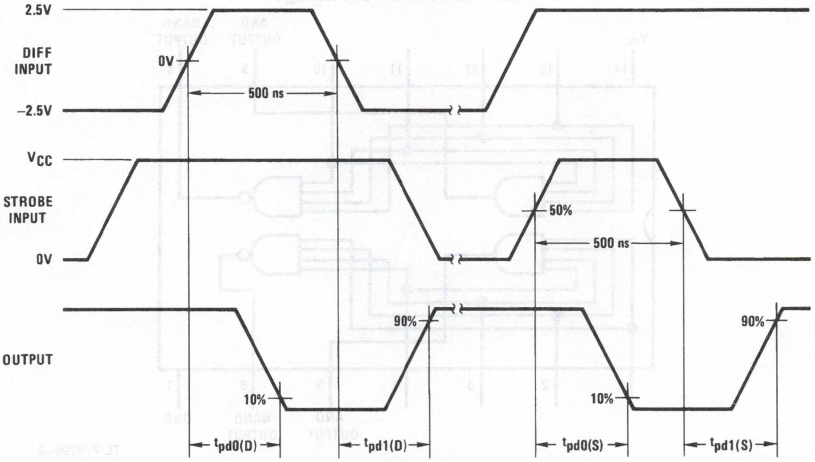

DIFF INPUT
V_{CC}
PULSE GEN
1
14
50
6
OUTPUT
3
7
50 pF*
4
PULSE GEN
STROBE INPUT
50

$t_r = t_f = \leq 10$ ns
PRR = 1 MHz

TL/F/5798-5

*Includes probe and jig capacitance

Switching Time Waveforms



TL/F/5798-6

National Semiconductor

DS7830/DS8830 Dual Differential Line Driver

General Description

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

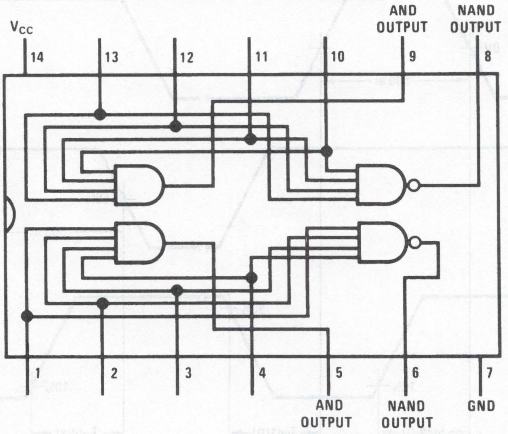
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package


V_{CC}
14
13
12
11
10
AND OUTPUT
9
NAND OUTPUT
8
1
2
3
4
5
AND OUTPUT
6
NAND OUTPUT
7
GND

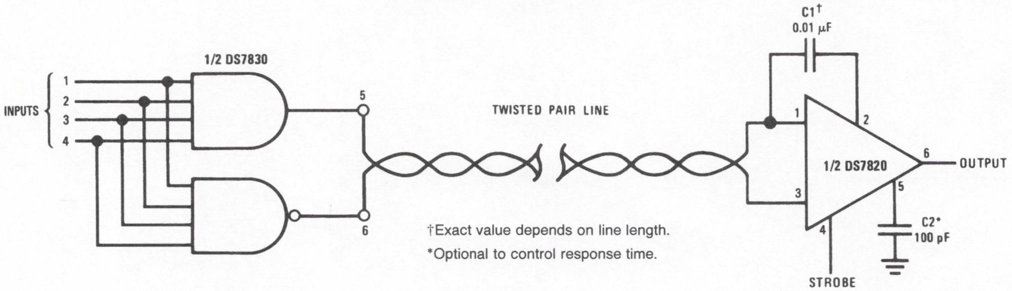
TL/F/5799-2

Top View

Order Number DS7830J, DS8830J or DS8830N
See NS Package Number J14A or N14A

Typical Application

Digital Data Transmission


C1†
0.01 µF
1/2 DS7830
INPUTS
1
2
3
4
5
6
TWISTED PAIR LINE
1
2
3
1/2 DS7820
6
OUTPUT
5
4
C2*
100 pF
STROBE

†Exact value depends on line length.

*Optional to control response time.

TL/F/5799-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8730	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$	$I_{OUT} = -0.8$ mA	2.4			V
			$I_{OUT} = 40$ mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 2.0V$	$I_{OUT} = 32$ mA		0.2	0.4	V
			$I_{OUT} = 40$ mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				120	µA
		$V_{IN} = 5.5V$				2	mA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−4.8	mA
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$, $T_A = 125°C$, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$, (Each Driver)			11	18	mA
V_I	Input Clamp	$V_{CC} = $ Min, $I_{IN} = -12$ mA			−1.0	−1.5	V

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay AND Gate	$R_L = 400\Omega$, $C_L = 15$ pF *(Figure 1)*		8	12	ns
t_{pd0}				11	18	ns
t_{pd1}	Propagation Delay NAND Gate	$R_L = 400\Omega$, $C_L = 15$ pF *(Figure 1)*		8	12	ns
t_{pd0}				5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

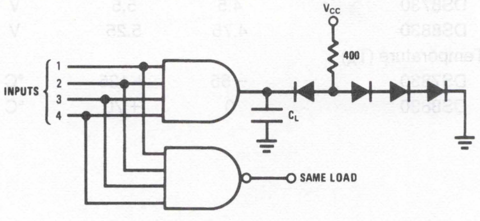
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values for $T_A = 25°C$ and $V_{CC} = 5.0V$.

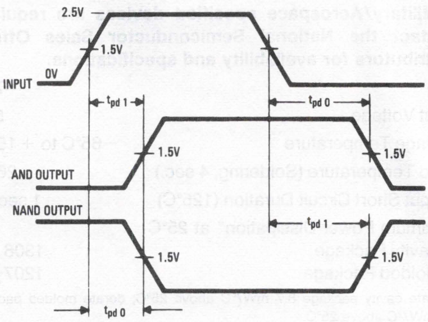
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms


V_{CC}
400
INPUTS
1
2
3
4
C_L
SAME LOAD

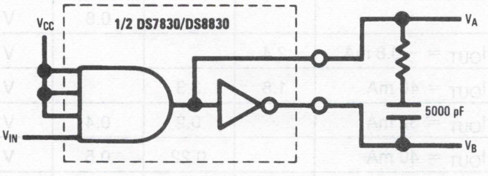
TL/F/5799-4


2.5V
1.5V
INPUT
0V
t_{pd 1}
t_{pd 0}
1.5V
1.5V
AND OUTPUT
NAND OUTPUT
t_{pd 1}
1.5V
1.5V
t_{pd 0}

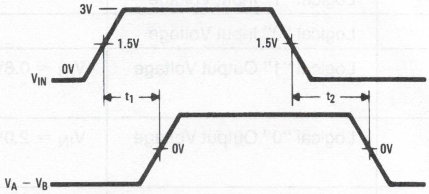
f = 1 MHz
$t_r = t_f \le 10$ ns (10% to 90%)
Duty cycle = 50%

TL/F/5799-9

FIGURE 1


V_{CC}
1/2 DS7830/DS8830
V_{IN}
V_A
5000 pF
V_B

TL/F/5799-8

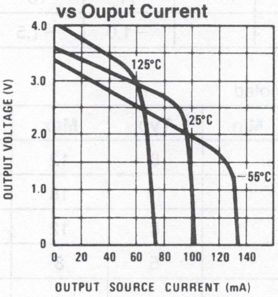

3V
1.5V
1.5V
0V
V_{IN}
t₁
t₂
0V
0V
V_A − V_B

TL/F/5799-10

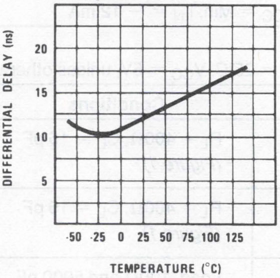
FIGURE 2

Typical Performance Characteristics

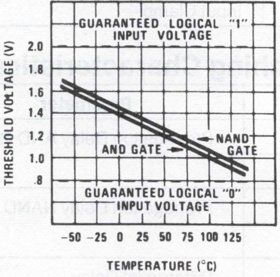
Output High Voltage (Logical "1") vs Ouput Current



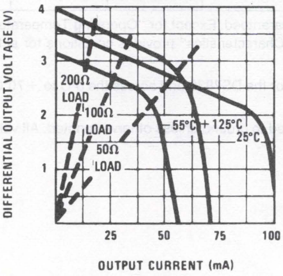
Differential Delay vs Temperature



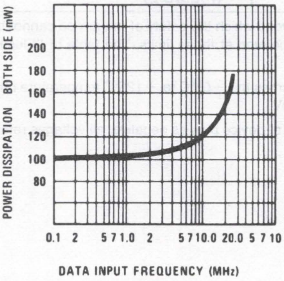
Threshold Voltage vs Temperature



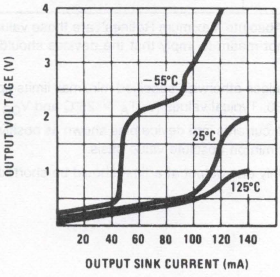
Differential Output Voltage (|V_{AND} - V_{NAND}|) vs Differential Output Current



Power Dissipation (No Load) vs Data Input Frequency

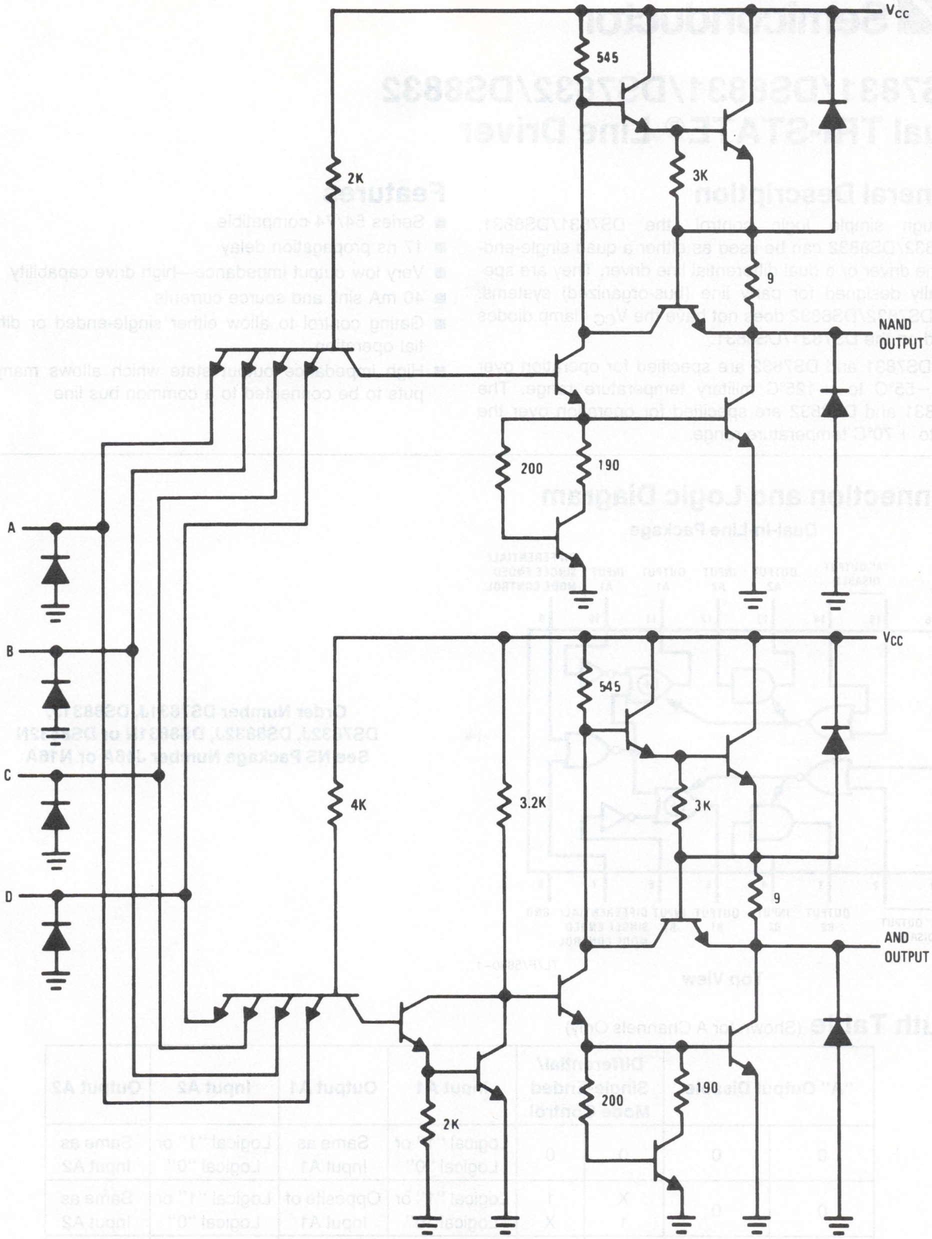


Output Low Voltage (Logical "0") vs Output Current



TL/F/5799-7

Schematic Diagram


V_CC
545
2K
3K
9
NAND OUTPUT
200
190
A
B
C
D
V_CC
545
4K
3.2K
3K
9
AND OUTPUT
190
200
2K

TL/F/5799-1

*2 Per Package

National Semiconductor

DS7831/DS8831/DS7832/DS8832 Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

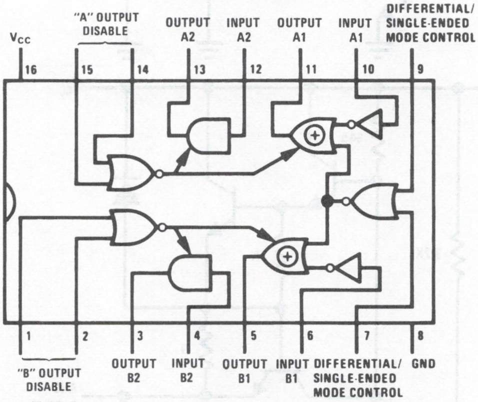
The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package


V_{CC}
"A" OUTPUT DISABLE
OUTPUT A2
INPUT A2
OUTPUT A1
INPUT A1
DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
"B" OUTPUT DISABLE
OUTPUT B2
INPUT B2
OUTPUT B1
INPUT B1
DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL
GND

TL/F/5800-1

Top View

Order Number DS7831J, DS8831J, DS7832J, DS8832J, DS8831N or DS8832N
See NS Package Number J16A or N16A

Truth Table (Shown for A Channels Only)

"A" Output Disable		Differential/ Single-Ended Mode Control		Input A1	Output A1	Input A2	Output A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High Impedance State	X	High Impedance State

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7831/DS7832	4.5	5.5	V
DS8831/DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831/DS7832	−55	+125	°C
DS8831/DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831/DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831/DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831/DS7832, V_{IN} = 5.5V				1	mA
			DS8831/DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC} + 1.5	V

Switching Characteristics $T_A = 25°C, V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	(See *Figures 4* and *5*)		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for $T_A = 125°C$ only. Only one output should be shorted at a time.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

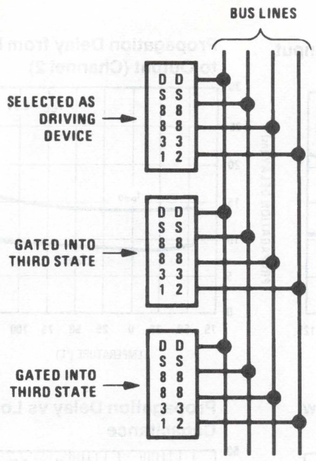
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

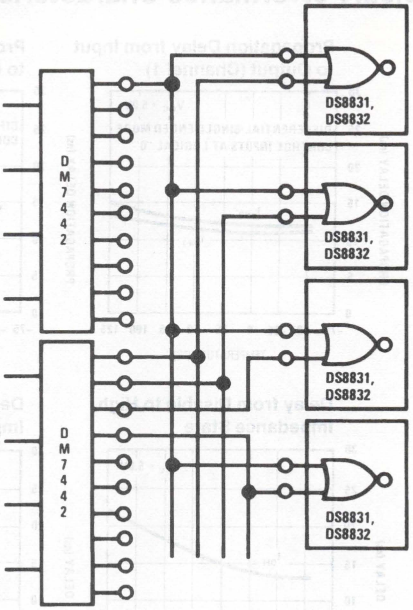
When operating in a bus-organized system with outputs tied directly to outputs of other DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.


BUS LINES
SELECTED AS DRIVING DEVICE
GATED INTO THIRD STATE
GATED INTO THIRD STATE
DS8831
DS8832
DS8831
DS8832
DS8831
DS8832

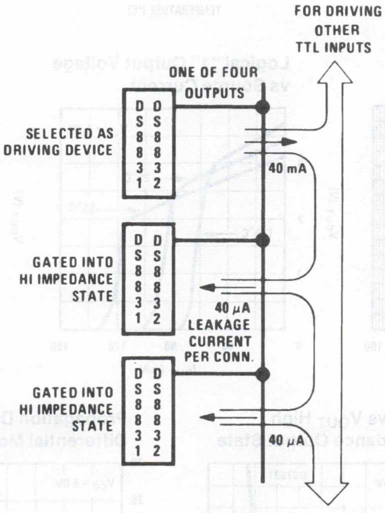
TL/F/5800-2

FIGURE 1


DM7442
DM7442
DS8831, DS8832
DS8831, DS8832
DS8831, DS8832
DS8831, DS8832

TL/F/5800-3

FIGURE 2

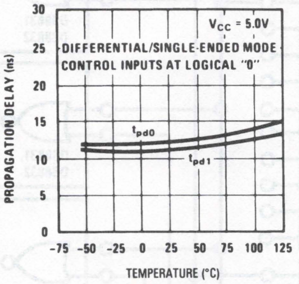

FOR DRIVING OTHER TTL INPUTS
ONE OF FOUR OUTPUTS
SELECTED AS DRIVING DEVICE
DS8831
DS8832
40 mA
GATED INTO HI IMPEDANCE STATE
DS8831
DS8832
40 μA LEAKAGE CURRENT PER CONN.
GATED INTO HI IMPEDANCE STATE
DS8831
DS8832
40 μA

TL/F/5800-4

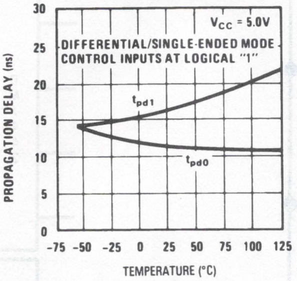
FIGURE 3

Typical Performance Characteristics

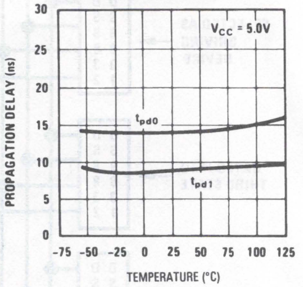
Propagation Delay from Input to Output (Channel 1)



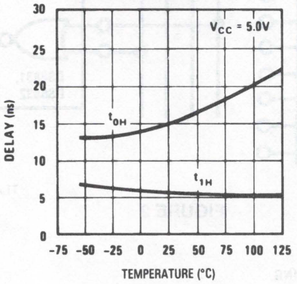
Propagation Delay from Input to Output (Channel 1)



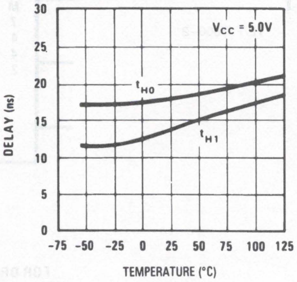
Propagation Delay from Input to Output (Channel 2)



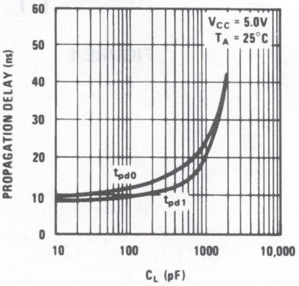
Delay from Disable to High Impedance State



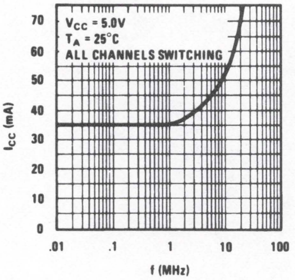
Delay from Disable to Low Impedance State



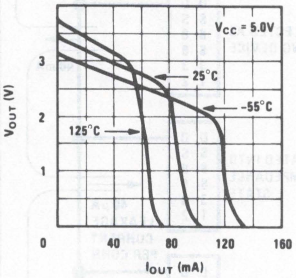
Propagation Delay vs Load Capacitance



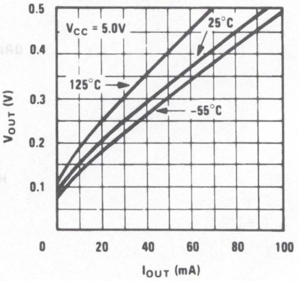
Total Supply Current vs Frequency



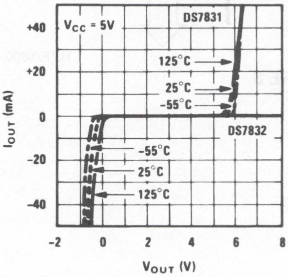
Logical "1" Output Voltage vs Source Current



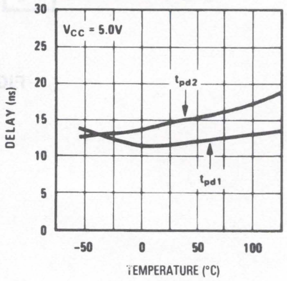
Logical "0" Output Voltage vs Sink Current



IOUT vs VOUT High Impedance Output State

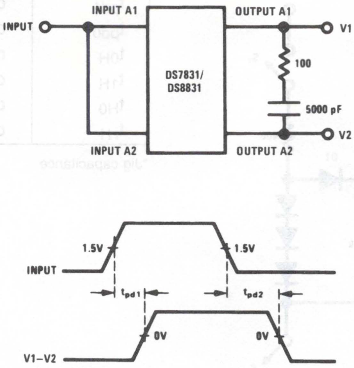


Propagation Delay in Differential Mode



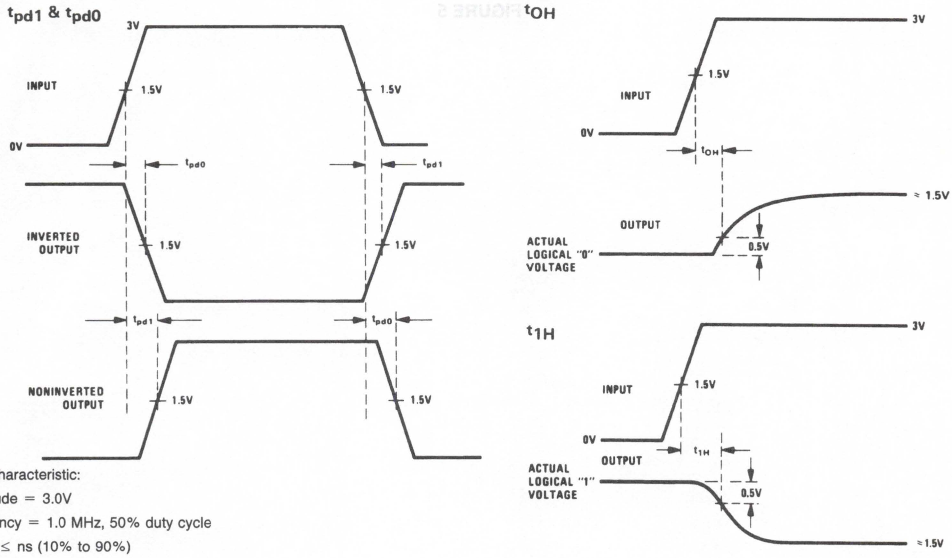
TL/F/5800-5

Typical Performance Characteristics (Continued)


INPUT
INPUT A1
OUTPUT A1
V1
DS7831/
DS8831
100
5000 pF
V2
INPUT A2
OUTPUT A2
1.5V
1.5V
INPUT
t_{pd1}
t_{pd2}
0V
0V
V1–V2

TL/F/5800-6

Switching Time Waveforms


t_{pd1} & t_{pd0}
3V
INPUT
1.5V
1.5V
0V
t_{pd0}
t_{pd1}
INVERTED
OUTPUT
1.5V
1.5V
t_{pd1}
t_{pd0}
NONINVERTED
OUTPUT
1.5V
1.5V
t_{OH}
3V
1.5V
INPUT
0V
t_{OH}
≈ 1.5V
OUTPUT
ACTUAL
LOGICAL "0"
VOLTAGE
0.5V
t_{1H}
3V
INPUT
1.5V
0V
t_{1H}
OUTPUT
ACTUAL
LOGICAL "1"
VOLTAGE
0.5V
≈ 1.5V

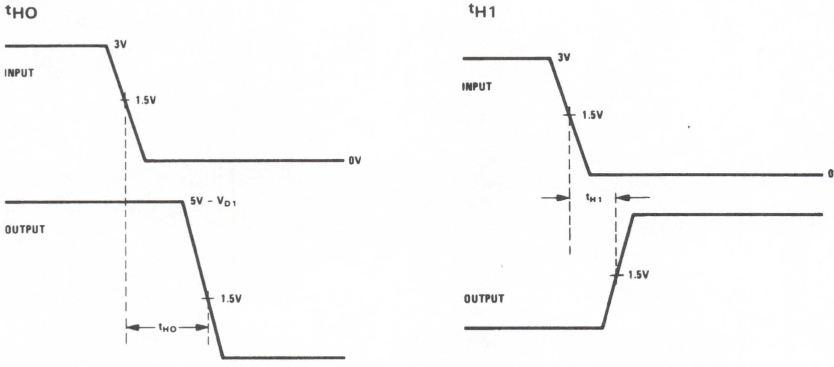
Input characteristic:

Amplitude = 3.0V

Frequency = 1.0 MHz, 50% duty cycle

$t_r = t_f \leq$ ns (10% to 90%)

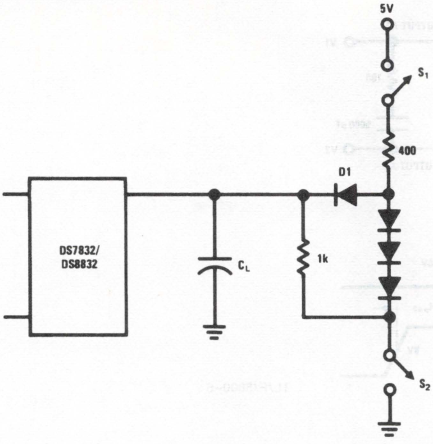
TL/F/5800-7


t_{HO}
3V
INPUT
1.5V
0V
$5V - V_{D1}$
OUTPUT
1.5V
t_{HO}
t_{H1}
3V
INPUT
1.5V
0V
t_{H1}
1.5V
OUTPUT

TL/F/5800-8

FIGURE 4

AC Load Circuit


5V
S₁
400
D1
DS7832/
DS8832
C_L
1k
S₂

TL/F/5800-9

FIGURE 5

Symbol	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	*5 pF
t_{1H}	closed	closed	*5 pF
t_{H0}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance

National Semiconductor

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

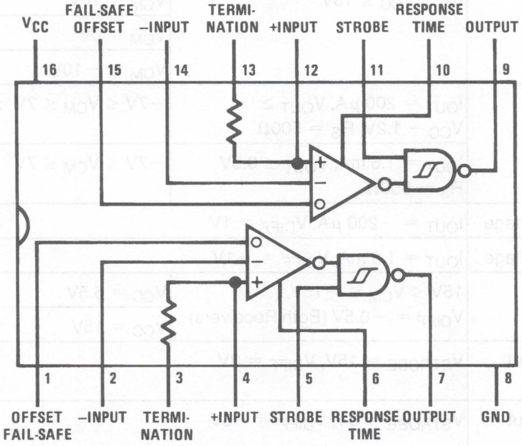
Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



VCC
FAIL-SAFE OFFSET
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
16
15
14
13
12
11
10
9
+
−
O
O
−
+
1
2
3
4
5
6
7
8
OFFSET FAIL-SAFE
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
GND

TL/F/5801–1

Top View

Order Number DS78C120J, DS88C120J or DS88C120N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 1.6$ mA, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage Fail-Safe	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	Offset = 5V	$I_{OUT} = 1.6$ mA, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	$V_{CM} = 10V$		2	3.1	mA
			$V_{CM} = 0V$		0	−0.5	mA
			$V_{CM} = -10V$		−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6$ mA, $V_{OUT} \leq 0.5V$ $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$			15	100	µA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−0.5	−100	µA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V$, $I_{OUT} = 1.6$ mA	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} V_{CC} − 1.2V, I_{OUT} = −200 μA	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

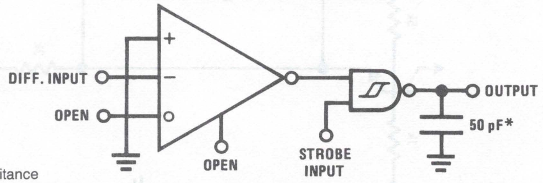
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

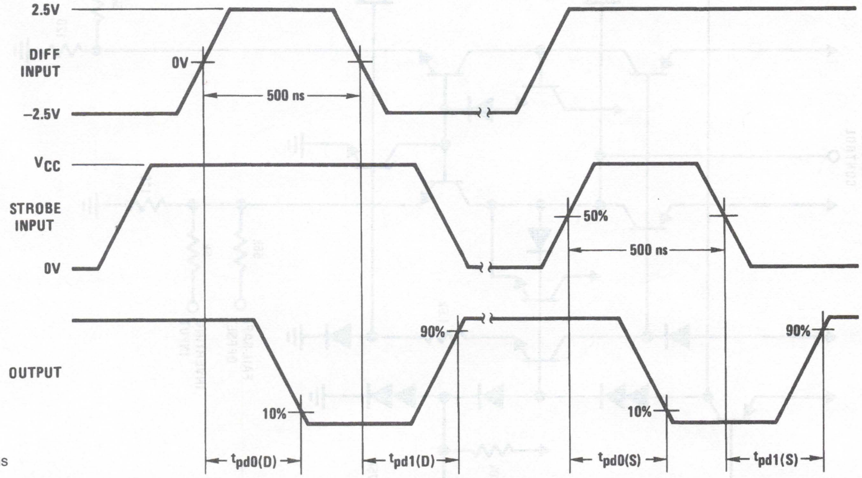
AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

TL/F/5801-3



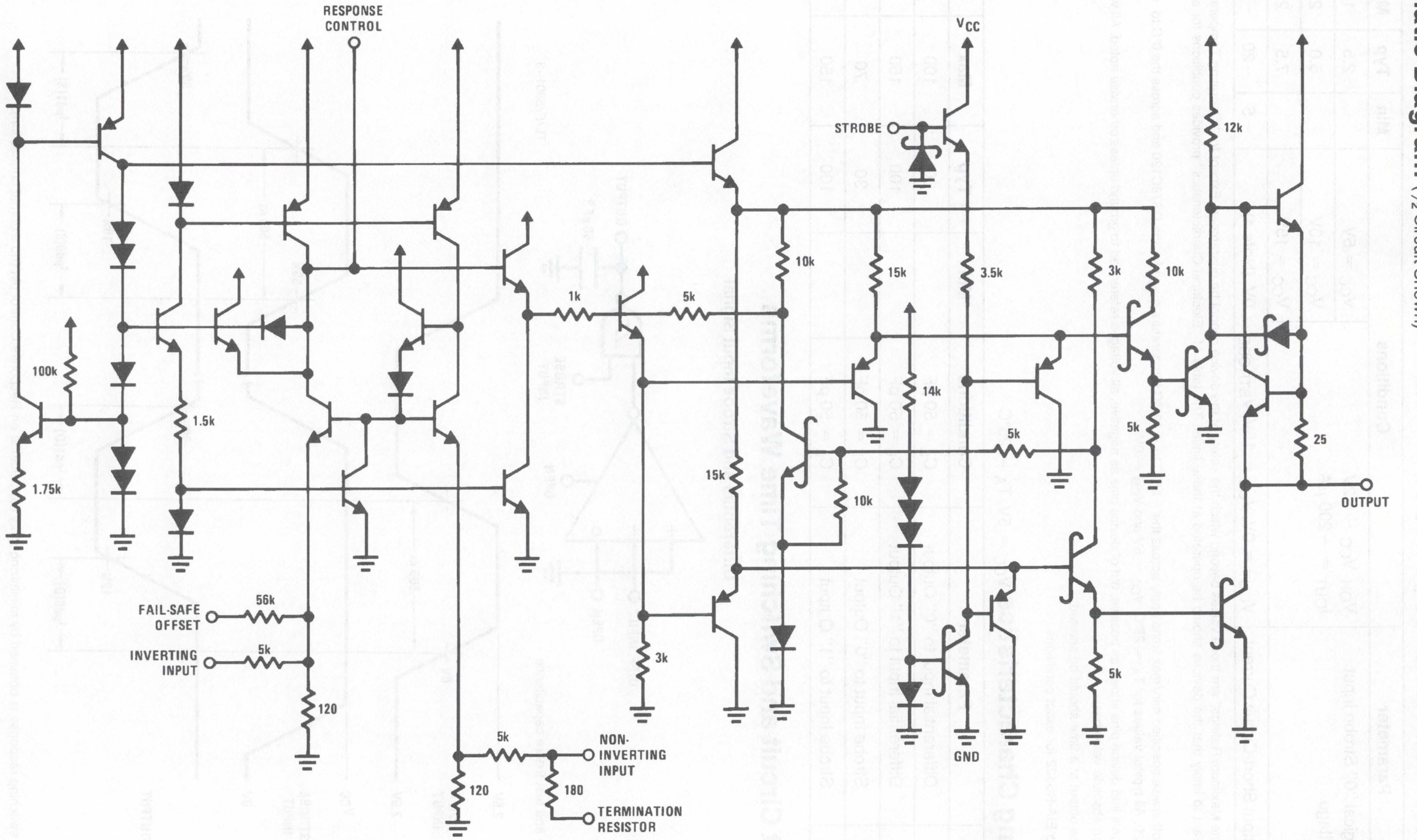
t_r = t_f ≤ 10 ns

PRR = 1 MHz

TL/F/5801-4

Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

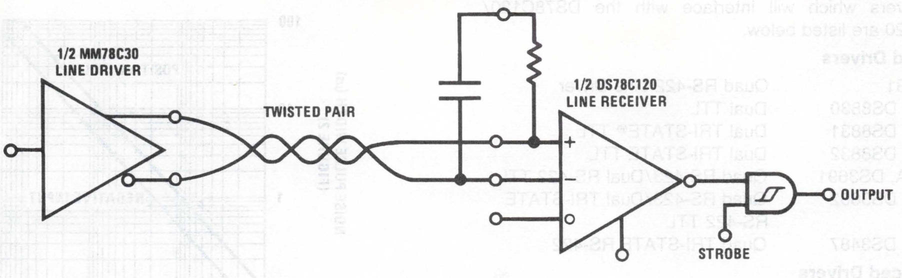
Schematic Diagram (1/2 Circuit Shown)


RESPONSE CONTROL
STROBE
V_CC
12k
10k
15k
3.5k
3k
10k
1k
5k
100k
1.5k
1.75k
14k
5k
5k
5k
25
OUTPUT
15k
10k
FAIL-SAFE OFFSET
56k
INVERTING INPUT
5k
120
3k
5k
GND
5k
NON-INVERTING INPUT
120
180
TERMINATION RESISTOR

TL/F/5801–2

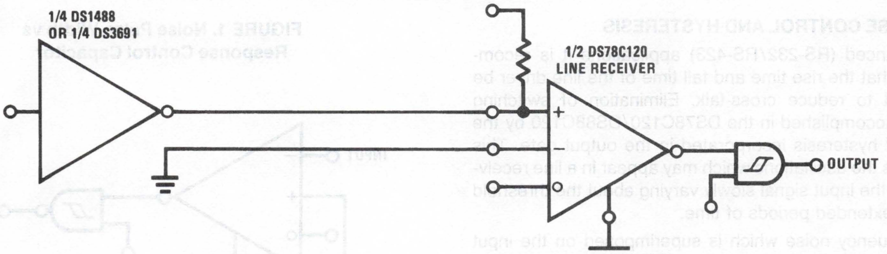
Application Hints

Balanced Data Transmission


1/2 MM78C30
LINE DRIVER
TWISTED PAIR
1/2 DS78C120
LINE RECEIVER
+
−
OUTPUT
STROBE

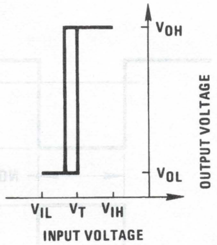
TL/F/5801-5

Unbalanced Data Transmission

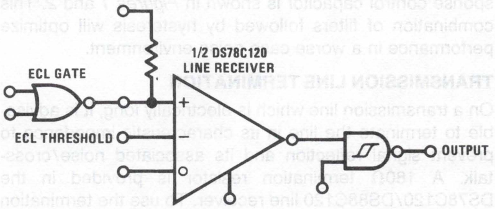

1/4 DS1488
OR 1/4 DS3691
1/2 DS78C120
LINE RECEIVER
+
−
OUTPUT

TL/F/5801-6

Logic Level Translator



TL/F/5801-7


1/2 DS78C120
LINE RECEIVER
ECL GATE
ECL THRESHOLD
+
−
OUTPUT

TL/F/58018

The DS78C120/DS88C120 may be used as a level transistor to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

Application Hints (Continued)

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3587, DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS14C88	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

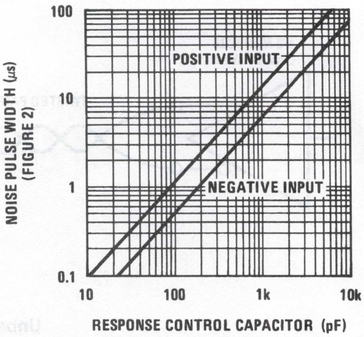
In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

TRANSMISSION LINE TERMINATION

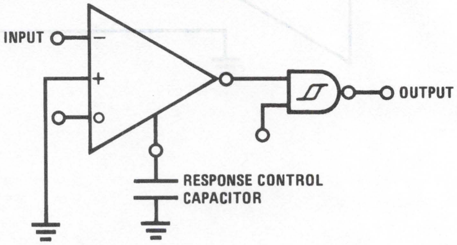
On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

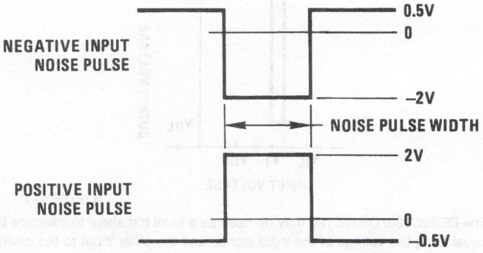


TL/F/5801–9

FIGURE 1. Noise Pulse Width vs Response Control Capacitor



TL/F/5801–10



TL/F/5801–11

FIGURE 2

Application Hints (Continued)

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to $V_{CC} = 5V$, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)} + 0.45V$ or $V_{IN(INVERTING)} + 0.9V$ when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

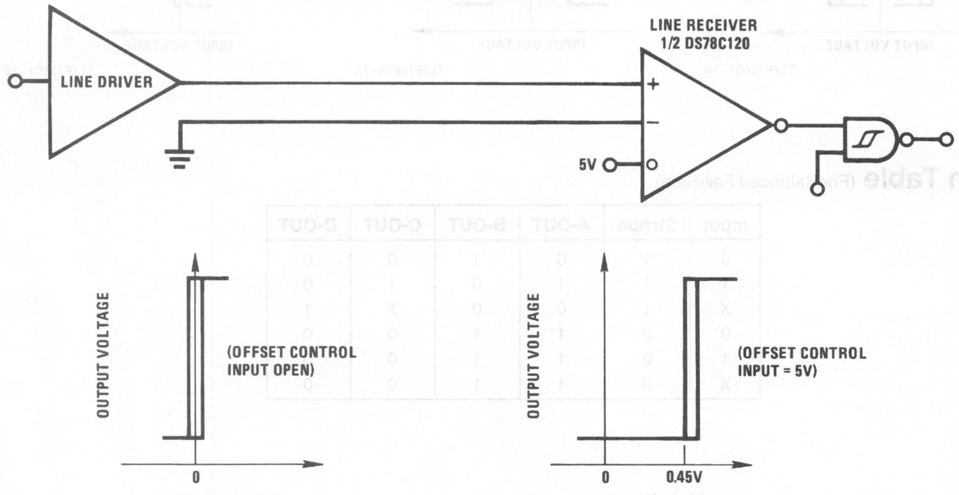
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or shorted.

For balanced operation with inputs shorted or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault condition. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

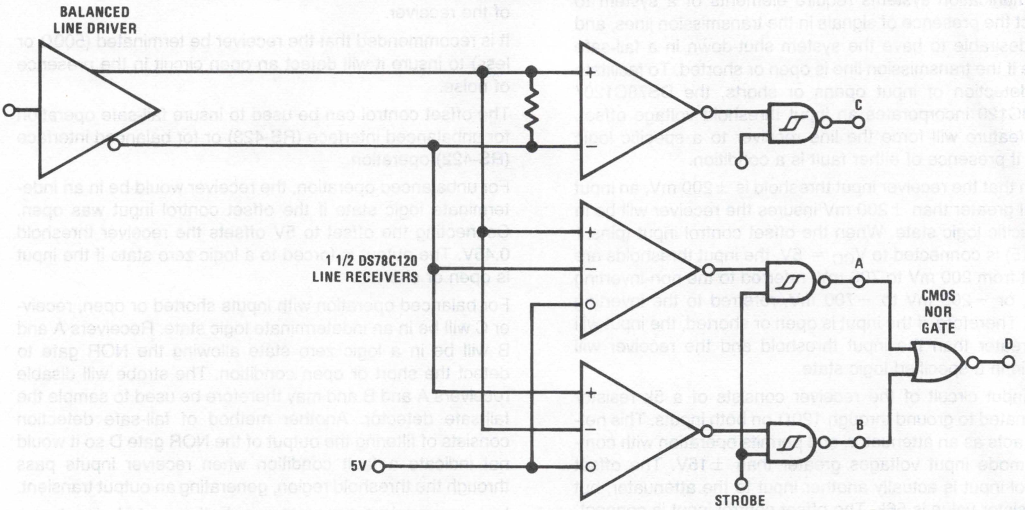
Unbalanced RS-423 and RS-232 Fail-Safe



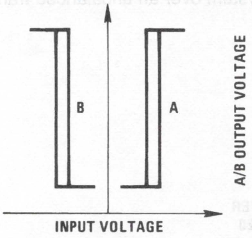
TL/F/5801–12

Application Hints (Continued)

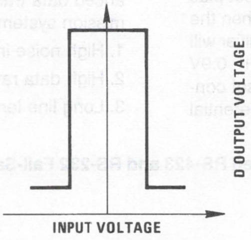
Balanced RS-422 Fail-Safe


BALANCED LINE DRIVER
+
−
C
A
B
1 1/2 DS78C120 LINE RECEIVERS
CMOS NOR GATE
D
5V
STROBE

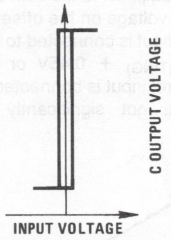
TL/F/5801-13



TL/F/5801-14



TL/F/5801-15



TL/F/5801-16

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

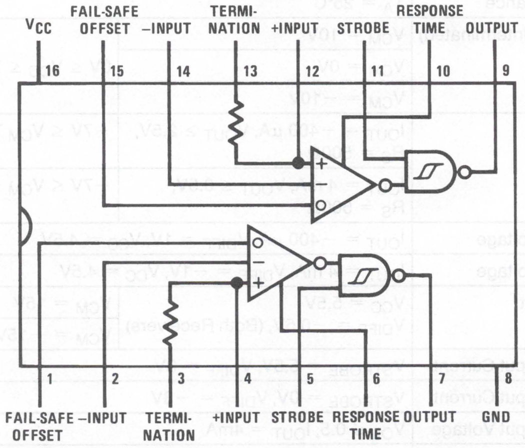
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package


V_{CC}
FAIL-SAFE OFFSET
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
FAIL-SAFE OFFSET
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
GND
TL/F/7499-1

Top View

Order Number DS78LS120J, DS88LS120J or DS88LS120N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mV
Molded Package	1362 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15 \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 4\ mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH} V_{TL}	Differential Threshold Voltage with Fail-Safe Offset = 5V	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
		$I_{OUT} = 4\ mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	−0.2	−0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 7V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$	$0V \leq V_{CC} \leq 7V$		2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$, $R_S = 500\Omega$	$-7V \leq V_{CM}$ 7V		0.1	0.4	V
		$I_{OUT} = 4\ mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\ \mu A$, $V_{DIFF} = 1V$, $V_{CC} = 4.5V$		2.5	3		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 4\ mA$, $V_{DIFF} = -1V$, $V_{CC} = 4.5V$			0.35	0.5	V
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$ $V_{DIFF} = -0.5V$, (Both Receivers)	$V_{CM} = 15V$		10	16	mA
			$V_{CM} = -15V$		10	16	mA
$I_{IN\ (1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$			1	100	μA
$I_{IN\ (0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5$, $I_{OUT} = 4mA$		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} \geq 2.5V$, I_{OUT}, $= -400\ \mu A$			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$, (Note 4)		−30	−100	−170	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

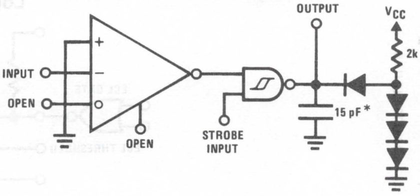
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, $C_L = 15\ pF, R_L = 2\ k\Omega$		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

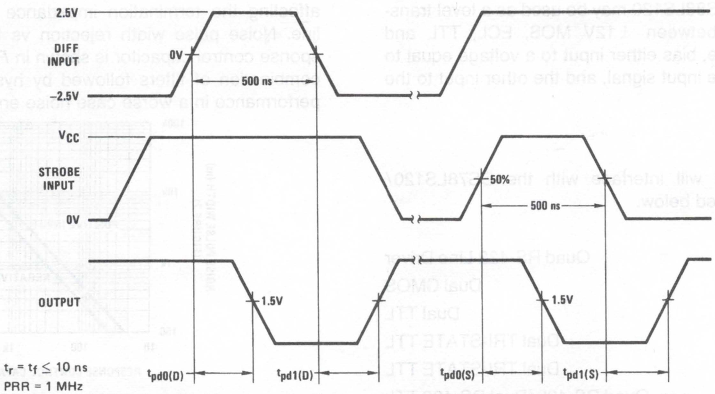
AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal


OUTPUT
VCC
2k
INPUT
OPEN
OPEN
15 pF *
STROBE
INPUT

TL/F/7499-3

*Includes probe and test fixture capacitance

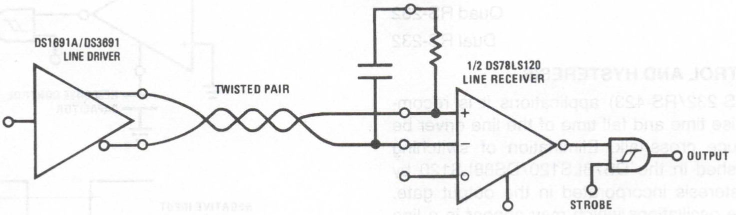


Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

TL/F/7499-4

Application Hints

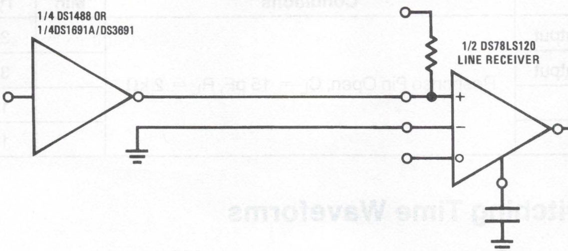
Balanced Data Transmission


DS1691A/DS3691
LINE DRIVER
TWISTED PAIR
1/2 DS78LS120
LINE RECEIVER
+
OUTPUT
STROBE

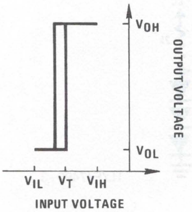
TL/F/7499-5

Application Hints (Continued)

Unbalanced Data Transmission

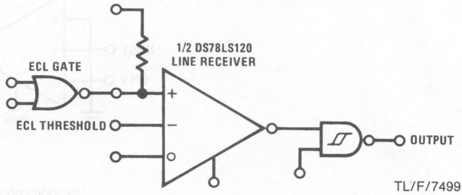

1/4 DS1488 OR
1/4DS1691A/DS3691
1/2 DS78LS120
LINE RECEIVER
+
−
OUTPUT

TL/F/7499-6



TL/F/7499-7

Logic Level Translator


ECL GATE
1/2 DS78LS120
LINE RECEIVER
+
−
ECL THRESHOLD
OUTPUT

TL/F/7499-8

The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3487	Quad TRI-STATE RS-422

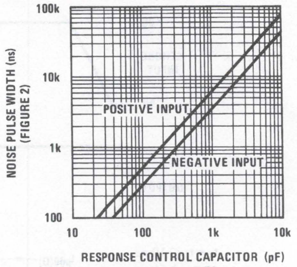
Unbalanced Drivers

DS1488	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

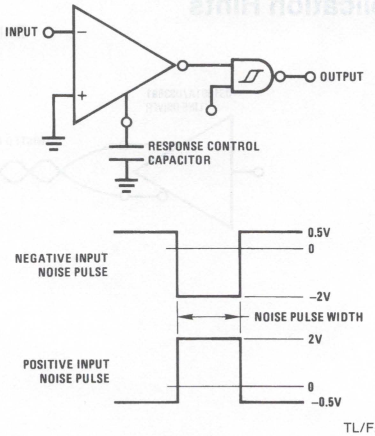
In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2.* This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.



TL/F/7499-9

FIGURE 1. Noise Pulse Width vs Response Control Capacitor


INPUT
−
+
OUTPUT
RESPONSE CONTROL
CAPACITOR
NEGATIVE INPUT
NOISE PULSE
0.5V
0
−2V
NOISE PULSE WIDTH
2V
POSITIVE INPUT
NOISE PULSE
0
−0.5V

TL/F/7499-10

FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/crosstalk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

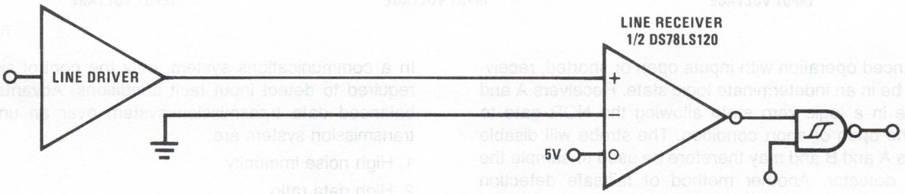
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ +0.45V or $V_{IN(INVERTING)}$ +0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the fail-safe offset pin to 5V, offsets the receiver threshold to 0.45V. The output is forced to a logic zero state if the input is open or shorted.

Unbalanced RS-423 and RS-232 Fail-Safe



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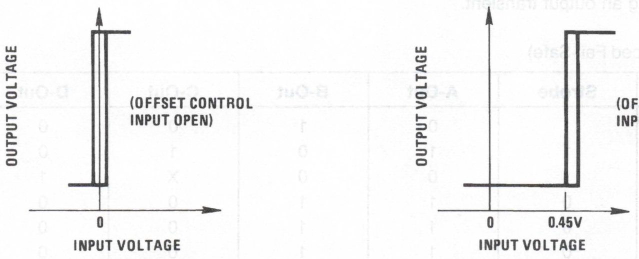
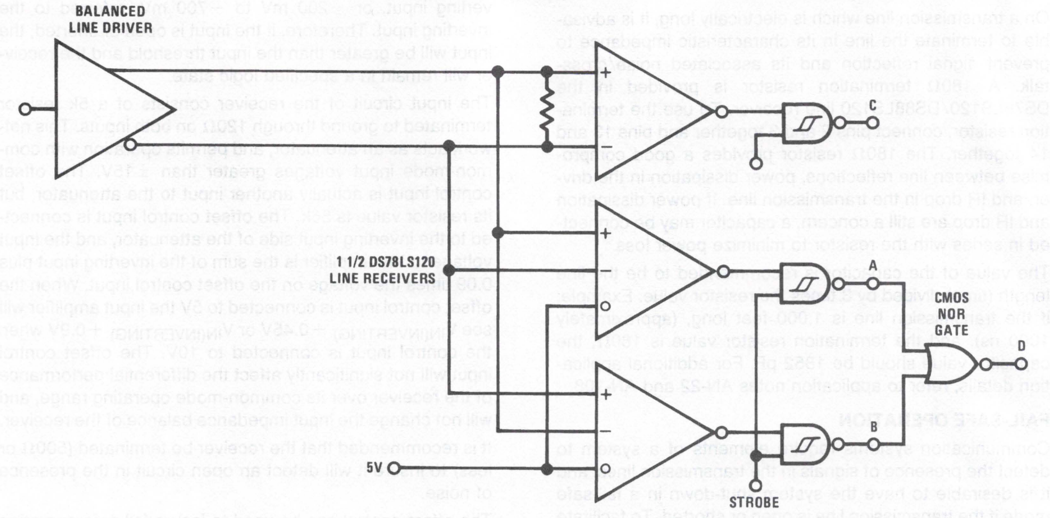


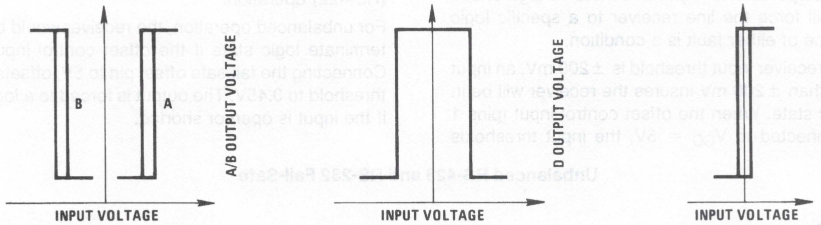
TL/F/7499-12

Application Hints (Continued)

Balanced RS-422 Fail-Safe



TL/F/7499–13



TL/F/7499–14

For balanced operation with inputs open or shorted, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the open or short condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

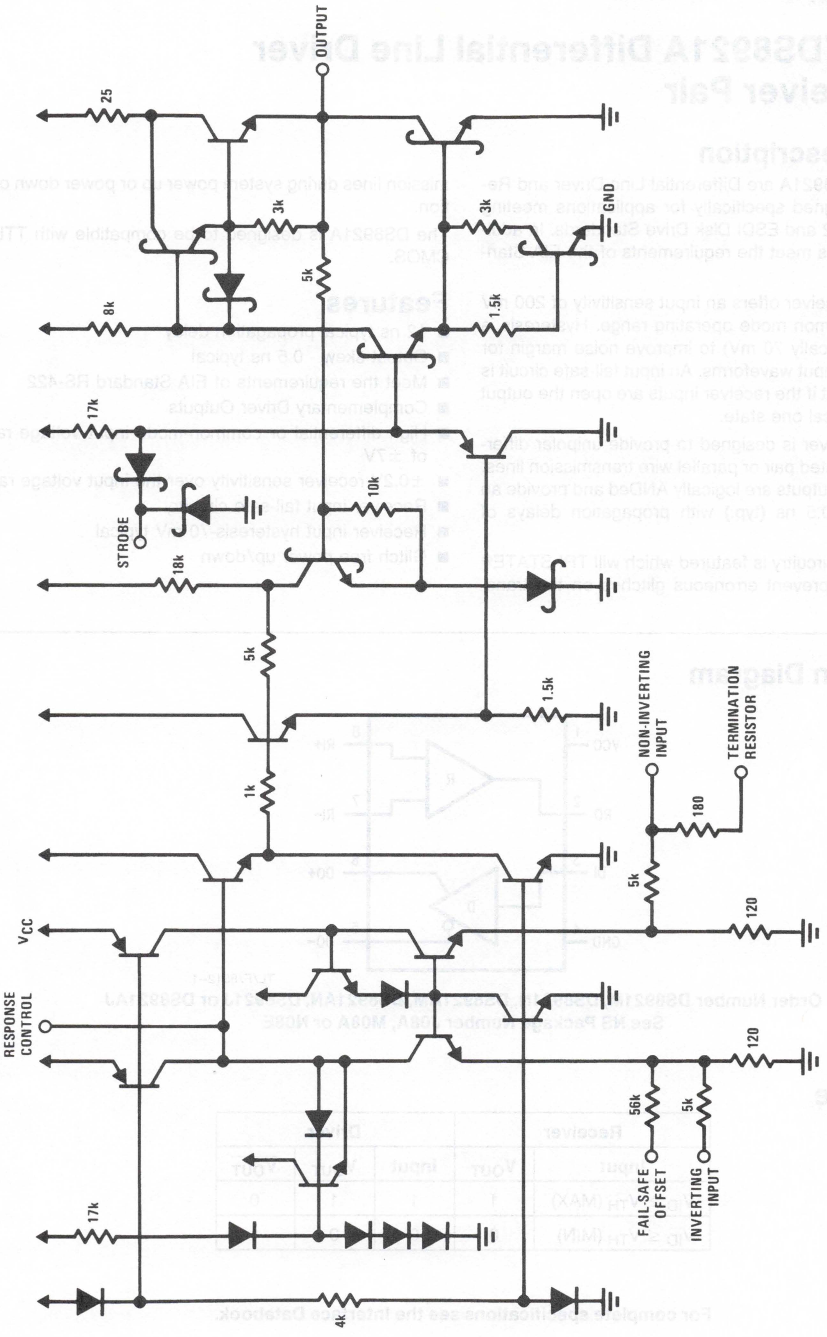
In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-Out	B-Out	C-Out	D-Out
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Schematic Diagram


RESPONSE CONTROL
VCC
17k
4k
STROBE
18k
17k
10k
5k
1k
1.5k
8k
25
3k
5k
3k
1.5k
OUTPUT
GND
FAIL-SAFE OFFSET
56k
INVERTING INPUT
5k
120
120
5k
NON-INVERTING INPUT
180
TERMINATION RESISTOR

TL/F/7499-2

National Semiconductor

DS8921/DS8921A Differential Line Driver and Receiver Pair

General Description

The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921A receiver offers an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8921A driver is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

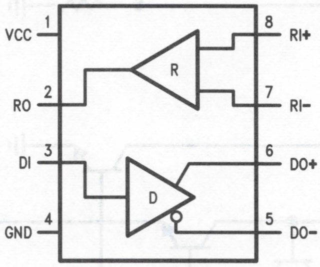
Power up/down circuitry is featured which will TRI-STATE® the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

The DS8921A is designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew - 0.5 ns typical
- Meet the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis-70 mV typical
- Glitch free power up/down

Connection Diagram



TL/F/8512-1

Order Number DS8921M, DS8921N, DS8921AM, DS8921AN, DS8921J or DS8921AJ
See NS Package Number J08A, M08A or N08E

Truth Table

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Driver Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8921/DS8921A Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Conditions	Min	Typ	Max	Units
RECEIVER					
V_{TH}	$-7V \leq V_{CM} \leq +7V$	−200	±35	+200	mV
V_{HYST}	$-7V \leq V_{CM} \leq +7V$	15	70		mV
R_{IN}	$-7V \leq V_{CM} \leq +7V$	4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$			3.25	mA
	$V_{IN} = -10V$			−3.25	mA
V_{OH}	$I_{OH} = -400\ \mu A$	2.5			V
V_{OL}	$I_{OL} = 8\ mA$			0.5	V
I_{SC}	$V_{CC} = MAX, V_{OUT} = 0V$	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	$V_{CC} = MAX, V_{IN} = 0.4V$		−40	−200	μA
I_{IH}	$V_{CC} = MAX, V_{IN} = 2.7V$			20	μA
I_I	$V_{CC} = MAX, V_{IN} = 7.0V$			100	μA
V_{CL}	$V_{CC} = MIN, I_{IN} = -18\ mA$			−1.5	V
V_{OH}	$V_{CC} = MIN, I_{OH} = -20\ mA$	2.5			V
V_{OL}	$V_{CC} = MIN, I_{OL} = +20\ mA$			0.5	V
I_{OFF}	$V_{CC} = 0V, V_{OUT} = 5.5V$			100	μA
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$				0.4	V
I_{SC}	$V_{CC} = MAX, V_{OUT} = 0V$	−30		−150	mA
DRIVER and RECEIVER					
I_{CC}	$V_{CC} = MAX, V_{OUT} = Logic\ 0$			35	mA

Receiver Switching Characteristics (*Figures 1 and 2*)

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	$C_L = 30$ pF		14	22.5	20	ns
T_{pHL}	$C_L = 30$ pF		14	22.5	20	ns
$\|T_{pLH} - T_{pHL}\|$	$C_L = 30$ pF		0.5	5	3.5	ns

Driver Switching Characteristics (*Figures 3 and 4*)

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	$C_L = 30$ pF		10	15	15	ns
T_{pHL}	$C_L = 30$ pF		10	15	15	ns
T_{TLH}	$C_L = 30$ pF		5	8	8	ns
T_{THL}	$C_L = 30$ pF		5	8	8	ns
Skew	CL = 30 pF (Note 5)		1	5	3.5	ns

Driver Switching Characteristics (*Figures 3 and 5*)

DIFFERENTIAL CHARACTERISTICS (Note 6)

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	$C_L = 30$ pF		10	15	15	ns
T_{pHL}	$C_L = 30$ pF		10	15	15	ns
$\|T_{pLH} - T_{pHL}\|$	$C_L = 30$ pF		0.5	6	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

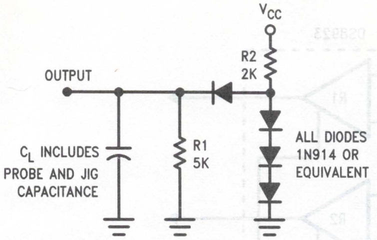
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

Where: T_{cr} = Crossing Point

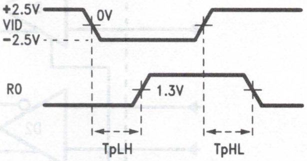
T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See *Figure 6*.

AC Test Circuits and Switching Diagrams


V_{CC}
R2
2K
OUTPUT
C_L INCLUDES
PROBE AND JIG
CAPACITANCE
R1
5K
ALL DIODES
1N914 OR
EQUIVALENT

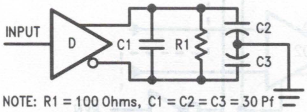
TL/F/8512-3

FIGURE 1


+2.5V
VID
−2.5V
0V
RO
1.3V
TpLH
TpHL

TL/F/8512-4

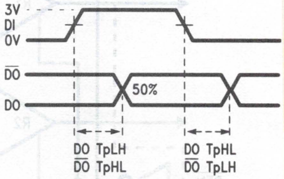
FIGURE 2


INPUT
D
C1
R1
C2
C3

NOTE: R1 = 100 Ohms, C1 = C2 = C3 = 30 Pf

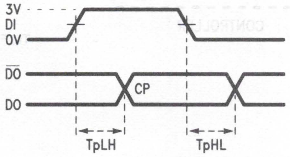
TL/F/8512-5

FIGURE 3


3V
DI
0V
DO
DO
50%
DO TpLH
DO TpHL
DO TpHL
DO TpLH

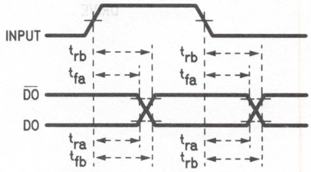
TL/F/8512-6

FIGURE 4


3V
DI
0V
DO
DO
CP
TpLH
TpHL

TL/F/8512-7

FIGURE 5

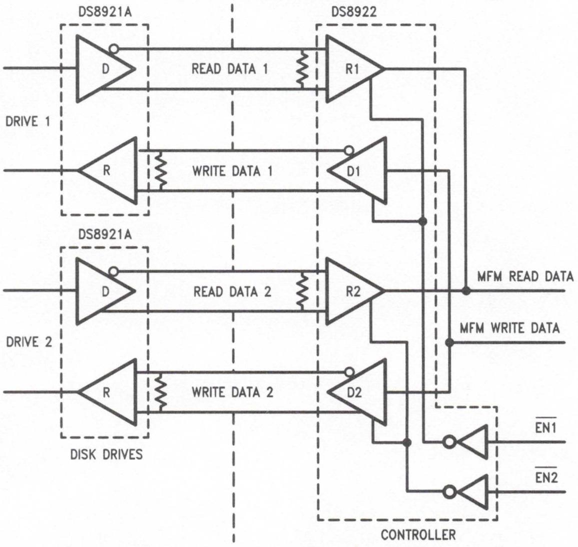

INPUT
trb
tfa
trb
tfa
DO
DO
tra
tfb
tra
trb

TL/F/8512-2

FIGURE 6

Typical Applications

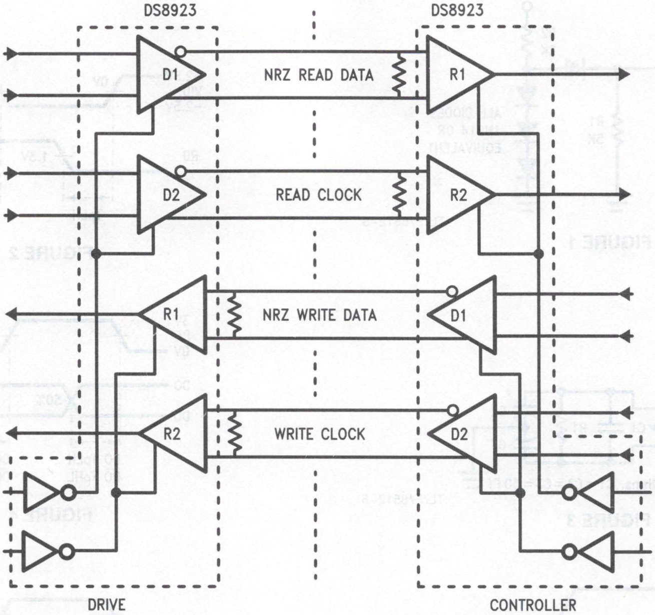
ST506 and ST412 Application


DS8921A
D
READ DATA 1
DS8922
R1
DRIVE 1
R
WRITE DATA 1
D1
DS8921A
D
READ DATA 2
R2
MFM READ DATA
DRIVE 2
MFM WRITE DATA
R
WRITE DATA 2
D2
EN1
EN2
DISK DRIVES
CONTROLLER

TL/F/8512-8

Typical Applications (Continued)

ESDI Application


DS8923
DS8923
D1
NRZ READ DATA
R1
D2
READ CLOCK
R2
R1
NRZ WRITE DATA
D1
R2
WRITE CLOCK
D2
DEN
REN
REN
DEN
DRIVE
CONTROLLER

TL/F/8512-9

National Semiconductor

DS8922/22A/DS8923/23A TRI-STATE® RS-422 Dual Differential Line Driver and Receiver Pairs

General Description

The DS8922/22A and DS8923/23A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923/23A have separate driver and receiver control functions.

Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

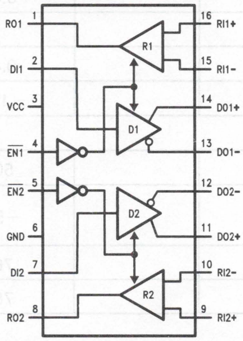
The DS8922/22A and DS8923/23A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew—±0.5 ns typical
- Meets the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis—±70 mV typical
- Glitch free power up/down
- TRI-STATE outputs

Connection Diagrams

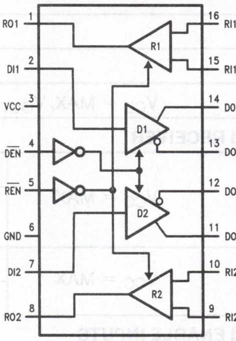
DS8922A Dual-In-Line



TL/F/8511–1

Order Number DS8922N, J, M, DS8922AN, AJ, AM
See NS Package Number N16A, J16A or M16A

DS8923A Dual-In-Line



TL/F/8511–2

Order Number DS8923N, J, M
DS8923AN, AJ, AM
See NS Package Number N16A, J16A or M16A

Truth Tables

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923/23A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Drive Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Storage Temperature Range	−65°C to +165°C
Lead Temp. (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8922/22A and DS8923/23A Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER						
V_{TH}	$-7V \leq V_{CM} \leq +7V$		−200	±35	+200	mV
V_{HYST}	$-7V \leq V_{CM} \leq +7V$		15	50		mV
R_{IN}	$-7V \leq V_{CM} \leq +7V$		4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$				3.25	mA
	$V_{IN} = -10V$				−3.25	mA
V_{OH}	V_{CC} = MIN, $I_{OH} = -400\ \mu A$		2.5			V
V_{OL}	V_{CC} = MAX, I_{OL} = 8 mA				0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−15		−100	mA
DRIVER						
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA		2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA				0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V				100	µA
$\lvert VT \rvert - \lvert \overline{VT} \rvert$					0.4	V
VT			2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$					0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−30		−150	mA
DRIVER and RECEIVER						
I_{OZ} TRI-STATE Leakage	V_{CC} = MAX	V_{OUT} = 2.5V			50	µA
		V_{OUT} = 0.4V			−50	µA
I_{CC}	V_{CC} = MAX	ACTIVE			76	mA
		TRI-STATE			78	mA
DRIVER and ENABLE INPUTS						
V_{IH}			2.0			V
V_{IL}					0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V			−40	−200	µA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V				20	µA
I_I	V_{CC} = MAX, V_{IN} = 7.0V				100	µA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA				−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	22.5	20	ns
T_{pHL}	CL = 30 pF		12	22.5	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	5	3.5	ns
Skew (Channel to Channel)	CL = 30 pF		0.5	3.0	2.0	ns
T_{pLZ}	CL = 15 pF S2 Open		15			ns
T_{pHZ}	CL = 15 pF S1 Open		15			ns
T_{pZL}	CL = 30 pF S2 Open		20			ns
T_{pZH}	CL = 30 pF S1 Open		20			ns

Driver Switching Characteristics (*Figures 4, 5* and *6*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
SINGLE ENDED CHARACTERISTICS						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
T_{TLH}	CL = 30 pF		5	10	10	ns
T_{THL}	CL = 30 pF		5	10	10	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5			ns
Skew	CL = 30 pF (Note 5)		0.5	5	3.5	ns
Skew (Channel to Channel)			0.5	3.0	2.0	ns
T_{pLZ}	CL = 30 pF		15			ns
T_{pHZ}	CL = 30 pF		15			ns
T_{pZL}	CL = 30 pF		20			ns
T_{pZH}	CL = 30 pF		20			ns

Differential Switching Characteristics (Note 6, *Figure 7*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	6.0	2.75	ns

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

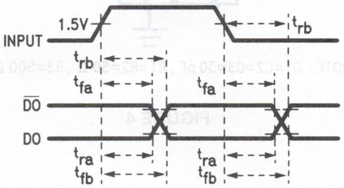
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$Tcr = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

Where: Tcr = Crossing Point

Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

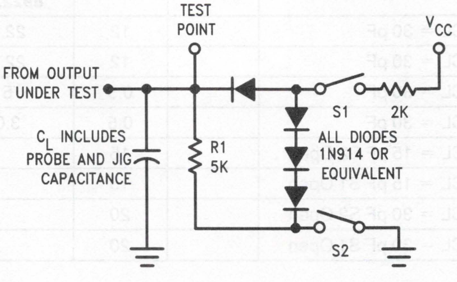
Switching Time Waveforms



TL/F/8511-3

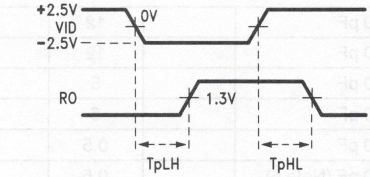
1

AC Test Circuits and Switching Waveforms


TEST POINT
V_CC
FROM OUTPUT UNDER TEST
S1
2K
C_L INCLUDES PROBE AND JIG CAPACITANCE
R1 5K
ALL DIODES 1N914 OR EQUIVALENT
S2

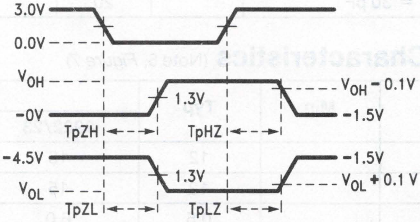
TL/F/8511–4

FIGURE 1


+2.5V
VID
−2.5V
0V
RO
1.3V
TpLH
TpHL

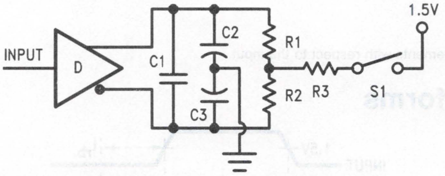
TL/F/8511–5

FIGURE 2


3.0V
0.0V
V_OH
−0V
−4.5V
V_OL
1.3V
1.3V
TpZH
TpHZ
TpZL
TpLZ
V_OH − 0.1V
−1.5V
−1.5V
V_OL + 0.1 V

TL/F/8511–6

FIGURE 3

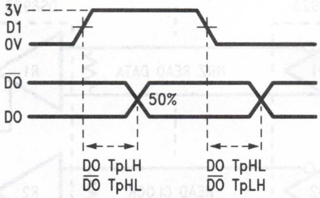

INPUT
D
C1
C2
C3
R1
R2
R3
S1
1.5V

NOTE: C1=C2=C3=30 pF, R1=R2=50 Ω, R3=500 Ω

TL/F/8511–7

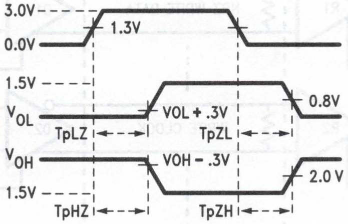
FIGURE 4

AC Test Circuit and Switching Waveforms (Continued)


3V
D1
0V
$\overline{DO}$
50%
DO
DO TpLH
$\overline{DO}$ TpHL
DO TpHL
$\overline{DO}$ TpLH

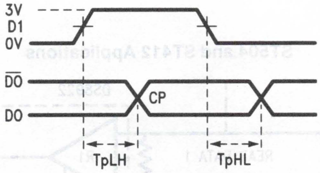
TL/F/8511-8

FIGURE 5


3.0V
1.3V
0.0V
1.5V
V_{OL}
VOL + .3V
TpLZ
TpZL
0.8V
V_{OH}
VOH - .3V
1.5V
2.0 V
TpHZ
TpZH

TL/F/8511-9

FIGURE 6

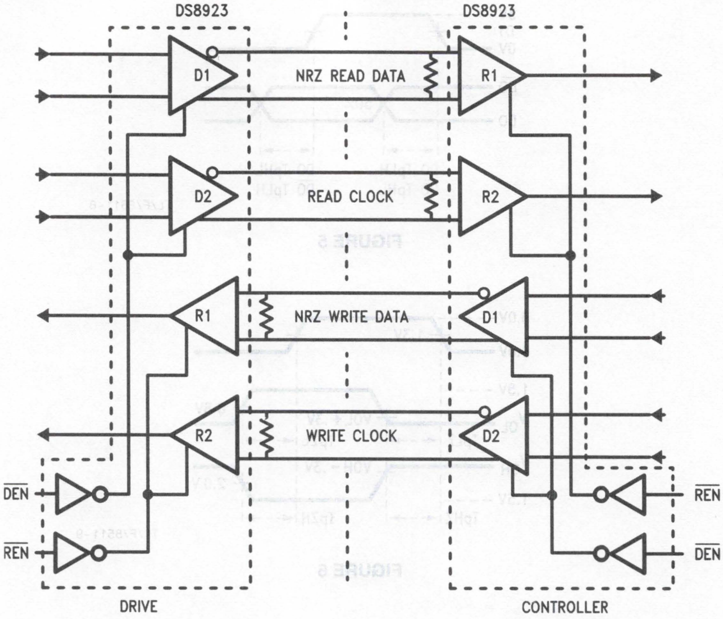

3V
D1
0V
$\overline{DO}$
CP
DO
TpLH
TpHL

TL/F/8511-10

FIGURE 7

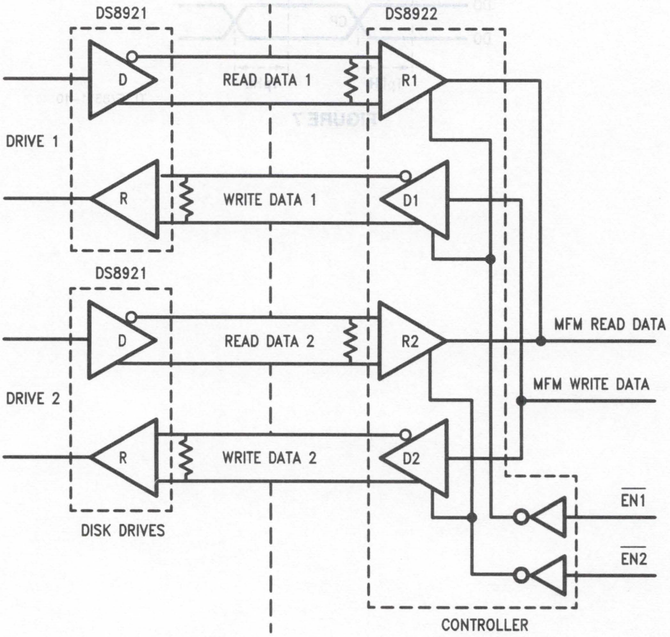
Typical Applications

ESDI Application


DS8923
DS8923
D1
NRZ READ DATA
R1
D2
READ CLOCK
R2
R1
NRZ WRITE DATA
D1
R2
WRITE CLOCK
D2
$\overline{DEN}$
$\overline{REN}$
$\overline{REN}$
$\overline{DEN}$
DRIVE
CONTROLLER

TL/F/8511-11

ST504 and ST412 Applications


DS8921
DS8922
D
READ DATA 1
R1
DRIVE 1
R
WRITE DATA 1
D1
DS8921
D
READ DATA 2
R2
MFM READ DATA
MFM WRITE DATA
DRIVE 2
R
WRITE DATA 2
D2
$\overline{EN1}$
$\overline{EN2}$
DISK DRIVES
CONTROLLER

TL/F/8511-12

National Semiconductor

DS8924 Quad TRI-STATE® Differential Line Driver

General Description

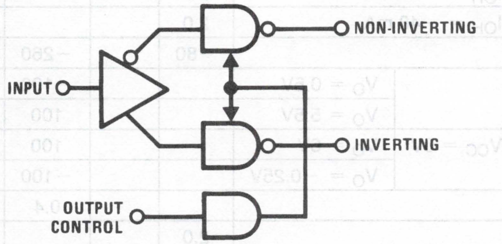
The DS8924 is a quad differential line driver designed for digital data transmission over balanced lines. The outputs are TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

The DS8924 is pin and functionally compatible with DS3487. It features improved performance over 3487-type circuit as outputs can source and sink 48 mA. In addition, outputs are not significantly affected by negative line reflections that can occur when the transmission line is unterminated at the receiver end.

Features

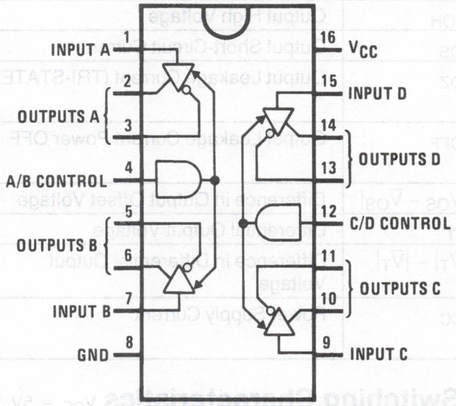
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs
- Power up/down protection
- Fast propagation times (typ 12 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with DS3487 and MC3487
- Output skew—2 ns typ

Block and Connection Diagrams


INPUT
NON-INVERTING
INVERTING
OUTPUT CONTROL

TL/F/8507-1

Dual-In-Line Package


INPUT A 1
2
OUTPUTS A
3
A/B CONTROL 4
5
OUTPUTS B
6
INPUT B 7
GND 8
16 VCC
15 INPUT D
14
OUTPUTS D
13
12 C/D CONTROL
11
OUTPUTS C
10
9 INPUT C

TL/F/8507-2

Top View

Order Number DS8924J or N
See NS Package J16A or N16A

Truth Table

Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1550 mW
Molded Package	1560 mW

*Derate cavity package 10.3 mW/°C above 25°C; derate molded package 12.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8924	4.75	5.25	V
Temperature (T_A)			
DS8924	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	$V_{IL} = 0.5V$			−200	µA
I_{IH}	Input High Current	$V_{IH} = 2.7V$			50	µA
		$V_{IH} = 5.5V$			100	µA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA			−1.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 48$ mA			0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -20$ mA	2.5			V
V_{OH}	Output High Voltage	$I_{OH} = -48$ mA	2.0			V
I_{OS}	Output Short-Circuit Current		−80		−260	mA
I_{OZ}	Output Leakage Current (TRI-STATE)	$V_O = 0.5V$			−100	µA
		$V_O = 5.5V$			100	µA
I_{OFF}	Output Leakage Current Power OFF	$V_{CC} = 0V$, $V_O = 6V$			100	µA
		$V_O = -0.25V$			−100	µA
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference in Output Offset Voltage				0.4	V
V_T	Differential Output Voltage		2.0			V
$\lvert V_T\rvert - \lvert\overline{V}_T\rvert$	Difference in Differential Output Voltage				0.4	V
I_{CC}	Power Supply Current	Active		50	80	mA
		TRI-STATE		35	60	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			12	20	ns
t_{PLH}	Input to Output			12	20	ns
Skew	Output to Output	$C_L = 50$ pF		2.0	5.0	ns
t_{THL}	Differential Fall Time			10	20	ns
t_{TLH}	Differential Rise Time			10	20	ns
t_{PHZ}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF		17	25	ns
t_{PLZ}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF		20	30	ns
t_{PZH}	Enable to Output	$R_L = \infty$, $C_L = 50$ pF, S1 Open		13	25	ns
t_{PZL}	Enable to Output	$R_L = 200\Omega$, $C_L = 50$ pF, S2 Open		17	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

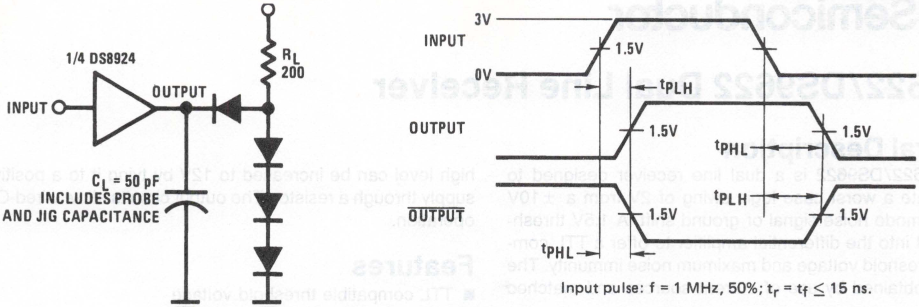
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS8924. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

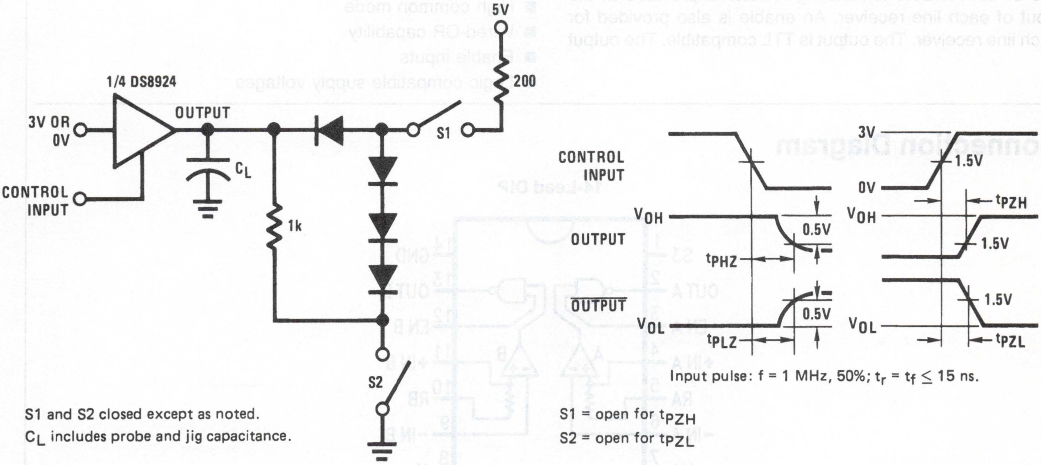
AC Test Circuits and Switching Time Waveforms


1/4 DS8924
INPUT
OUTPUT
RL
200
CL = 50 pF
INCLUDES PROBE
AND JIG CAPACITANCE
3V
0V
INPUT
1.5V
tPLH
OUTPUT
1.5V
tPHL
1.5V
tPLH
OUTPUT
1.5V
tPHL
1.5V

Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

TL/F/8507–3

FIGURE 1. Propagation Delays


5V
200
1/4 DS8924
3V OR
0V
OUTPUT
S1
CL
CONTROL
INPUT
1k
S2
CONTROL
INPUT
3V
1.5V
0V
VOH
OUTPUT
0.5V
tPHZ
OUTPUT
VOL
0.5V
tPLZ
tPZH
VOH
1.5V
1.5V
VOL
tPZL

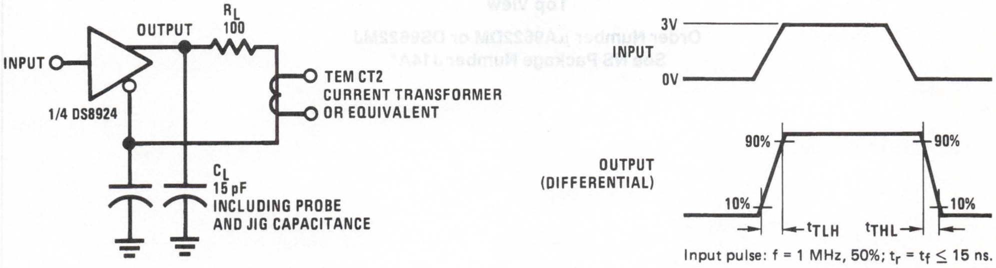
S1 and S2 closed except as noted.
C_L includes probe and jig capacitance.

Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

S1 = open for t_{PZH}
S2 = open for t_{PZL}

TL/F/8507–4

FIGURE 2. TRI-STATE Enable and Disable Delays


RL
100
OUTPUT
INPUT
1/4 DS8924
TEM CT2
CURRENT TRANSFORMER
OR EQUIVALENT
CL
15 pF
INCLUDING PROBE
AND JIG CAPACITANCE
3V
INPUT
0V
OUTPUT
(DIFFERENTIAL)
90%
90%
10%
10%
tTLH
tTHL

Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

TL/F/8507–5

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

μA9622/DS9622 Dual Line Receiver

General Description

The μA9622/DS9622 is a dual line receiver designed to discriminate a worst case logic swing of 2V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors.

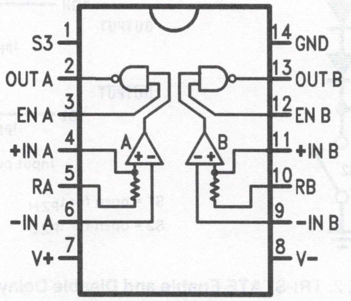
The μA9622/DS9622 allows the choice of output states with the input open, without affecting circuit performance by use of S3. A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to 12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

Features

- TTL compatible threshold voltage
- Input terminating resistors
- Choice of output state with inputs open
- TTL compatible output
- High common mode
- Wired-OR capability
- Enable inputs
- Logic compatible supply voltages

Connection Diagram

14-Lead DIP



TL/F/9760–2

Top View

Order Number μA9622DM or DS9622MJ
See NS Package Number J14A*

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* For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation	400 mW
V^+ to GND	−0.5V to +7.0V
Input Voltage	±15V
Voltage Applied to Outputs for Output High State	−0.5V to +13.2V
V^- to GND	−0.5V to −12V
Enable to GND	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Temperature, T_A	−55	+125	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = S3 = 4.5V$, $V^- = -11V$, $V_{DIFF} = 2.0V$, $I_{OL} = 12.4$ mA, EN = Open			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 4.5V$, $V^- = -9.0V$, $S3 = 0V$, $V_{DIFF} = 1.0V$, $I_{OH} = -0.2$ mA, EN = Open		2.8		V
I_{CEX}	Output Leakage Current	$V^+ = 4.5V$, $V^- = -11V$, $S3 = 0V$, $V_{DIFF} = 1.0V$, $V_O = 12V$, EN = Open			200	µA
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 5.0V$, $V^- = -10V$, $V_{DIFF} = 1.0V$, $V_O = S3 = 0V$, EN = Open		−3.1	−1.4	mA
I_R(EN)	Enable Input Leakage Curent	$V^+ = S3 = 4.5V$, $V^- = -11V$, I_N = Open, EN = 4.0V			5.0	µA
I_F(EN	Enable Input Forward Current	$V^+ = 5.5V$, $V^- = -9.0V$ V_I = Open, EN = S3 = 0V		−1.5		mA
I_F(+IN)	+ Input Forward Current	$V^+ = 5.0V$, $V^- = -10V$, $V_I^+ = 0V$, V_I^- = GND, EN = S3 = Open		−2.3		mA
I_F(−IN)	− Input Forward Curent	$V^+ = S3 = 5.0V$, $V^- = -10V$, V_I^+ = GND, $V_I^- = 0V$, EN = Open		−2.6		mA
V_{IL}(EN)	Input Voltage LOW	$4.5V \le V^+ \le 5.5V$, $-11V \le V^- \le -9.0V$, EN = Open	+25°C		1.0	V
			+125°C		0.7	V
			−55°C		1.3	V
V_{TH}	Differential Input Threshold Voltage	$4.5V, \le V^+ \le 5.5V$, $-11V \le V^- \le -9.0V$, EN = Open		1.0	2.0	V
V_{CM}	Common Mode Voltage	$V^+ = 5.0V$, $V^- = -10V$, $1.0V \le V_{DIFF} \le 2.0V$	25°C	−10	+10	V
R_T	Terminating Resistance		25°C	91	215	Ω
I^+	Positive Supply Current	$V^+ = S3 = V_I^+ = 5.5V$, $V^- = 11V$, $V_I^- = 0V$	25°C		22.9	mA
I^-	Negative Supply Current			−11.1		mA
SWITCHING CHARACTERISTICS $T_A = 25°C$						
t_{PLH}	Propagation Delay to High Level	$V^+ = 5.0V$, $V^- = -10V$, $0V \le V_I \le 3.0V$, $C_L = 30$ pF (See *Figure 1*)	$R_L = 3.9$ kΩ		50	ns
t_{PHL}	Propagation Delay to Low Level		$R_L = 390Ω$		50	ns

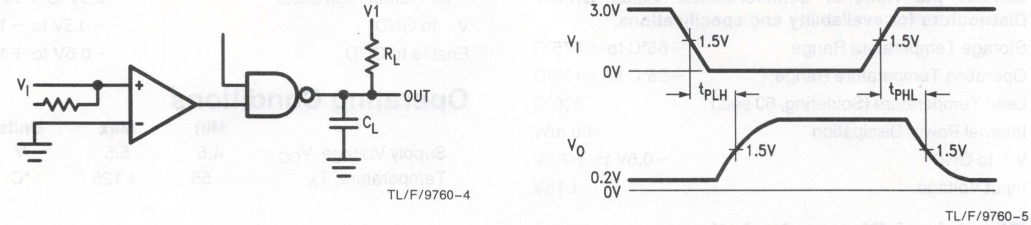
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Test Circuit and Waveforms

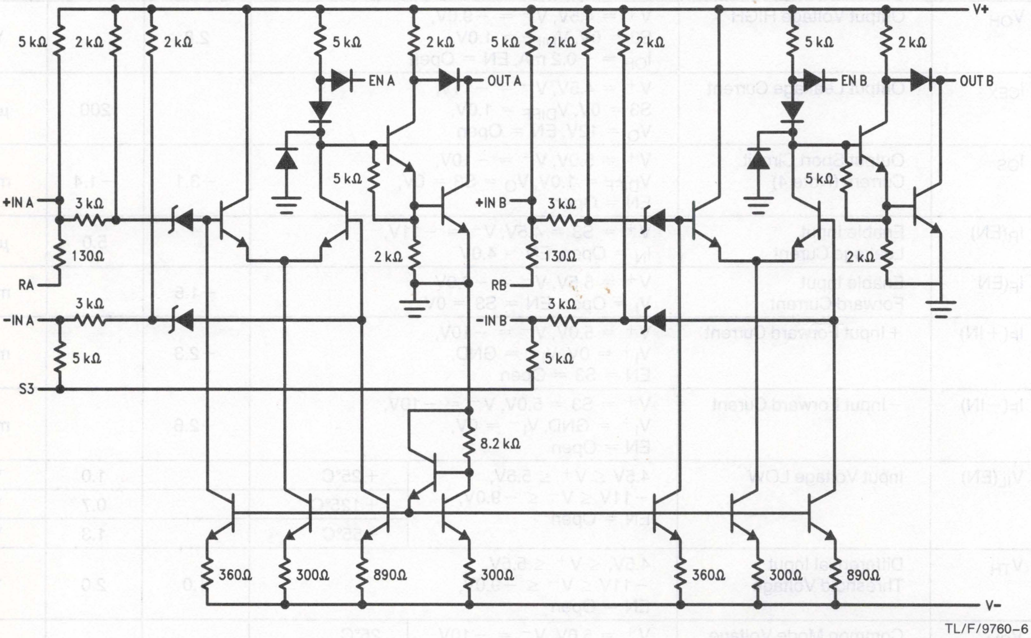

V1
R_L
OUT
C_L
V_I
+
-
3.0V
V_I
1.5V
1.5V
0V
t_{PLH}
t_{PHL}
V_O
1.5V
1.5V
0.2V
0V

TL/F/9760-4

TL/F/9760-5

FIGURE 1

Equivalent Circuit


V+
V−
5 kΩ
2 kΩ
2 kΩ
5 kΩ
2 kΩ
5 kΩ
2 kΩ
2 kΩ
5 kΩ
2 kΩ
EN A
OUT A
EN B
OUT B
5 kΩ
5 kΩ
+IN A
3 kΩ
130Ω
RA
−IN A
3 kΩ
5 kΩ
S3
+IN B
3 kΩ
130Ω
RB
−IN B
3 kΩ
5 kΩ
2 kΩ
2 kΩ
8.2 kΩ
360Ω
300Ω
890Ω
300Ω
360Ω
300Ω
890Ω

TL/F/9760-6

National Semiconductor

μA9627/DS9627 Dual Line Receiver

General Description

The μA9627/DS9627 is a dual-line receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accommodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The μA9627/DS9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V−, the typical switching points are at 2.6V and −2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the typical switching points are at 50 μA and −50 μA, thus satisfying the requirements of MIL-STD-188C LOW level interface. Connecting the RA and/or RB pins to the (−) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving RA and/or RB pins unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

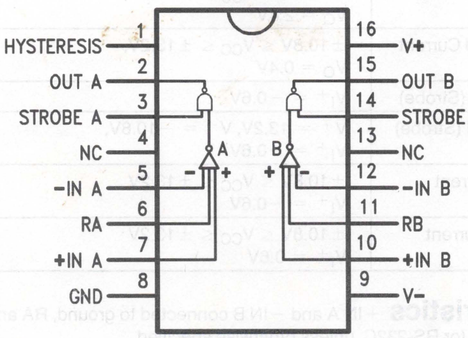
The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wired-OR function. A TTL/DTL strobe is also provided for each receiver.

Features

- EIA RS-232-C input standards
- MIL-STD-188C input standards
- Variable hysteresis control
- High common mode rejection
- R control (5 kΩ or 10 kΩ)
- Wired-OR capability
- Choice of inverting and non-inverting inputs
- Outputs and strobe TTL compatible

Connection Diagram

16-Lead DIP



TL/F/9761–1

Top View

Order Number μA9627DM or DS9627MJ
See NS Package Number* J16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation	400 mW
V^+ to GND	0V to +15V
V^- to GND	0V to −15V
Input Voltage Referred to GND	±25V
Strobe to GND	−0.5V to +5.5V
Applied Output Voltage	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)	−55	+125	°C

Electrical Characteristics

Hysteresis, −IN A, −IN B, RA and RB Open for MIL-STD-188C, unless otherwise specified (Notes 2 and 3)

Symbol	Characteristics	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = 10.8V$, $V^- = -13.2V$, $V_I^+ = 0.6V$, $I_{OL} = 6.4$ mA			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 10.8V$, $V^- = -13.2V$, $V_I^+ = 0.6V$, $I_{OH} = -0.5$ mA		2.4		V
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 13.2V$, $V^- = -10.8V$, $V_I^+ = 0.6V$, $V_O = 0V$		−3.0		mA
I_{IH}(ST)	Input Current HIGH (Strobe)	$V^+ = 10.8V$, $V^- = -13.2V$, $V_I^+ = 0.6V$	$V_{ST} = 2.4V$		40	μA
			$V_{ST} = 5.5V$		1.0	mA
R_I	Input Resistance	$V^+ = 13.2V$, $V^- = -13.2V$, $-3.0V \le V_I^+ \le 3.0V$		6.0		kΩ
I_{TH}^+	Positive Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$, $V_O = 2.4V$			100	μA
I_{TH}^-	Negative Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$, $V_O = 0.4V$		−100		μA
V_{IL}(ST)	Input Voltage LOW (Strobe)	$V_I^+ = -0.6V$			0.8	V
V_{IH}(ST)	Input Voltage HIGH (Strobe)	$V^+ = 13.2V$, $V^- = -10.8V$, $V_I^+ = -0.6V$		2.0		V
I^+	Positive Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = -0.6V$			18	mA
I^-	Negative Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = 0.6V$		−16		mA

Electrical Characteristics

+IN A and −IN B connected to ground, RA and RB connected to −IN A and −IN B and Hysteresis connected to V^- for RS-232C, unless otherwise specified

Symbol	Characteristics	Conditions	Min	Max	Units
R_I	Input Resistance	$3.0V \le V_I \le 25V$	3.0	7.0	kΩ
		$-3.0V \le V_I \le -25V$	3.0	7.0	kΩ
V_I	Input Voltage		−2.0	2.0	V
V_{TH+}	Positive Threshold Voltage			3.0	V
V_{TH-}	Negative Threshold Voltage		−3.0		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

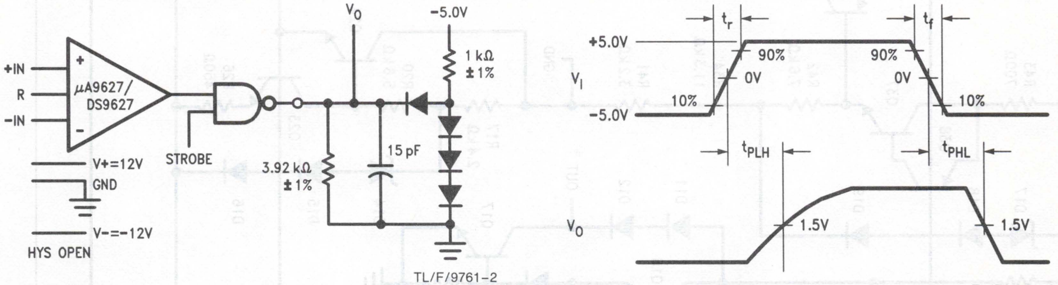
Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Electrical Characteristics V_{CC} = ±12V for MIL-STD-188C and RS-232C, T_A = 25°C

Symbol	Characteristics	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay to High Level	(See *Figure 1*)		250	ns
t_{PHL}	Propagation Delay to Low Level	(See *Figure 1*)		250	ns


+IN
R
-IN
+
-
μA9627/
DS9627
V+=12V
GND
V-=-12V
HYS OPEN
STROBE
V_O
-5.0V
1 kΩ
±1%
3.92 kΩ
±1%
15 pF
t_r
t_f
+5.0V
-5.0V
V_I
90%
90%
0V
0V
10%
10%
t_{PLH}
t_{PHL}
V_O
1.5V
1.5V

TL/F/9761-2

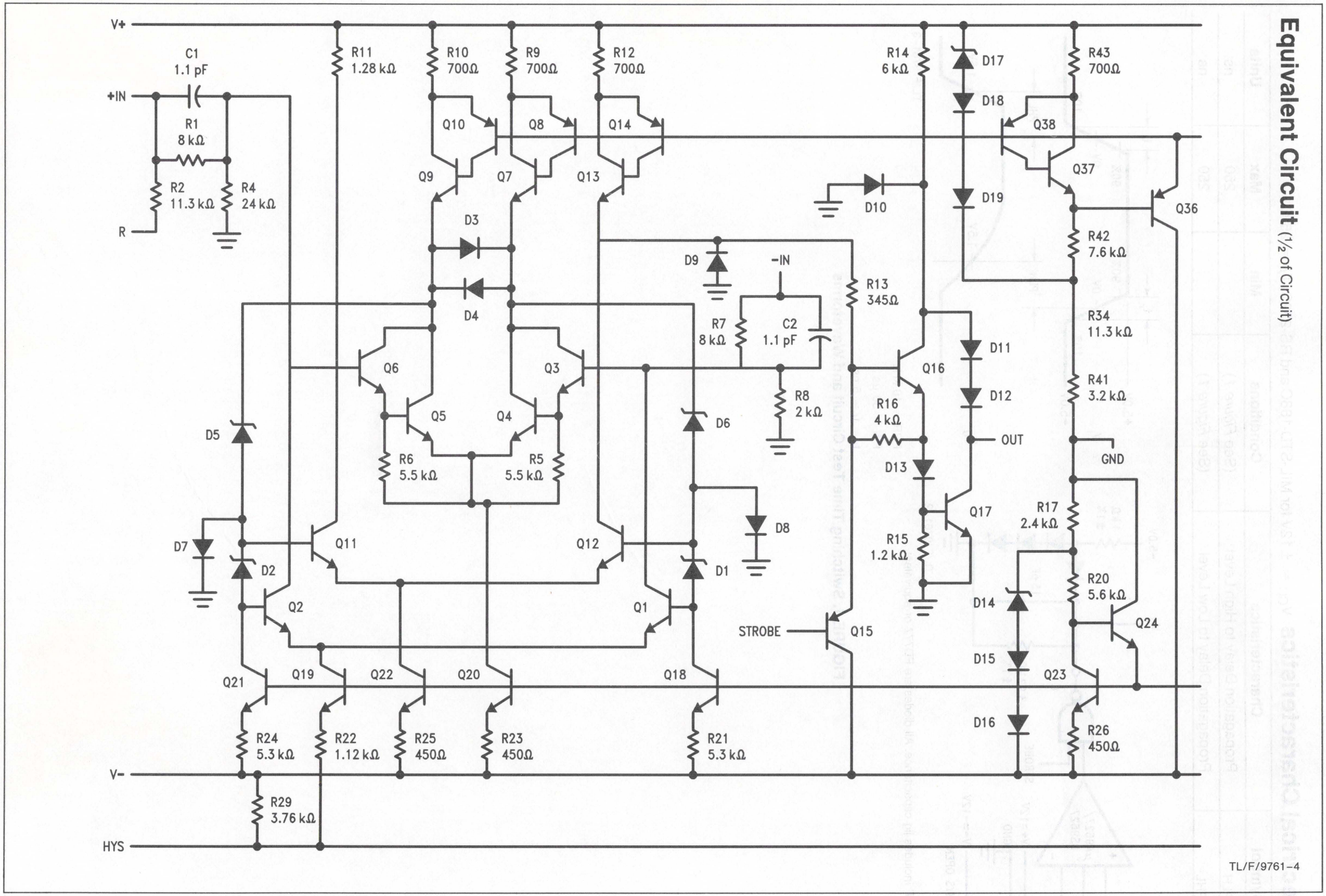
TL/F/9761-3

15 pF includes jig capacitance. All diodes are FD777 or equivalent.

PRR = 10 kHz
PW = 50 μs
t_r = t_f = 5 ns

FIGURE 1. Switching Time Test Circuit and Waveforms

Equivalent Circuit (½ of Circuit)


V+
C1
1.1 pF
+IN
R1
8 kΩ
R2
11.3 kΩ
R4
24 kΩ
R
R11
1.28 kΩ
R10
700Ω
R9
700Ω
R12
700Ω
Q10
Q8
Q14
Q9
Q7
Q13
D3
D4
Q6
Q5
Q4
Q3
R6
5.5 kΩ
R5
5.5 kΩ
D5
D7
D2
Q11
Q12
Q2
Q1
D6
D1
D8
D9
-IN
R7
8 kΩ
C2
1.1 pF
R8
2 kΩ
R13
345Ω
R14
6 kΩ
D10
D17
D18
D19
R43
700Ω
Q38
Q37
Q36
R42
7.6 kΩ
R34
11.3 kΩ
R41
3.2 kΩ
Q16
R16
4 kΩ
D11
D12
OUT
GND
D13
Q17
R15
1.2 kΩ
R17
2.4 kΩ
R20
5.6 kΩ
Q24
D14
D15
D16
Q23
R26
450Ω
STROBE
Q15
Q21
Q19
Q22
Q20
Q18
R24
5.3 kΩ
R22
1.12 kΩ
R25
450Ω
R23
450Ω
R21
5.3 kΩ
V-
R29
3.76 kΩ
HYS

TL/F/9761–4

National Semiconductor

DS9636A/μA9636A RS-423 Dual Programmable Slew Rate Line Driver

General Description

The DS9636A/μA9636A is a TTL/CMOS compatible, dual, single ended line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The DS9636A/μA9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current-limiting is provided in both output states. The DS9636A/μA9636A is designed for nominal power supplies of ±12V.

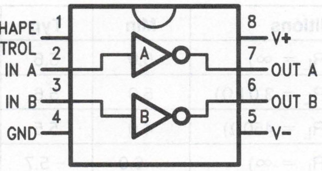
Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

Features

- Programmable slew rate limiting
- Meets EIA Standard RS-423
- Commercial or extended temperature range
- Output short circuit protection
- TTL and CMOS compatible inputs

Connection Diagram

8-Lead DIP



TL/F/9620–1

Top View

Order Number DS9636ACJ, μA9636ARC, DS9636AMJ, μA9636ARM or DS9636ACN, μA9636ATC
See NS Package Number J08A or N08E

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
V+ Lead Potential to Ground Lead	V− to +15V
V− Lead Potential to Ground Lead	+0.5V to −15V
V+ Lead Potential to V− Lead	0V to +30V
Output Potential to Ground Lead	±15V
Output Source Current	−150 mA
Output Sink Current	150 mA

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

Characteristics	DS9636AM/μA9636AM			DS9636AC/μA9636AC			Units
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V+)	10.8	12	13.2	10.8	12	13.2	V
Negative Supply Voltage (V−)	−13.2	−12	−10.8	−13.2	−12	−10.8	V
Operating Temperature (T_A)	−55	25	125	0	25	70	°C
Wave Shaping Resistance (R_{WS})	10		500	10		1000	kΩ

Electrical Characteristics

Over recommended operating temperature, supply voltage and wave shaping resistance ranges unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH1}	Output Voltage HIGH	R_L to GND ($R_L = \infty$)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND ($R_L = 3.0\ k\Omega$)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND ($R_L = 450\Omega$)	4.0	5.5	6.0	V
V_{OL1}	Output Voltage LOW	R_L to GND ($R_L = \infty$)	−6.0	−5.7	−5.0	V
V_{OL2}		R_L to GND ($R_L = 3.0\ k\Omega$)	−6.0	−5.6	−5.0	V
V_{OL3}		R_L to GND ($R_L = 450\Omega$)	−6.0	−5.4	−4.0	V
R_O	Output Resistance	$450\Omega \le R_L$		25	50	Ω
I_{OS+}	Output Short Circuit Current (Note 4)	$V_O = 0V, V_I = 0V$	−150	−60	−15	mA
I_{OS-}		$V_O = 0V, V_I = 2.0V$	15	60	150	mA
I_{CEX}	Output Leakage Current	$V_O = \pm 6.0V$, Power-Off	−100		+100	μA
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{IC}	Input Clamp Diode Voltage	$I_I = 15$ mA	−1.5	−1.1		V
I_{IL}	Input Current LOW	$V_I = 0.4V$	−80	−16		V
I_{IH}	Input Current HIGH	$V_I = 2.4V$		1.0	10	μA
		$V_I = 5.5V$		10	100	
I+	Positive Supply Current	$V_{CC} = \pm 12V$, $R_L = \infty$, $R_{WS} = 100\ k\Omega$, $V_I = 0V$		13	18	mA
I−	Negative Supply Current	$V_{CC} = \pm 12V$, $R_L = \infty$, $R_{WS} = 100\ k\Omega$, $V_I = 0V$	−18	−13		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

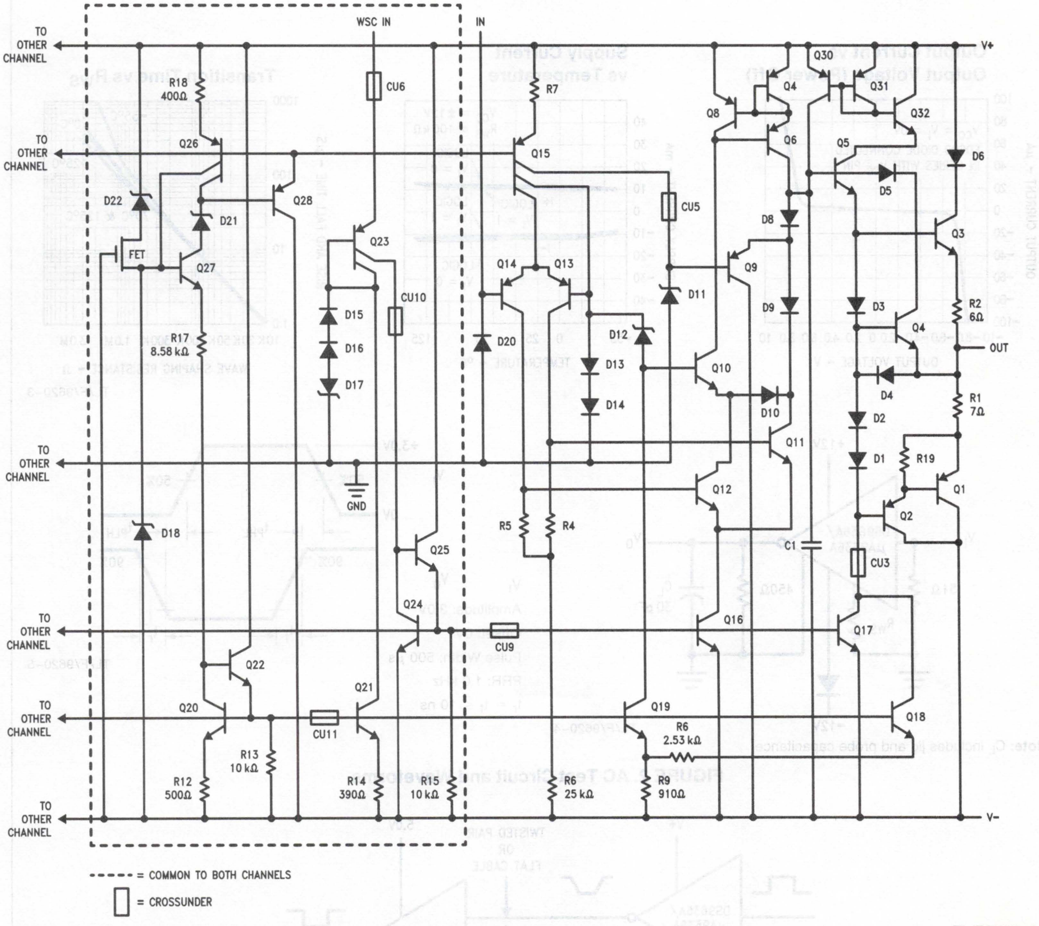
Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for the DS9636AM and across the 0°C to +70°C range for the DS9636AC. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = \pm 12V \pm 10\%$, $T_A = 25°C$, see AC Test Circuit

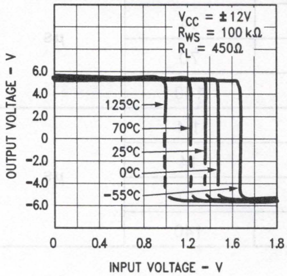
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r	Rise Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	µs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	
t_f	Fall Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	µs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	


TO OTHER CHANNEL
WSC IN
IN
V+
R18 400Ω
CU6
R7
Q30
Q4
Q31
Q8
Q32
Q26
Q15
Q6
Q5
D6
CU5
D22
Q28
D21
D5
D8
FET
Q23
Q3
Q27
Q14
Q13
Q9
D11
CU10
D15
D9
D3
R2 6Ω
D20
D12
Q4
OUT
R17 8.58 kΩ
D16
D13
Q10
D4
D17
D14
D10
R1 7Ω
D2
Q11
D1
R19
GND
Q12
Q1
R5
R4
Q2
D18
Q25
C1
CU3
Q16
Q24
Q17
CU9
Q22
Q21
Q19
Q18
Q20
CU11
R6 2.53 kΩ
R13 10 kΩ
R12 500Ω
R14 390Ω
R15 10 kΩ
R6 25 kΩ
R9 910Ω
V−
= COMMON TO BOTH CHANNELS
= CROSSUNDER

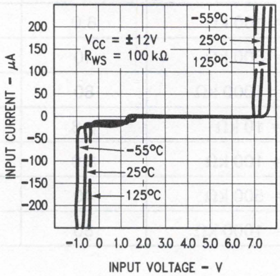
TL/F/9620-2

FIGURE 1. Equivalent Circuit

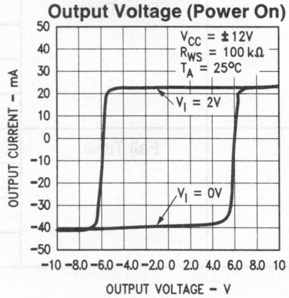
Typical Performance Characteristics



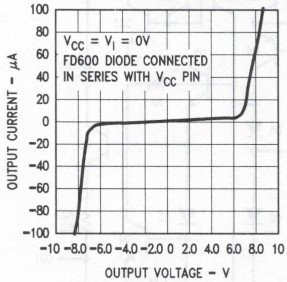
Input/Output Transfer Characteristic vs Temperature



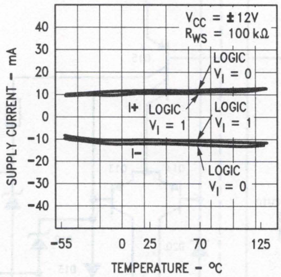
Input Current vs Input Voltage



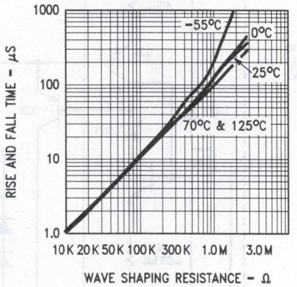
Output Current vs Output Voltage (Power On)



Output Current vs Output Voltage (Power Off)

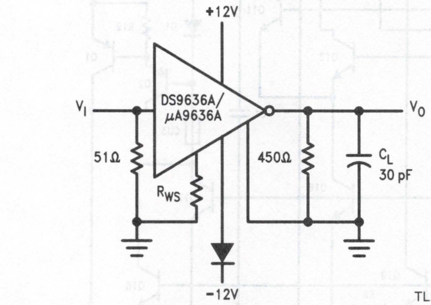


Supply Current vs Temperature



Transition Time vs R_{WS}

TL/F/9620-3



+12V
V_I
DS9636A/ μA9636A
V_O
51Ω
R_{WS}
450Ω
C_L
30 pF
−12V

TL/F/9620-4

V_I

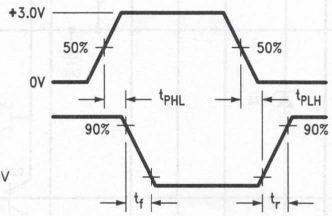
Amplitude: 3.0V

Offset: 0V

Pulse Width: 500 μs

PRR: 1.0 kHz

$t_r = t_f \leq 10$ ns

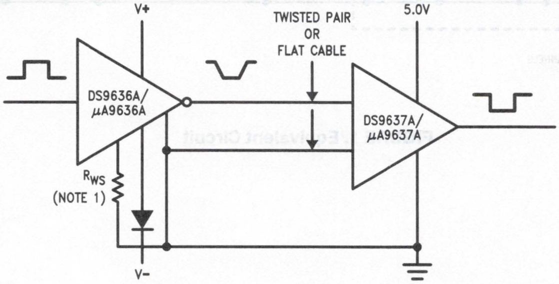


+3.0V
V_I
50%
50%
0V
t_{PHL}
t_{PLH}
90%
90%
V_O
t_f
t_r

TL/F/9620-5

Note: C_L includes jig and probe capacitance

FIGURE 2. AC Test Circuit and Waveforms



V+
TWISTED PAIR OR FLAT CABLE
5.0V
DS9636A/ μA9636A
DS9637A/ μA9637A
R_{WS} (NOTE 1)
V−

Note: Use 1N4448 or equivalent.

TL/F/9620-6

FIGURE 3. RS-423 System Application

National Semiconductor

DS9637A/μA9637A
Dual Differential Line Receiver

General Description

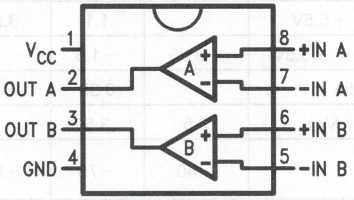
The DS9637A/μA9637A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the DS9637A/μA9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9637A/μA9637A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5V power supply and has Schottky TTL compatible outputs. The DS9637A/μA9637A has an operational input common mode range of ±7V either differentially or to ground.

Features

- Dual channels
- Single 5V supply
- Satisfies EIA standards RS-422 and RS423
- Built-in ±35 mV hysteresis
- High common mode range
- High input impedance
- TTL compatible output
- Schottky technology
- Extended temperature range

Connection Diagram

8-Lead DIP and SO-8 Package



TL/F/9621-1

Top View

Order Number DS9637ACJ, μA9637ARC, DS9637AMJ, μA9637ARM
See NS Package Number J08A*

Order Number DS9637ACM, μA9637ASC
See NS Package Number M08A

Order Number DS9637ACN, μA9637ATC
See NS Package Number N08E

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to + 175°C
Molded DIP	−65°C to + 150°C
Lead Temperature	
Ceramic DIP (Soldering, 30 seconds)	300°C
Molded DIP and SO Package (Soldering, 10 seconds)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
SO Package	810 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW/°C above 25°C.

V_{CC} Lead Potential to Ground	−0.5V to 7.0V
Input Potential to Ground	±15V
Differential Input Voltage	±15V
Output Potential to Ground	−0.5V to +5.5V
Output Sink Current	50 mA

Recommended Operating Conditions

	Min	Max	Units
DS9637AM/μA9637AM			
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temperature (T_A)	−55	+125	°C
DS9637AC/μA9637AC			
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics

Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \leq V_{CM} \leq +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \leq V_{CM} \leq +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \leq V_{CC} \leq +5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \leq V_{CC} \leq +5.5V$	−3.25	−1.6		
V_{OL}	Output Voltage LOW	$I_{OL} = 20$ mA, $V_{CC} = $ Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0$ mA, $V_{CC} = $ Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	$V_O = 0V, V_{CC} = $ Max	−40	−75	−100	mA
I_{CC}	Supply Current	$V_{CC} = $ Max, $V_I+ = 0.5V$, $V_I- = $ GND		35	50	mA
V_{HYST}	Input Hysteresis	$V_{CM} = \pm 7.0V$ (See Curves)		70		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for DS9637AM and across the 0°C to +70°C range for the DS9637ASC. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

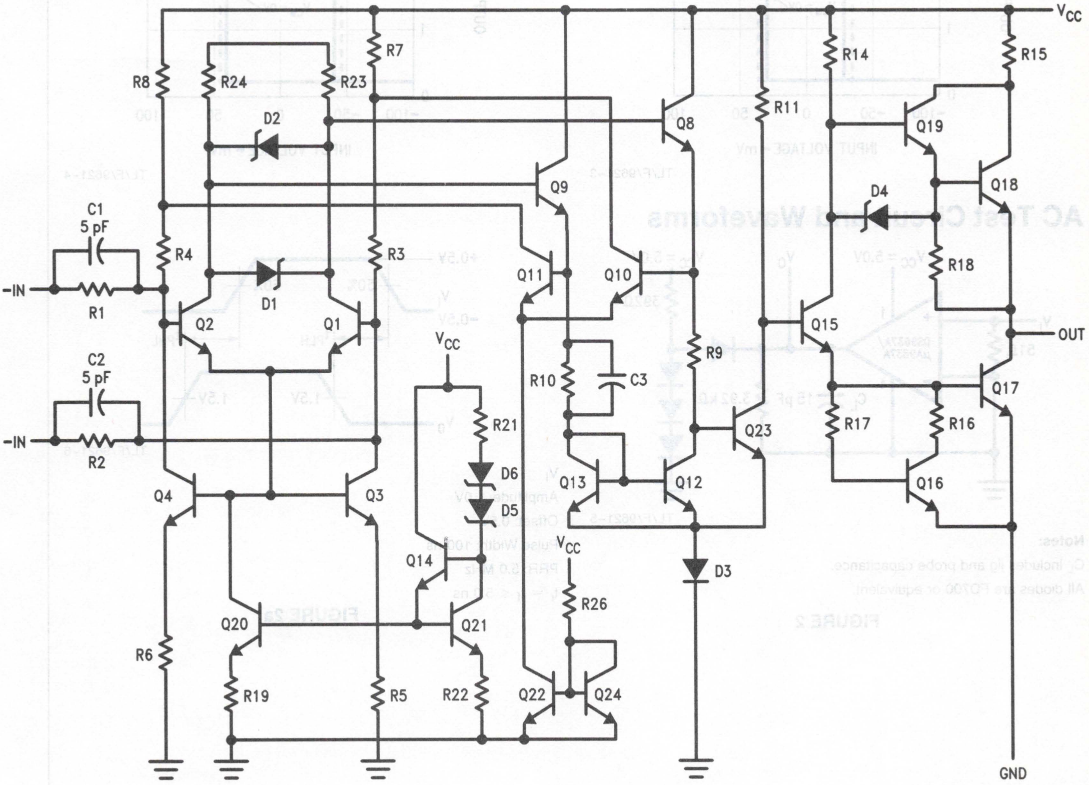
Note 5: V_{DIFF} (Differential Input Voltage) = $(V_I+) - (V_I-)$. V_{CM} (Common Mode Input Voltage) = V_I+ or V_I-.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

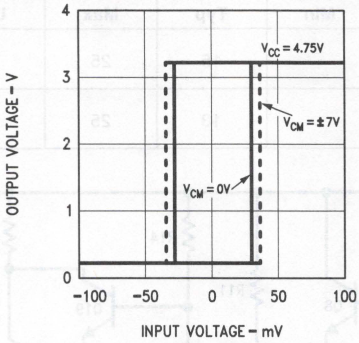
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		15	25	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		13	25	ns


V_CC
R7
R8
R24
R23
D2
Q8
R11
R14
R15
Q19
Q9
Q18
D4
C1
5 pF
R4
R3
Q11
Q10
R18
-IN
R1
D1
Q2
Q1
V_CC
Q15
OUT
R9
C2
5 pF
R10
C3
Q17
-IN
R2
R21
Q23
R17
R16
Q4
Q3
D6
Q13
Q12
Q16
D5
Q14
V_CC
D3
R26
Q20
Q21
R6
R19
R5
R22
Q22
Q24
GND

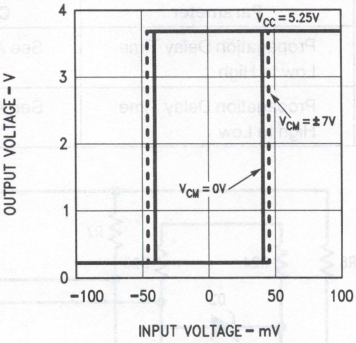
TL/F/9621-2

FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics

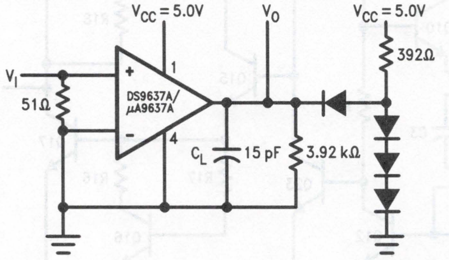


TL/F/9621-3



TL/F/9621-4

AC Test Circuit and Waveforms


$V_{CC} = 5.0V$
V_O
$V_{CC} = 5.0V$
392Ω
V_I
51Ω
+
−
1
4
DS9637A/ μA9637A
C_L
15 pF
3.92 kΩ

TL/F/9621-5

Notes:

C_L includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 2

V_I

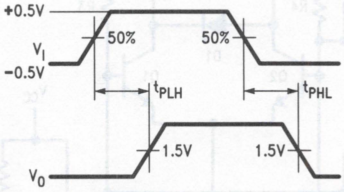
Amplitude: 1.0V

Offset: 0.5V

Pulse Width: 100 ns

PRR: 5.0 MHz

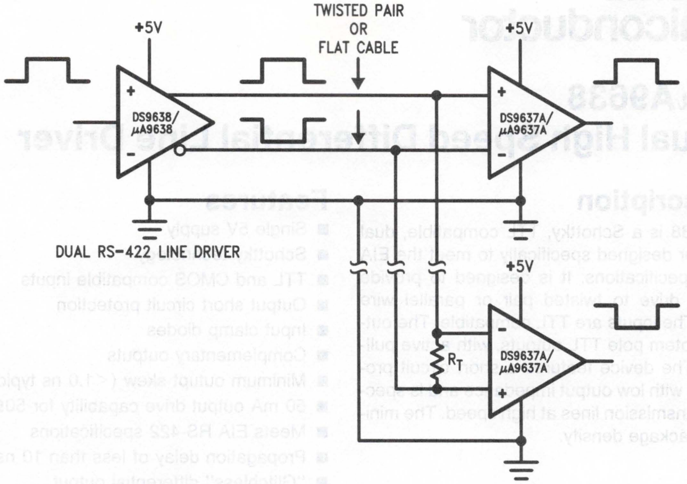
$t_r = t_f \leq 5.0$ ns


+0.5V
V_I
−0.5V
50%
50%
t_{PLH}
t_{PHL}
V_O
1.5V
1.5V

TL/F/9621-6

FIGURE 2a

Typical Applications


+5V
TWISTED PAIR
OR
FLAT CABLE
+5V
+
DS9638/
μA9638
-
+
DS9637A/
μA9637A
-
DUAL RS-422 LINE DRIVER
+5V
-
R_T
DS9637A/
μA9637A
+

TL/F/9621-7

FIGURE 3. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

Notes:

$R_T \geq 50\Omega$ for RS-422 operation.

R_T combined with input impedance of receivers must be greater than 90Ω.

National Semiconductor

PRELIMINARY

DS9638/μA9638
RS-422 Dual High Speed Differential Line Driver

General Description

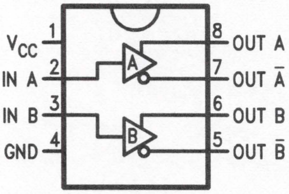
The DS9638/μA9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50Ω transmission lines at high speed. The mini-DIP provides high package density.

Features

- Single 5V supply
- Schottky technology
- TTL and CMOS compatible inputs
- Output short circuit protection
- Input clamp diodes
- Complementary outputs
- Minimum output skew (<1.0 ns typical)
- 50 mA output drive capability for 50Ω transmission lines
- Meets EIA RS-422 specifications
- Propagation delay of less than 10 ns
- "Glitchless" differential output
- Delay time stable with V_{CC} and temperature variations (<2.0 ns typical) *(Figure 3)*
- Extended temperature range

Connection Diagram

8-Lead DIP and SO-8 Package



TL/F/9622–1

Top View

Order Number DS9638MJ, μA9638RM, DS9638CJ or μA9638RC
See NS Package Number J08A*

Order Number DS9638CM or μA9638SC
See NS Package Number M08A

Order Number DS9638CN or μA9638TC
See NS Package Number N08E

*For most current package information: contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO Package (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
SO Package	810 mW
V_{CC} Lead Potential to Ground	−5V to 7V
Input Voltage	−0.5V to +7V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW°C above 25°C.

Recommended Operating Conditions

	DS9638M/μA9638M			DS9638C/μA9638C			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Supply Voltage (V_{CC})	4.5	5.0	5.5	4.75	5.0	5.25	V
Output Current HIGH (I_{OH})			−50			−50	mA
Output Current LOW (I_{OL})				40		50	mA
Operating Temperature (T_A)	−55	25	125	0	25	70	°C

Electrical Characteristics

Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW	0°C to +70°C			0.8	V
		−55°C to +125°C			0.5	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA		−1.0	−1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $V_{IH} = V_{IH\,Min}$, $V_{IL} = V_{IL\,Max}$; I_{OH} = −10 mA	2.5	3.5		V
		I_{OH} = −40 mA	2.0			
V_{OL}	Output Voltage LOW	V_{CC} = Min, $V_{IH} = V_{IH\,Min}$, $V_{IL} = V_{IL\,Max}$, I_{OL} = 40 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_{I\,Max}$ = 5.5V			50	μA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IH} = 2.7V			25	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_{IL} = 0.5V			−200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V (Note 4)	−50		−150	mA
$V_T, \overline{V}_T$	Terminated Output Voltage	See *Figure 1*	2.0			V
$V_T - \overline{V}_T$	Output Balance				0.4	V
$V_{OS}, \overline{V}_{OS}$	Output Offset Voltage				3.0	V
$V_{OS} - \overline{V}_{OS}$	Output Offset Balance				0.4	V
I_X	Output Leakage Current	T_A = 25°C $-0.25V < V_X < 6.0V$			100	μA
I_{CC}	Supply Current (Both Drivers)	V_{CC} = 5.5V, All input at 0V, No Load		45	65	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics provide conditions for actual device operation.

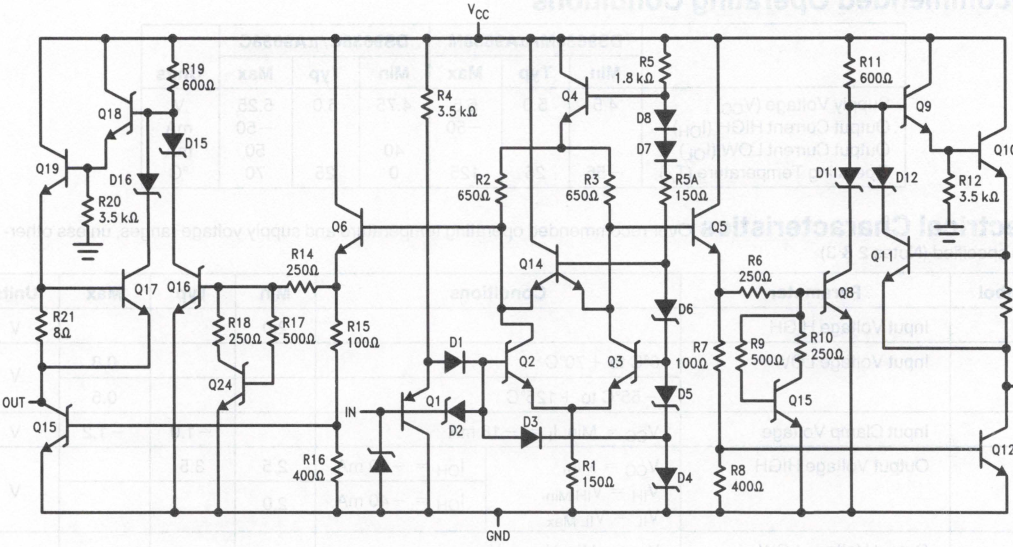
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS9638M and across the 0°C to +70°C range for the DS9638C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$.

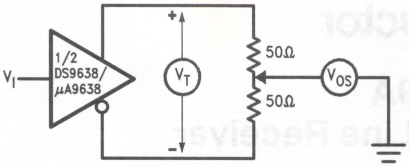
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay	$C_L = 15$ pF $R_L = 100\Omega$, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90%–10%			10	20	ns
t_r	Rise Time, 10%–90%			10	20	ns
$t_{PO}-t_{\overline{PO}}$	Skew Between Outputs A/$\overline{A}$ and B/$\overline{B}$			1.0		ns


V_CC
R19 600Ω
Q18
D15
Q19
D16
R20 3.5 kΩ
Q17
Q16
R21 8Ω
OUT
Q15
R4 3.5 kΩ
Q6
R14 250Ω
R18 250Ω
R17 500Ω
R15 100Ω
Q24
R16 400Ω
IN
Q1
D1
D2
Q4
R2 650Ω
R3 650Ω
Q14
Q2
Q3
D3
R1 150Ω
GND
R5 1.8 kΩ
D8
D7
R5A 150Ω
Q5
D6
R7 100Ω
D5
D4
R8 400Ω
R6 250Ω
Q8
R9 500Ω
R10 250Ω
Q15
R11 600Ω
Q9
Q10
D11
D12
R12 3.5 kΩ
Q11
R13 8Ω
OUT
Q12

TL/F/9622-2

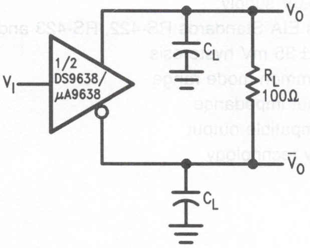
FIGURE 1. Equivalent Circuit

DC Test Circuit


V_I
1/2
DS9638/
μA9638
+
V_T
-
50Ω
50Ω
V_{OS}

TL/F/9622-3

FIGURE 2. Terminated Output Voltage and Output Balance


V_I
1/2
DS9638/
μA9638
V_O
C_L
R_L
100Ω
V̄_O
C_L

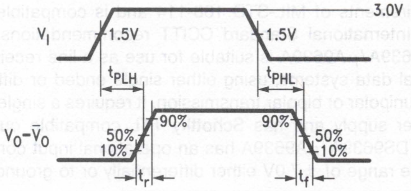
TL/F/9622-4

Note:

The pulse generator has the following characteristics:
PRR = 500 kHz, t_W = 100 ns,
$t_r \le 5.0$ ns, $Z_O = 50\Omega$.

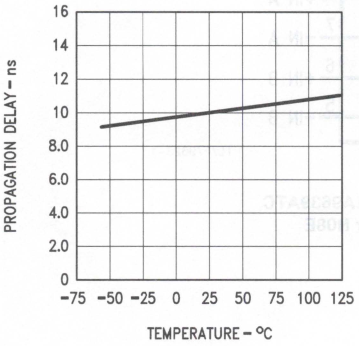
C_L includes probe and jig capacitance.

FIGURE 3. AC Test Circuit and Voltage Waveform


3.0V
V_I
1.5V
1.5V
t_{PLH}
t_{PHL}
V_O-V̄_O
90%
90%
50%
50%
10%
10%
t_r
t_f

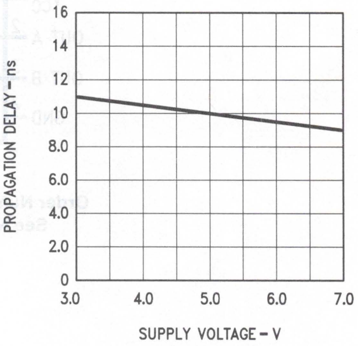
TL/F/9622-5

FIGURE 3a



TL/F/9622-6

FIGURE 4. Typical Delay Characteristics



TL/F/9622-7

FIGURE 4a

National Semiconductor

DS9639A/μA9639A Dual Differential Line Receiver

General Description

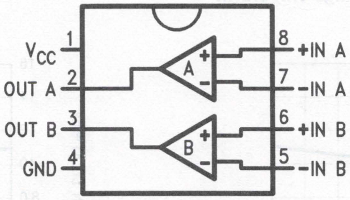
The DS9639A/μA9639A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422, RS-423 and RS-232C. In addition, the DS9639A/μA9639A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9639A/μA9639A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5.0V power supply and has Schottky TTL compatible outputs. The DS9639A/μA9639A has an operational input common mode range of ±7.0V either differentially or to ground.

Features

- Dual channels
- Single 5.0V supply
- Satisfies EIA Standards RS-422, RS-423 and RS-232C
- Built-in ±35 mV hysteresis
- High common mode range
- High input impedance
- TTL compatible output
- Schottky technology

Connection Diagram

8-Lead DIP



TL/F/9623–1

Top View

Order Number DS9639ACN/μA9639ATC
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature Molded DIP (soldering, 10 sec.)	265°C
V_{CC} Lead Potential to Ground	−0.5V to +7.0V
Input Potential to Ground Lead	±25V
Differential Input Voltage	±25V
Output Differential to Ground Lead	−0.5V to 5.5V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	930 mW

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions (Note 1)	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \leq V_{CM} \leq +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \leq V_{CM} \leq +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \leq V_{CC} \leq 5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \leq V_{CC} \leq 5.5V$	−3.25	−1.6		
V_{OL}	Output Voltage LOW	$I_{OL} = 20$ mA, $V_{CC} =$ Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0$ mA, $V_{CC} =$ Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	$V_O = 0V, V_{CC} =$ Max	−40	−75	−100	mA
I_{CC}	Supply Current	$V_{CC} =$ Max, $V_I+ = 0.5V$, $V_I- =$ GND		35	50	mA
V_{HYST}	Input Hysteresis	$V_{CM} = \pm 7.0V$ (See Curves)		70		mV

Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		55	85	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		50	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS9639A. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

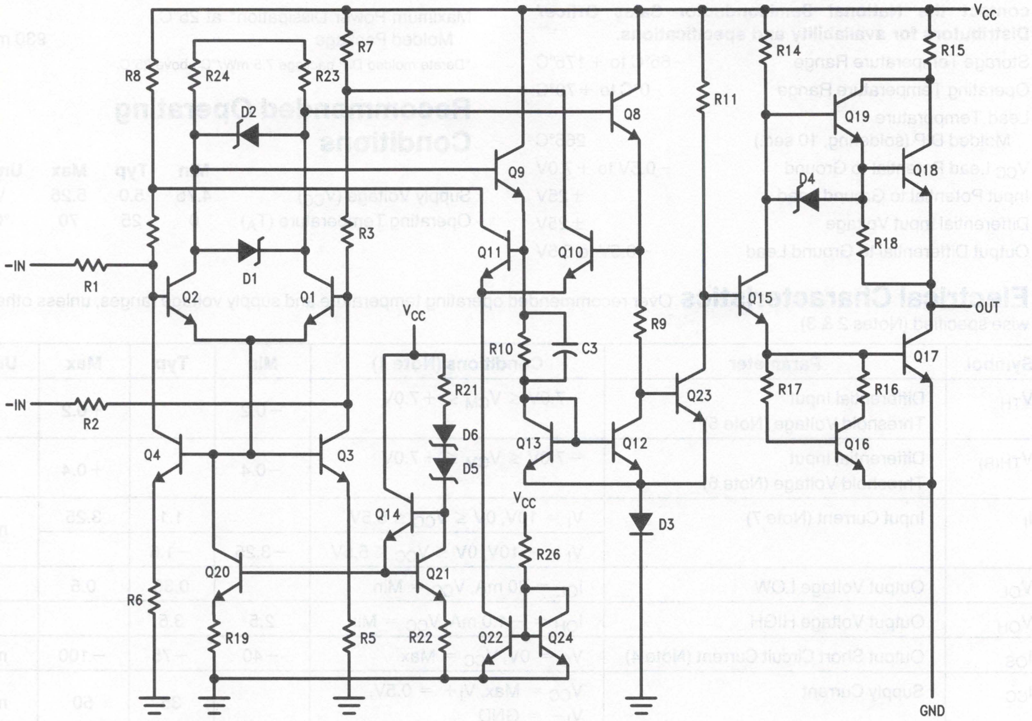
Note 4. Only one output at a time should be shorted.

Note 5: V_{DIFF} (Differential Input Voltage) $= (V_{I+}) - (V_{I-})$. V_{CM} (Common Mode Input Voltage) $= V_{I+}$ or V_{I-}.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

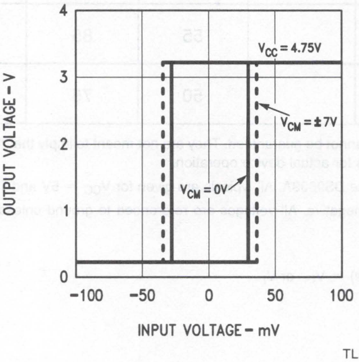
Equivalent Circuit


VCC
R8
R24
R23
R7
D2
R14
R15
R11
Q8
Q19
Q9
Q18
D4
R18
R3
Q11
Q10
-IN
R1
D1
Q2
Q1
Q15
OUT
VCC
R9
R10
C3
Q17
R21
R17
R16
-IN
R2
D6
Q23
D5
Q13
Q12
Q16
Q4
Q3
VCC
Q14
D3
R26
Q20
Q21
R6
R19
R22
R5
Q22
Q24
GND

TL/F/9623-2

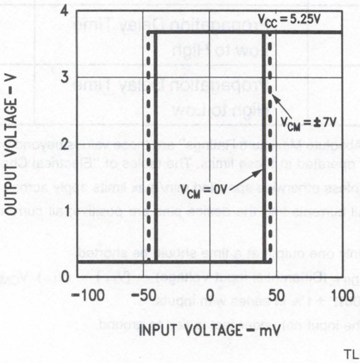
FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics



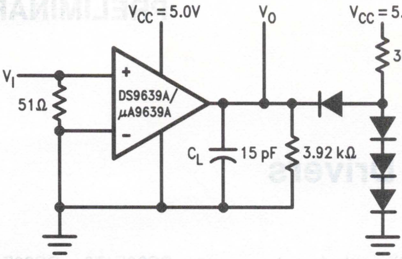
TL/F/9623-3

FIGURE 2



TL/F/9623-4

FIGURE 2a


V$_{CC}$ = 5.0V
V$_O$
V$_{CC}$ = 5.0V
392Ω
V$_I$
51Ω
DS9639A/ μA9639A
+
−
C$_L$
15 pF
3.92 kΩ

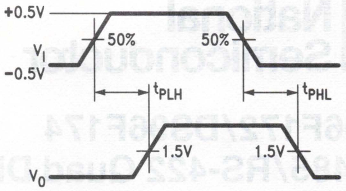
TL/F/9623–5

Notes:

C$_L$ includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 3. AC Test Circuit and Waveforms


+0.5V
V$_I$
−0.5V
50%
50%
t$_{PLH}$
t$_{PHL}$
1.5V
1.5V
V$_O$

TL/F/9623–6

V$_I$

Amplitude: 1.0V

Offset: 0.5V

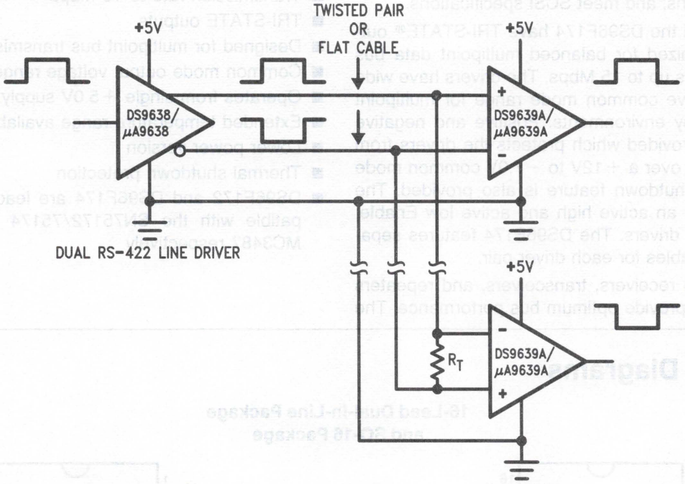
Pulse Width: 500 ns

PRR: 1 MHz

$t_r = t_f \leq 5.0$ ns

FIGURE 3a

Typical Applications


+5V
DS9638/ μA9638
DUAL RS–422 LINE DRIVER
TWISTED PAIR OR FLAT CABLE
+5V
+
−
DS9639A/ μA9639A
+5V
−
+
R$_T$
DS9639A/ μA9639A

TL/F/9623–7

Notes:

R$_t$ ≥ 50Ω for RS-422 operation.

R$_t$ combined with input impedance of receivers must be greater than 90Ω.

FIGURE 4. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

National Semiconductor

PRELIMINARY

DS96F172/DS96F174
RS-485/RS-422 Quad Differential Drivers

General Description

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The DS96F172 and the DS96F174 offer improved performance due to the use of new, state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS96F172 and the DS96F174 feature lower power, extended temperature range, improved RS-485 specifications, and meet SCSI specifications.

The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

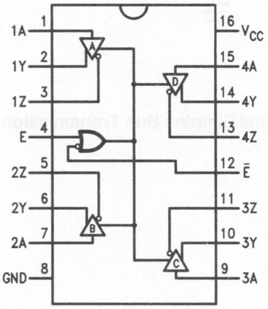
Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96F173, DS96F175, DS36F95, DS96F177 and DS96F178.

Features

- Meets EIA Standard RS-485 and RS-422A
- Meets SCSI specifications
- Monotonic differential output switching
- Transmission rate to 10 Mbps
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7.0V to +12V
- Operates from single +5.0V supply
- Extended temperature range available
- Lower power version
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

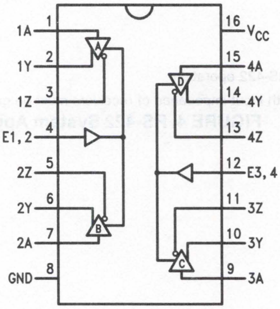
Connection Diagrams

16-Lead Dual-In-Line Package and SO-16 Package



TL/F/9625–1

Top View



TL/F/9625–2

Top View

Order Number DS96F172CJ, DS96F172MJ, DS96F174CJ or DS96F174MJ
See NS Package Number J16A*

Order Number DS96F172CM or DS96F174CM
See NS Package Number M16A

Order Number DS96F172CN or DS96F174CN
See NS Package Number N16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-16	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-16 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F172C/DS96F174C	4.75	5.0	5.25	V
DS96F172M/DS96F174M	4.50	5.0	5.50	
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)				
DS96F172C/DS96F174C	0	+25	+70	°C
DS96F172M/DS96F174M	−55	+25	+125	

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW		$T_A = 0°C$ to $+70°C$			0.8	V
			$T_A = -55°C$ to $+125°C$			0.7	
V_{OH}	Output Voltage HIGH	$I_{OH} = -55$ mA, $V_{CC} = 5.0V$, $T_A = +25°C$ to $+70°C$		3.0			V
V_{OL}	Output Voltage LOW	$I_{OL} = 55$ mA	$T_A = 0°C$ to $+70°C$			2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 54\Omega$, *Figure 1*		1.5	2.0		V
		$R_L = 100\Omega$, *Figure 1*		2.0	2.3		
V_{OD}	Differential Output Voltage	$V_{CM} = -7.0V$ to $+12V$	$T_A = 0°C$ to $+70°C$	1.0			V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω, *Figure 1*				±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0V$, $V_O = -7.0V$ to $+12V$				±50	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0V$ to $+12V$			±20	±50	μA
I_{IH}	Input Current HIGH	$V_I = 2.4V$				20	μA
I_{IL}	Input Current LOW	$V_I = 0.4V$				−50	μA
I_{OS}	Short Circuit Output Current (Note 6)	$V_O = -7.0V$				−250	mA
		$V_O = 0V$				−150	
		$V_O = V_{CC}$				150	
		$V_O = +12V$				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			30	

1

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 2*		15	20	ns
t_{TD}	Differential Output Transition Time			15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, *Figure 3*		12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	16	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 4*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 5*		25	32	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 4*		25	30	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 5*		20	25	ns
t_{SKEW}	Driver Output to Output	$R_L = 60\Omega$		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS96F172M/DS96F174M and across the 0°C to +70°C range for the DS96F172C/DS96F174C. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Only one output at a time should be shorted.

Parameter Measurement Information

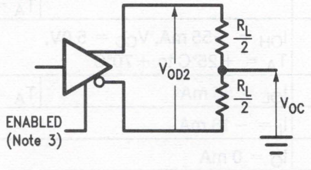


FIGURE 1. Differential and Common Mode Output Voltage

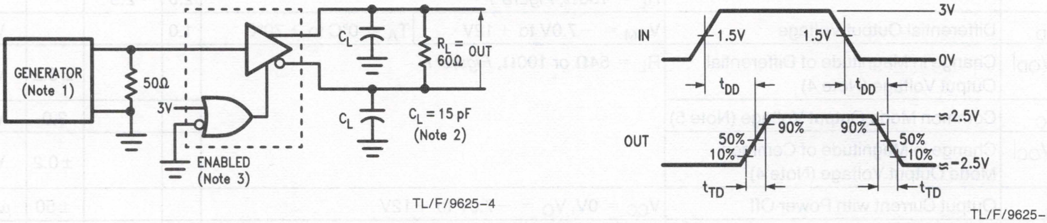
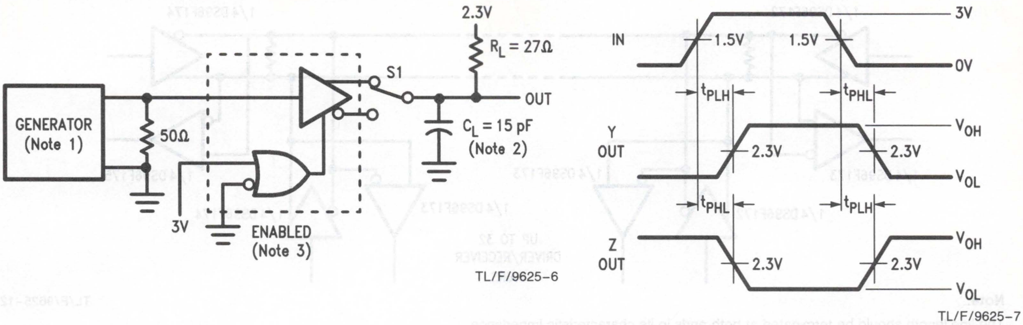


FIGURE 2. Differential Output Delay and Transition Times

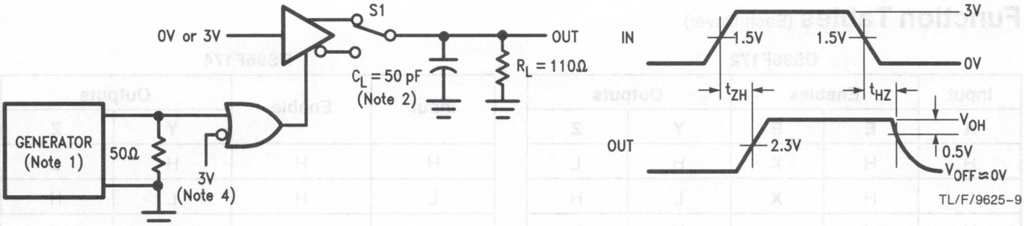
Parameter Measurement Information (Continued)


2.3V
$R_L = 27\Omega$
S1
OUT
GENERATOR (Note 1)
50Ω
$C_L = 15$ pF (Note 2)
3V
ENABLED (Note 3)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
2.3V
2.3V
V_{OH}
V_{OL}

TL/F/9625-6

TL/F/9625-7

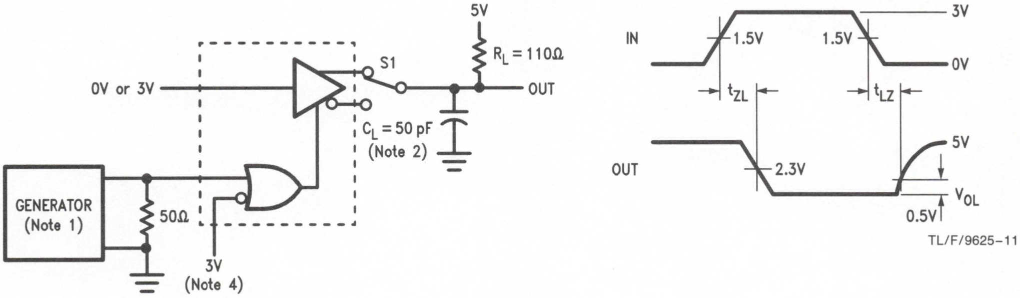
FIGURE 3. Propagation Delay Times


0V or 3V
S1
OUT
$C_L = 50$ pF (Note 2)
$R_L = 110\Omega$
GENERATOR (Note 1)
50Ω
3V (Note 4)
IN
1.5V
1.5V
3V
0V
t_{ZH}
t_{HZ}
OUT
2.3V
V_{OH}
0.5V
$V_{OFF} \approx 0V$

TL/F/9625-9

TL/F/9625-8

FIGURE 4. t_{ZH} and t_{HZ}


5V
$R_L = 110\Omega$
0V or 3V
S1
OUT
$C_L = 50$ pF (Note 2)
GENERATOR (Note 1)
50Ω
3V (Note 4)
IN
1.5V
1.5V
3V
0V
t_{ZL}
t_{LZ}
OUT
2.3V
5V
V_{OL}
0.5V

TL/F/9625-11

TL/F/9625-10

FIGURE 5. t_{ZL} and t_{LZ}

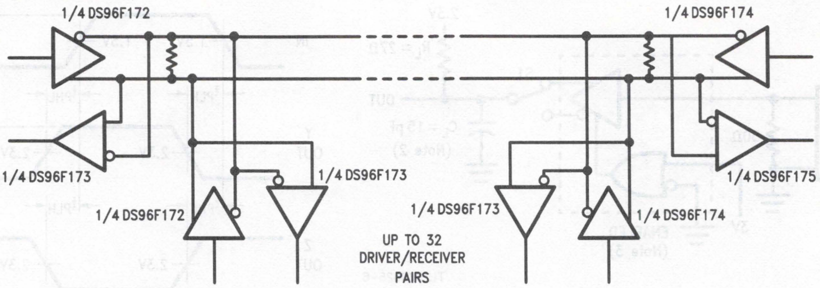
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \le 5.0$ ns, $t_f \le 5.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: DS96F172 with active high and active low Enables is shown here. DS96F174 has active high Enable only.

Note 4: To test the active low Enable $\overline{E}$ of DS96F172 ground E and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Typical Application


1/4 DS96F172
1/4 DS96F174
1/4 DS96F173
1/4 DS96F173
1/4 DS96F175
1/4 DS96F172
1/4 DS96F173
1/4 DS96F174
UP TO 32
DRIVER/RECEIVER
PAIRS

Note:

The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

TL/F/9625-12

FIGURE 6

Function Tables (Each Driver)

DS96F172

Input	Enables		Outputs	
A	**E**	**$\overline{E}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
		Y	**Z**
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

National Semiconductor

DS96172/μA96172/DS96174/μA96174 RS-485/RS-422 Quad Differential Line Drivers

General Description

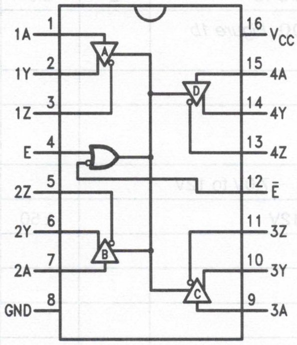
The DS96172/μA96172 and DS96174/μA96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The DS96172/μA96172 features an active high and active low Enable, common to all four drivers. The DS96174/μA96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96173/μA96173, DS96175/μA96175, DS96176/μA96176, DS96177/μA96177 and DS96178/μA96178.

Features

- Meets EIA Standard RS-485 and RS-422A
- Monotonic differential output switching
- Transmission rate to 10 Mbs
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7V to +12V
- Operates from single +5V supply
- Thermal shutdown protection
- DS96172/μA96172/DS96174/μA96174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

Connection Diagrams

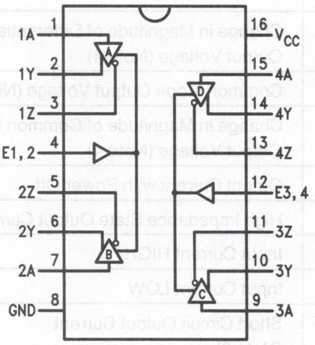
16-Lead DIP
DS96172/μA96172



TL/F/9626-1

Top View

16-Lead DIP
DS96174/μA96174



TL/F/9626-2

Top View

Order Number DS96172J, μA96172DC or DS96174J, μA96174DC
See NS Package Number J16A

Order Number DS96172N, μA96172PC or DS96174N, μA96174PC
See NS Package Number N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Supply Voltage	7V
Enable Input Voltage	5.5V
Maximum Power Dissipation*	25°C
Cavity Package	1500 mW
Molded Package	1040 mW

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Output Voltage (V_{OC})	−7		+12	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

over recommended temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH		2			V
V_{IL}	Input Voltage LOW				0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20$ mA		3.1		V
V_{OL}	Output Voltage LOW	$I_{OL} = 20$ mA		0.8		V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA			6	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 54\Omega$, *Figure 1a*	1.5	2		V
		$R_L = 100\Omega$, *Figure 1b*	2	2.3		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω, *Figure 1b*			±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)				3	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)				±0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0V$, $V_O = -7.0V$ to $12V$			±100	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0V$ to $12V$		±50	±200	μA
I_{IH}	Input Current HIGH	$V_I = 2.7V$			20	μA
I_{IL}	Input Current LOW	$V_I = 0.5V$			−100	μA
I_{OS}	Short Circuit Output Current (Note 6)	$V_O = -7.0V$			−250	mA
		$V_O = 0V$			−150	
		$V_O = V_{CC}$			150	
		$V_O = 12V$			250	
I_{CC}	Supply Current (All Drivers)	No Load Outputs Enabled		50	70	mA
		Output Disabled		50	60	

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 2*		15	25	ns
t_{TD}	Differential Output Transition Time			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, *Figure 3*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 4*		30	45	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 5*		30	45	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 4*		25	35	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 5*		30	45	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96172/µA96172/DS96174/µA96174. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

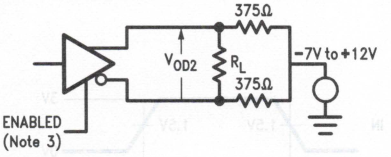
Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

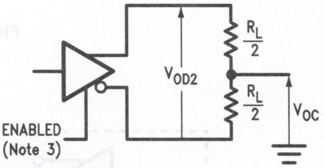
Note 6: Only one output at a time should be shorted.

Parameter Measurement Information



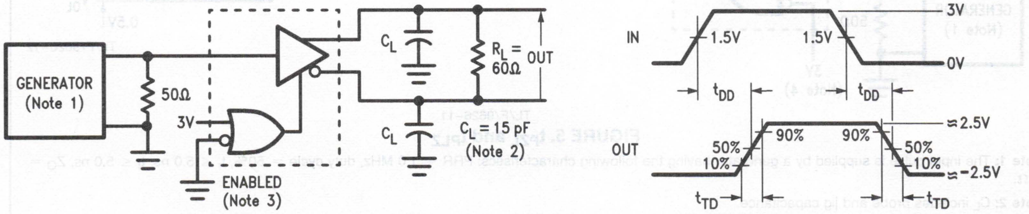
TL/F/9626-3

FIGURE 1. Differential Output Voltage with Varying Common Mode Voltage



TL/F/9626-4

FIGURE 1a. Differential and Common Mode Output Voltage

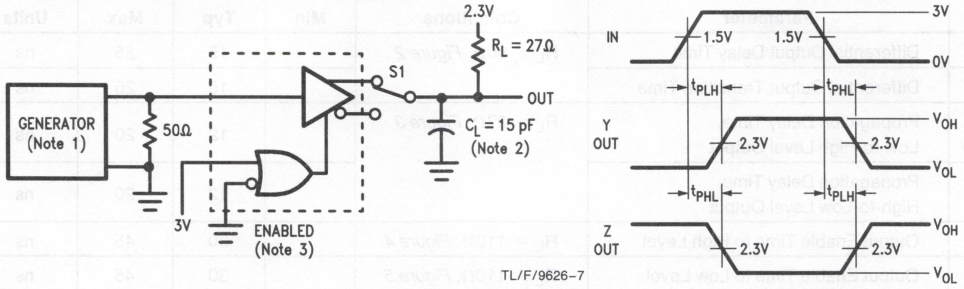


TL/F/9626-5

TL/F/9626-6

FIGURE 2. Differential Output Delay and Transition Times

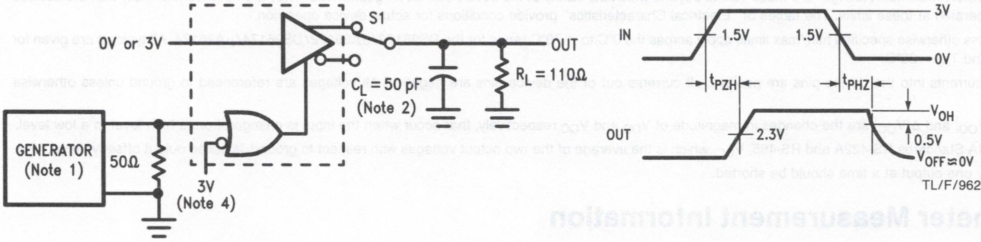
Parameter Measurement Information (Continued)


GENERATOR (Note 1)
50Ω
3V
ENABLED (Note 3)
S1
2.3V
$R_L = 27Ω$
OUT
$C_L = 15$ pF (Note 2)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
V_{OH}
V_{OL}

TL/F/9626-7

TL/F/9626-8

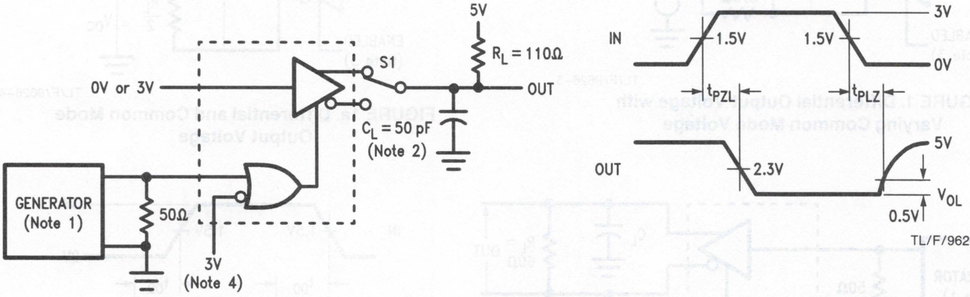
FIGURE 3. Propagation Delay Times


0V or 3V
S1
OUT
$C_L = 50$ pF (Note 2)
$R_L = 110Ω$
GENERATOR (Note 1)
50Ω
3V (Note 4)
IN
1.5V
1.5V
3V
0V
t_{PZH}
t_{PHZ}
OUT
2.3V
V_{OH}
0.5V
$V_{OFF} \approx 0V$

TL/F/9626-10

TL/F/9626-9

FIGURE 4. t_{PZH} and t_{PHZ}


5V
$R_L = 110Ω$
S1
0V or 3V
OUT
$C_L = 50$ pF (Note 2)
GENERATOR (Note 1)
50Ω
3V (Note 4)
IN
1.5V
1.5V
3V
0V
t_{PZL}
t_{PLZ}
OUT
2.3V
5V
V_{OL}
0.5V

TL/F/9626-12

TL/F/9626-11

FIGURE 5. t_{PZL} and t_{PLZ}

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, Z_O = 50Ω.

Note 2: C_L includes probe and jig capacitance.

Note 3: DS96172/μA96172 with active high and active low Enables is shown here. DS96174/μA96174 has active high Enable only.

Note 4: To test the active low Enable $\overline{E}$ of DS96172/μA96172, ground E and apply an inverted waveform to $\overline{E}$. DS96174/μA96174 has active high Enable only.

Function Tables

DS96172/µA96172

Input	Enables		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96174/µA96174

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Typical Application

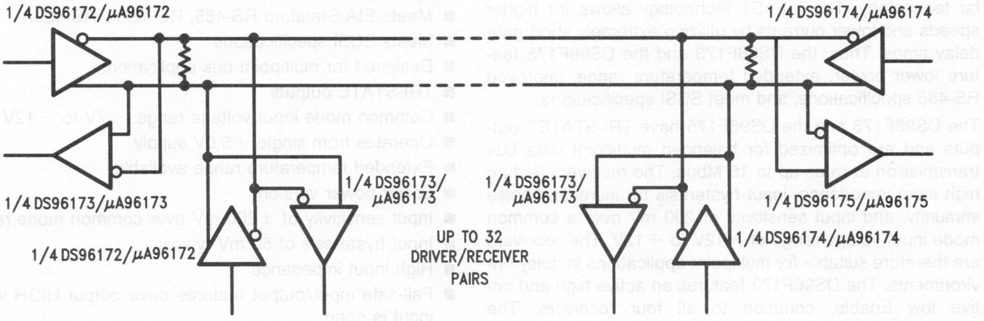

1/4 DS96172/µA96172
1/4 DS96174/µA96174
1/4 DS96173/µA96173
1/4 DS96173/
µA96173
1/4 DS96173/
µA96173
1/4 DS96175/µA96175
1/4 DS96172/µA96172
UP TO 32
DRIVER/RECEIVER
PAIRS
1/4 DS96174/µA96174
TL/F/9626–13

FIGURE 6

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

PRELIMINARY

DS96F173/DS96F175
RS-485/RS-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The DS96F173 and the DS96F175 offer improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS96F173 and the DS96F175 feature lower power, extended temperature range, improved RS-485 specifications, and meet SCSI specifications.

The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input volage range of −12V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96F172/DS96F174, DS36F95 and DS96F177/DS96F178.

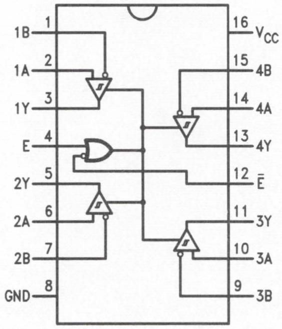
Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Meets SCSI specifications
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Extended temperature range available
- Lower power version
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Fail-safe input/output features drive output HIGH when input is open
- DS96F173 and DS96F175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively

Connection Diagrams

16-Lead DIP and SO-16 Package

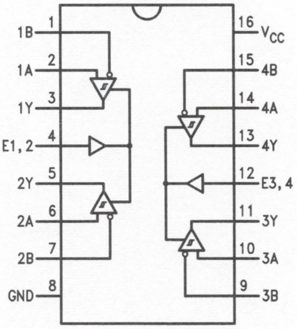
DS96F173



TL/F/9627-1

Top View

DS96F175



TL/F/9627-2

Top View

Order Number DS96F173CJ, DS96F173MJ,
DS96F175CJ or DS96F175MJ
See NS Package Number J16A*

Order Number DS96F173CM or DS96F175CM
See NS Package Number M16A

Order Number DS96F173CN or DS96F175CN
See NS Package Number N16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-16	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-16 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
SO Package	960 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F173C/DS96F175C	4.75	5.0	5.25	V
DS96F173M/DS96F175M	4.50	5.0	5.50	
Common Mode Input Voltage V_{CM}	−7		+12	V
Differential Input Voltage (Note 2) (V_{ID})	−7		+12	V
Output Current HIGH (I_{OH})			−400	µA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)				
DS96F173C/DS96F175C	0	25	70	°C
DS96F173M/DS96F175M	−55	25	125	

Electrical Characteristics over recommended operating conditions, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV	0°C to +70°C	2.8			V
		$I_{OH} = -400$ µA	−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4V$ to $2.4V$				±20	µA
I_I	Line Input Current (Note 6)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	µA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	µA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5V$ to $+2.5V$, $C_L = 15$ pF, *Figure 1*	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	$C_L = 15$ pF, *Figure 2*		12	16	ns
t_{ZL}	Output Enable Time to Low Level	$C_L = 15$ pF, *Figure 3*		13	18	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, *Figure 2*		14	20	ns
t_{LZ}	Output Disable Time from Low Level	$C_L = 5.0$ pF, *Figure 3*		14	18	ns
$\lvert t_{PLH}-t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*		1.0	3.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range the DS96F173M/DS96F175M and across the 0°C to +70°C range for the DS96F173C/DS96F175C. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Function Tables

(Each Receiver) DS96F173

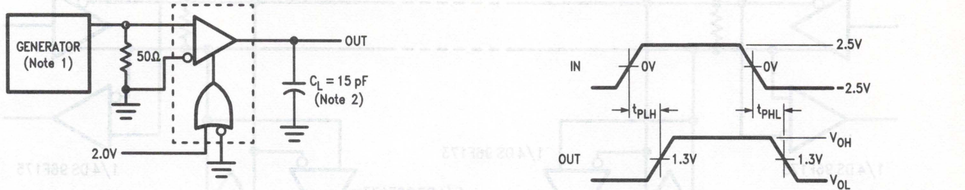
Differential Inputs	Enables		Outputs
A–B	E	Ē	V
$V_{ID} > 0.2V$	H	X	H
	X	L	H
$V_{ID} < -0.2V$	H	X	L
	X	L	L
X	L	H	Z

(Each Receiver) DS96F175

Differential Inputs A–B	Enable	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Immaterial

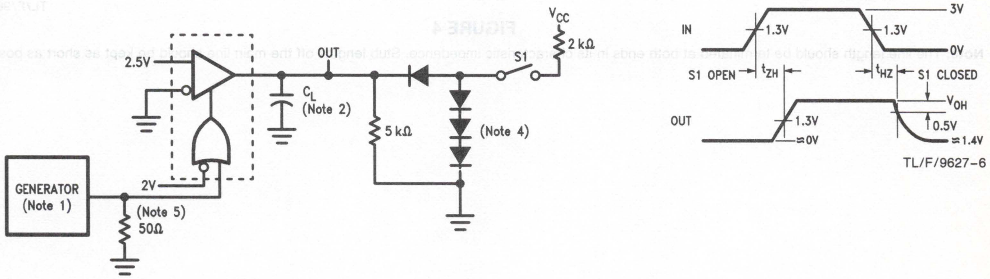
Parameter Measurement Information


GENERATOR (Note 1)
50Ω
OUT
C_L = 15 pF (Note 2)
2.0V
IN
0V
0V
2.5V
−2.5V
t_{PLH}
t_{PHL}
V_{OH}
OUT
1.3V
1.3V
V_{OL}

TL/F/9627-3

TL/F/9627-4

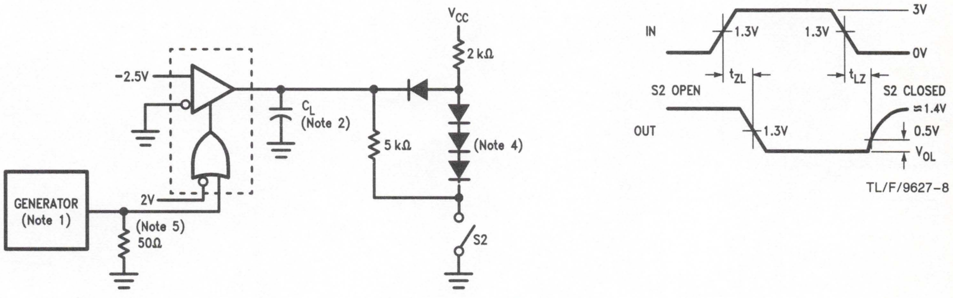
FIGURE 1. t_{PLH}, t_{PHL} (Note 3)


V_{CC}
2 kΩ
S1
OUT
2.5V
C_L (Note 2)
5 kΩ
(Note 4)
GENERATOR (Note 1)
2V
(Note 5) 50Ω
IN
1.3V
1.3V
3V
0V
S1 OPEN
t_{ZH}
t_{HZ}
S1 CLOSED
V_{OH}
OUT
1.3V
≈0V
0.5V
≈1.4V

TL/F/9627-6

TL/F/9627-5

FIGURE 2. t_{HZ}, t_{ZH} (Note 3)


V_{CC}
2 kΩ
−2.5V
C_L (Note 2)
5 kΩ
(Note 4)
GENERATOR (Note 1)
2V
(Note 5) 50Ω
S2
IN
1.3V
1.3V
3V
0V
S2 OPEN
t_{ZL}
t_{LZ}
S2 CLOSED
≈1.4V
OUT
1.3V
0.5V
V_{OL}

TL/F/9627-8

TL/F/9627-7

FIGURE 3. t_{ZL}, t_{LZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \le 6.0$ ns, $t_f \le 6.0$ ns, $Z_O = 50\Omega$.

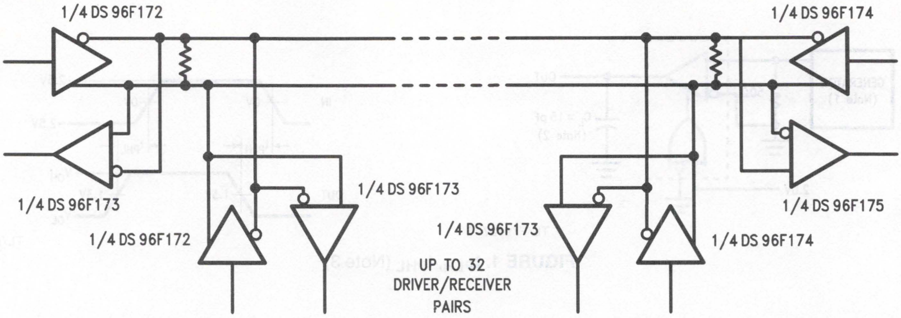
Note 2: C_L includes probe and stray capacitance.

Note 3: DS96F173 with active high and active low Enables is shown here. DS96F175 has active high Enable only.

Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

Typical Application


1/4 DS 96F172
1/4 DS 96F174
1/4 DS 96F173
1/4 DS 96F173
1/4 DS 96F172
1/4 DS 96F173
1/4 DS 96F175
1/4 DS 96F174
UP TO 32
DRIVER/RECEIVER
PAIRS

TL/F/9627-9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96173/μA96173/DS96175/μA96175 RS-485/RS-422 Quad Differential Line Receivers

General Description

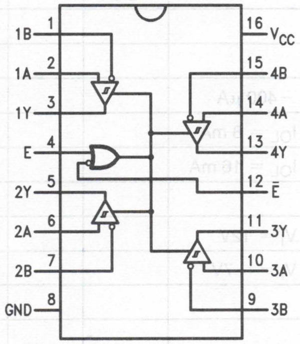
The DS96173/μA96173 and DS96175/μA96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173/μA96173 features an active high and active low Enable, common to all four receivers. The DS96175/μA96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172/μA96172, DS96174/μA96174, DS96176/μA96176, DS96177/μA96177 and DS96178/μA96178.

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE Outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5V supply
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Fail-safe input/output features drive output HIGH when input is open
- DS96173/μA96173/DS96175/μA96175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively.

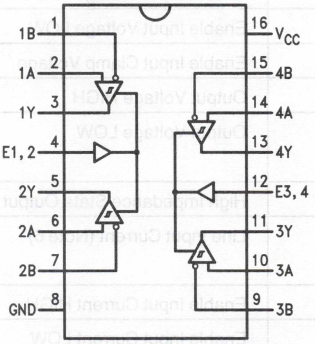
Connection Diagrams

16-Lead DIP
DS96173/μA96173



TL/F/9628-1

16-Lead DIP
DS96175/μA96175



TL/F/9628-2

Order Number DS96173J, μA96173DC, DS96175J, μA96175DC
See NS Package Number J16A*

Order Number DS96173N, μA96173PC, DS96175N, μA96175PC
See NS Package Number N16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
Supply Voltage	7V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7V
Low Level Output Current	50 mA

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})	−7		+12	V
Output Current High (I_{OH})			−400	μA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V, I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input (Note 4) Low Threshold Voltage	$V_O = 0.5V, I_O = 16$ mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA				2.7	V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High Impedance State Output	$V_O = 0.4V$ to $2.4V$				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	μA
R_I	Input Resistance			12	15		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96173/μA96173/DS96175/μA96175. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5V$ to 2.5V, $C_L = 15$ pF, *Figure 1*		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, *Figure 2*		15	22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 15$ pF, *Figure 3*		15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, *Figure 2*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, *Figure 3*		24	40	ns

Function Tables

(Each Receiver) DS96173/μA96173

Differential Inputs	Enables		Outputs
A−B	**E**	**$\overline{E}$**	**V**
$V_{ID} > 0.2V$	H	X	H
	X	L	H
$V_{ID} < -0.2V$	H	X	L
	X	L	L
X	L	H	Z

(Each Receiver) DS96175/μA96175

Differential Inputs A−B	Enable	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Parameter Measurement Information

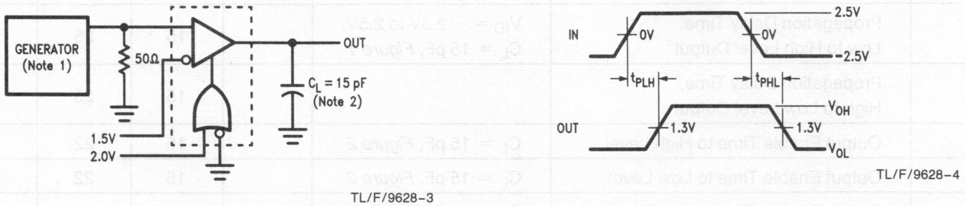

GENERATOR (Note 1)
50Ω
1.5V
2.0V
OUT
C_L = 15 pF (Note 2)
TL/F/9628-3
IN
2.5V
0V
0V
−2.5V
t_{PLH}
t_{PHL}
OUT
V_{OH}
1.3V
1.3V
V_{OL}
TL/F/9628-4

FIGURE 1. t_{PLH}, t_{PHL} (Note 3)

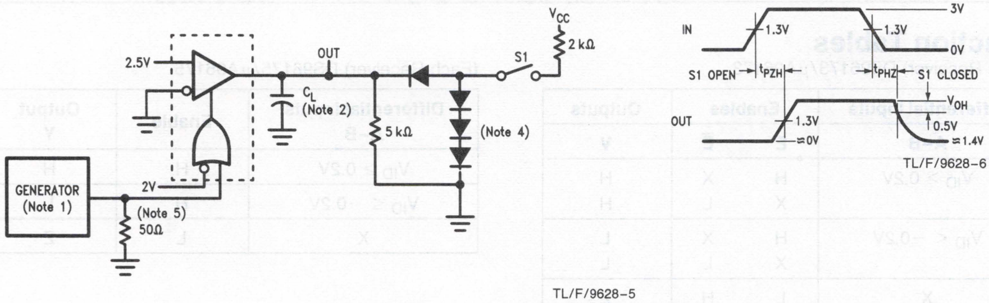

2.5V
OUT
C_L (Note 2)
5 kΩ
S1
V_{CC}
2 kΩ
(Note 4)
GENERATOR (Note 1)
2V
(Note 5)
50Ω
IN
1.3V
1.3V
3V
0V
S1 OPEN
t_{PZH}
t_{PHZ}
S1 CLOSED
OUT
V_{OH}
1.3V
0.5V
≈0V
≈1.4V
TL/F/9628-6
TL/F/9628-5

FIGURE 2. t_{PHZ}, t_{PZH} (Note 3)

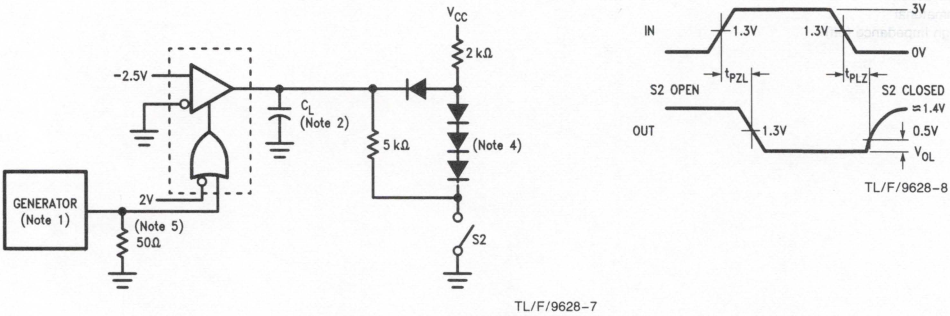

V_{CC}
2 kΩ
−2.5V
C_L (Note 2)
5 kΩ
(Note 4)
GENERATOR (Note 1)
2V
(Note 5)
50Ω
S2
IN
1.3V
1.3V
3V
0V
t_{PZL}
t_{PLZ}
S2 OPEN
S2 CLOSED
≈1.4V
OUT
1.3V
0.5V
V_{OL}
TL/F/9628-8
TL/F/9628-7

FIGURE 3. t_{PZL}, t_{PLZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

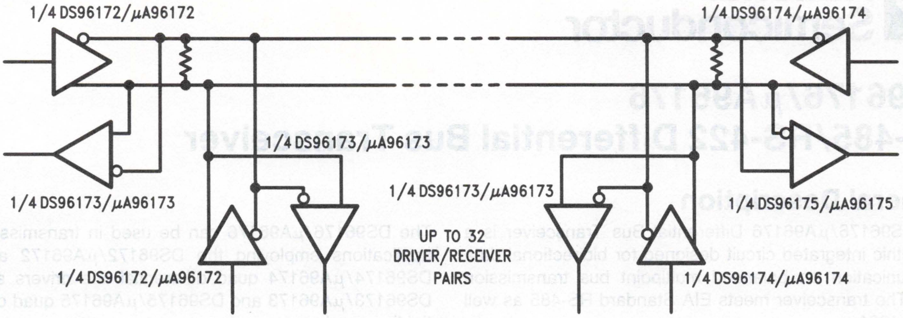
Note 2: C_L includes probe and stray capacitance.

Note 3: DS96173/μA96173 with active high and active low Enables is shown here. DS96175/μA96175 has active high Enable only.

Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96173/μA96173, ground E and apply an inverted input waveform to $\overline{E}$. DS96175/μA96175 has active high Enable only.

Typical Application


1/4 DS96172/μA96172
1/4 DS96174/μA96174
1/4 DS96173/μA96173
1/4 DS96173/μA96173
1/4 DS96173/μA96173
1/4 DS96175/μA96175
UP TO 32
DRIVER/RECEIVER
PAIRS
1/4 DS96172/μA96172
1/4 DS96174/μA96174

TL/F/9628–9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96176/μA96176
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS96176/μA96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS96176/μA96176 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 15 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

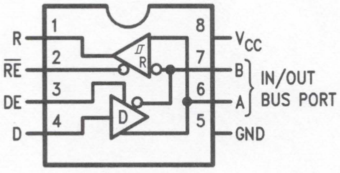
The DS96176/μA96176 can be used in transmission line applications employing the DS96172/μA96172 and the DS96174/μA96174 quad differential line drivers and the DS96173/μA96173 and DS96175/μA96175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability ±60 mA Maximum
- Thermal shutdown protection
- Driver positive and Negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead DIP



TL/F/9630-1

Top View

Order Number DS96176J, μA96176RC
See NS Package Number J08A*

Order Number DS96176N, μA96176TC
See NS Package Number N08E

Function Table

Driver

Differential Inputs	Enable	Outputs	
D	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	$\overline{\textbf{RE}}$	**R**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
Supply Voltage	7.0V
Differential Input Voltage	±25V
Enable Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at Any Bus Terminal (Separately or Common Mode)	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20$ mA			3.1		V
V_{OL}	Output Voltage LOW	$I_{OL} = 20$ mA			0.85		V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\lvert V_{OD1}\rvert$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\lvert V_{OD2}\rvert$	Differential Output Voltage	$R_L = 100\Omega$, *Figure 1*		2.0	2.25		V
		$R_L = 54\Omega$, *Figure 2*		1.5	2.0		
$\Delta\lvert V_{OD}\rvert$	Change in Magnitude of Differential Output Voltage (Note 4)					±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)	$R_L = 54\Omega$ or 100Ω, *Figure 1*				3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 4) (Includes Receiver I_I)	Output Disabled	$V_O = 12V$			1.0	mA
			$V_O = -7.0V$			−0.8	
I_{IH}	Input Current HIGH	$V_I = 2.4V$				20	μA
I_{IL}	Input Current LOW	$V_I = 0.4V$				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0V$				−250	mA
		$V_O = 0V$				−150	
		$V_O = V_{CC}$				150	
		$V_O = 12V$				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V$, $I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0$ mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA, *Figure 3*		2.7			V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV, *Figure 3*	$I_{OL} = 8{,}0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High Impedance State Output	$V_O = 0.45V$ to $2.4V$				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				100	μA
R_I	Input Resistance			12	15		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			40	mA
			Outputs Disabled				

Driver Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	$R_L = 60\Omega$, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 27\Omega$, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 6*		25	35	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 7*		25	35	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 7*		29	35	ns

Receiver Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{ID} = 0V$ to 3.0V $C_L = 15$ pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96176/μA96176. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

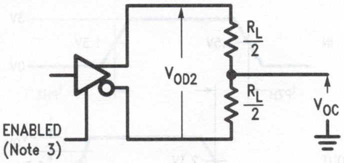
Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standard RS-485 for exact conditions.

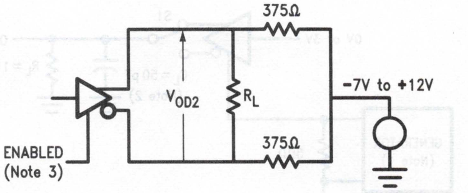
Note 9: Only one output at a time should be shorted.

Parameter Measurement Information



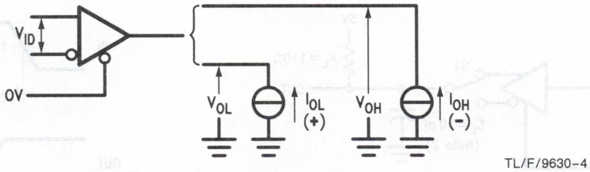
TL/F/9630-2

FIGURE 1. Driver V_{OD} and V_{OC}



TL/F/9630-3

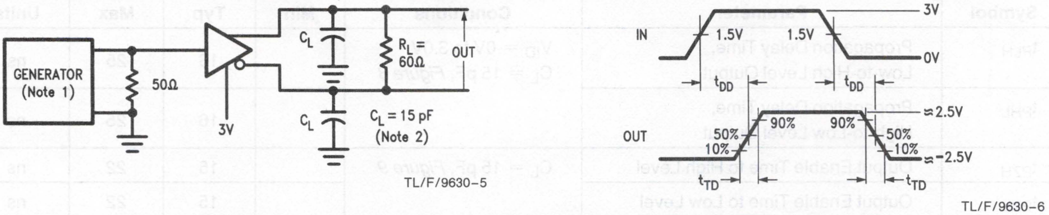
FIGURE 2. Driver V_{OD} with Varying Common Mode Voltage



TL/F/9630-4

FIGURE 3. Receiver V_{OH} and V_{OL}

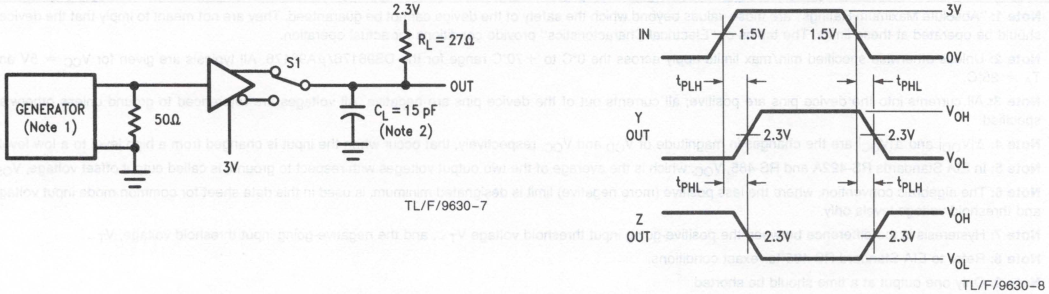
Parameter Measurement Information (Continued)


GENERATOR (Note 1)
50Ω
3V
C_L
C_L
R_L = 60Ω
OUT
C_L = 15 pF (Note 2)
IN
1.5V
1.5V
3V
0V
t_{DD}
t_{DD}
OUT
90%
90%
50%
10%
50%
10%
≈2.5V
≈−2.5V
t_{TD}
t_{TD}

TL/F/9630-5

TL/F/9630-6

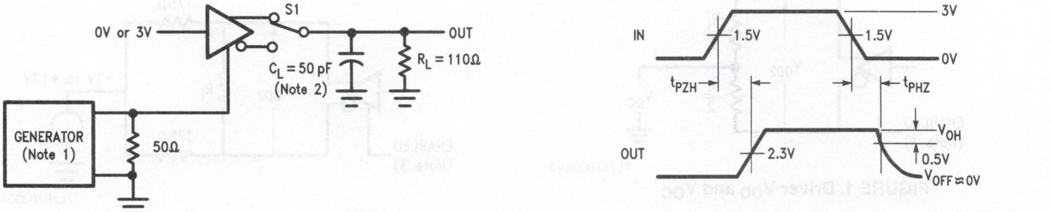
FIGURE 4. Driver Differential Output Delay and Transition Times


2.3V
R_L = 27Ω
S1
OUT
GENERATOR (Note 1)
50Ω
C_L = 15 pF (Note 2)
3V
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
2.3V
2.3V
V_{OH}
V_{OL}

TL/F/9630-7

TL/F/9630-8

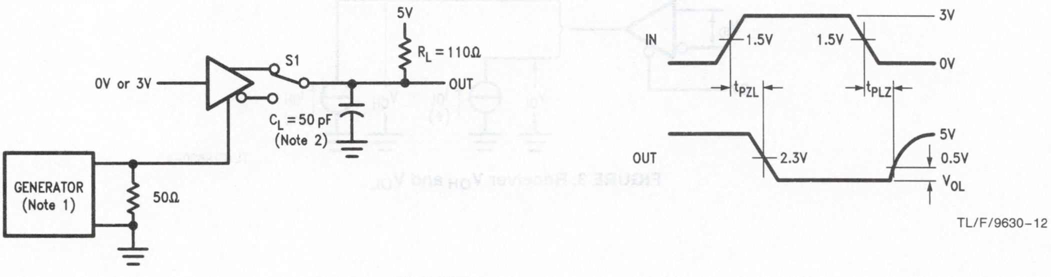
FIGURE 5. Driver Propagation Times


0V or 3V
S1
OUT
C_L = 50 pF (Note 2)
R_L = 110Ω
GENERATOR (Note 1)
50Ω
IN
1.5V
1.5V
3V
0V
t_{PZH}
t_{PHZ}
OUT
2.3V
V_{OH}
0.5V
V_{OFF}≈0V

TL/F/9630-9

TL/F/9630-10

FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

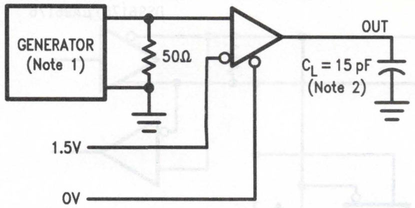

5V
R_L = 110Ω
S1
0V or 3V
OUT
C_L = 50 pF (Note 2)
GENERATOR (Note 1)
50Ω
IN
1.5V
1.5V
3V
0V
t_{PZL}
t_{PLZ}
OUT
2.3V
5V
0.5V
V_{OL}

TL/F/9630-11

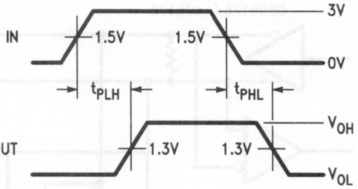
TL/F/9630-12

FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

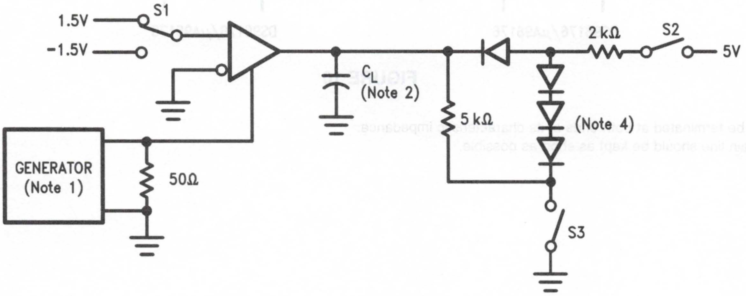

GENERATOR
(Note 1)
50Ω
OUT
C_L = 15 pF
(Note 2)
1.5V
0V

TL/F/9630–13

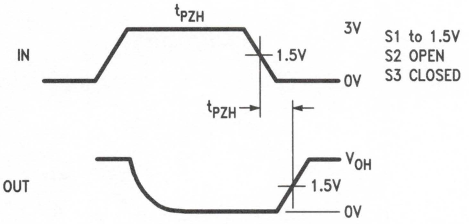

IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
OUT
1.3V
1.3V
V_{OH}
V_{OL}

TL/F/9630–14

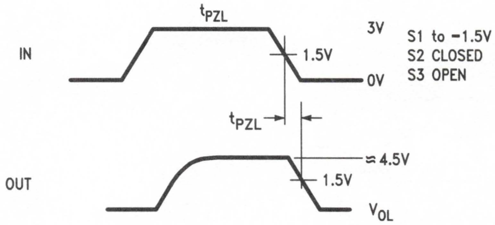
FIGURE 8. Receiver Propagation Delay Times


1.5V
S1
−1.5V
C_L
(Note 2)
GENERATOR
(Note 1)
50Ω
5 kΩ
2 kΩ
S2
5V
(Note 4)
S3

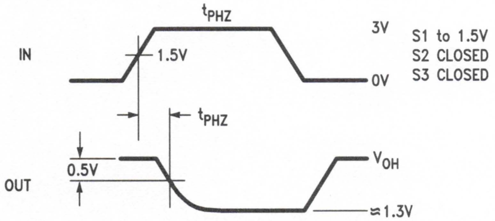
TL/F/9630–15


t_{PZH}
IN
3V
1.5V
0V
S1 to 1.5V
S2 OPEN
S3 CLOSED
t_{PZH}
OUT
V_{OH}
1.5V
0V

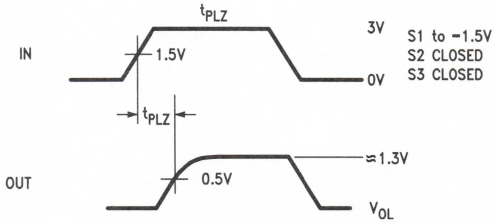
TL/F/9630–16


t_{PZL}
IN
3V
1.5V
0V
S1 to −1.5V
S2 CLOSED
S3 OPEN
t_{PZL}
OUT
≈4.5V
1.5V
V_{OL}

TL/F/9630–17


t_{PHZ}
IN
1.5V
3V
0V
S1 to 1.5V
S2 CLOSED
S3 CLOSED
t_{PHZ}
OUT
0.5V
V_{OH}
≈1.3V

TL/F/9630–18


t_{PLZ}
IN
1.5V
3V
0V
S1 to −1.5V
S2 CLOSED
S3 CLOSED
t_{PLZ}
OUT
0.5V
≈1.3V
V_{OL}

TL/F/9630–19

FIGURE 9. Receiver Enable and Disable Times

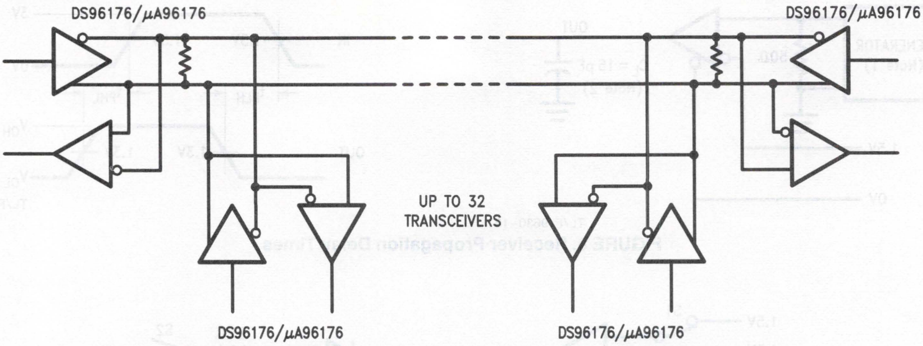
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96176/μA96176 Driver enable is Active-High.

Note 4: All diodes are 1N916 or equivalent.

Typical Application


DS96176/μA96176
DS96176/μA96176
UP TO 32
TRANSCEIVERS
DS96176/μA96176
DS96176/μA96176

TL/F/9630-20

FIGURE 10

Note:

The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

National Semiconductor

PRELIMINARY

DS96F177/DS96F178 RS-485/RS-422 Differential Bus Repeaters

General Description

The DS96F177 and DS96F178 Differential Bus Repeaters are monolithic integrated devices, each designed for one-way data communications on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-485 and RS-422A.

The DS96F177 and DS96F178 offer improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by using extremely short gate delay times. Thus, the DS96F177 and the DS96F178 feature lower power, extended temperature range, improved RS-485 specifications, and meet SCSI specifications.

Each device is designed to improve the performance of the data communication over long bus lines. The DS96F177 and DS96F178 are identical except for the Enable inputs, which are complementary. The DS96F177 is an active high Enable. The DS96F178 is an active low Enable. These complementary Enables allow the devices to be used in pairs for bidirectional communications.

The DS96F177 and DS96F178 feature positive and negative current limiting and TRI-STATE® outputs for the receiver and driver. The driver features thermal shutdown for protection from line fault conditions. The driver is designed to drive current loads up to 60 mA maximum.

The DS96F177 and DS96F178 are designed for optimum performance when used on transmission buses employing the DS96F172 and DS96F174 differential line drivers, DS96F173 and DS96F175 differential line receivers, or DS36F95 differential bus tranceiver.

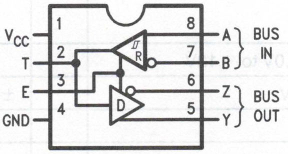
Features

- Meets EIA Standard RS-422A and RS-485
- Meets SCSI specifications
- Designed for multipoint transmission on long bus lines in noisy environments
- TRI-STATE outputs
- Bus voltage range −7.0V to 12V
- Positive and negative current limiting
- Driver output capability ±60 mA max
- Driver thermal shutdown protection
- Receiver input high impedance
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Extended temperature range available
- Lower power version
- DS96F177 and DS96F178 are lead and function compatible with SN75177 and SN75178 respectively

Connection Diagrams

8-Lead Dual-In-Line Package and SO-8 Package

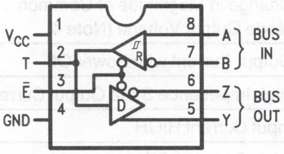
DS96F177



TL/F/9631-1

Top View

DS96F178



TL/F/9631-2

Top View

Order Number DS96F177CJ, DS96F177MJ, DS96F178CJ or DS96F178MJ
See NS Package Number J08A*

Order Number DS96F177CM or DS96F178CM
See NS Package Number M08A

Order Number DS96F177CN or DS96F178CN
See NS Package Number N08E

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*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-8 (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
SO Package	810 mW
Supply Voltage	7.0V
Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F177C/DS96F178C	4.75	5.0	5.25	V
DS96F177M/DS96F178M	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (V_I or V_{CM}) (Separately or Common Mode)	−7.0		12	V
Differential Input Voltage(V_{ID}) (Note 2)			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	
Operating Temperature (T_A)				
DS96F177C/DS96F178C	0	25	70	°C
DS96F177M/DS96F178M	−55	25	125	°C

Driver Electrical Characteristics

Over recommended operation conditions, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -55$ mA	0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	$I_{OH} = 55$ mA	0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.3	V
$\lvert V_{OD1}\rvert$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\lvert V_{OD2}\rvert$	Differential Output Voltage	$R_L = 100\Omega$ *Figure 1*		2.0	2.25		V
		$R_L = 54\Omega$ *Figure 1*		1.5	2.0		
$\lvert V_{OD3}\rvert$	Differential Output Voltage	$V_{CM} = -7.0V$ to $+12V$	0°C to +70°C	1.5			V
$\Delta\lvert V_{OD}\rvert$	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω, *Figure 1*				±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)					3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0V$, $V_O = -7.0V$ to $+12V$				±50	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0V$ to $+12V$			±20	±100	μA
I_{IH}	Input Current HIGH	$V_I = 2.4V$				20	μA
I_{IL}	Input Current LOW	$V_I = 0.4V$				−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0V$				−250	mA
		$V_O = 0V$				−150	
		$V_O = V_{CC}$				150	
		$V_O = +12V$				250	
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			28	mA
I_{CCX}			Outputs Disabled			25	

Driver Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 3*	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	25	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$R_L = 27\Omega$, *Figure 4*	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 5*		20	30	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 6*		25	35	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 5*		20	30	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 6*		20	30	ns
t_{SKEW}	Driver Output to Output	$R_L = 60\Omega$		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V$, $I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0$ mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$		35	50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.3	V
V_{OH}	High Level Output Voltage	$V_{ID} = 200$ mV, $I_{OH} = -400\ \mu A$, *Figure 2*	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Low Level Output Voltage	$V_{ID} = -200$ mV, *Figure 2*	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4V$				−360	μA
		$V_O = 2.4V$				20	
I_I	Line Input Current (Note 8)	Other Input = 0V	$V_I = +12V$			1.0	mA
			$V_I = -7.0V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−50	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enable			28	mA
I_{CCX}			Outputs Disabled			25	

Function Tables

DS96F177

Differential Inputs	Enable	Outputs		
A–B	E	T	Y	Z
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

DS96F178

Differential Inputs	Enable	Outputs		
A–B	$\overline{E}$	T	Y	Z
$V_{ID} \geq 0.2V$	L	H	H	L
$V_{ID} \leq -0.2V$	L	L	L	H
X	H	Z	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

Receiver Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{ID} = 0V$ to $+3.0V$ $C_L = 15$ pF, *Figure 7*	12	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	16	22	ns
t_{ZH}	Output Enable TIme to High Level	$C_L = 15$ pF, *Figure 8*		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, *Figure 8*		12	25	ns
t_{LZ}	Output Disable TIme from Low Level			12	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for the DS96F177M/DS96F178M and across the 0°C to +70°C range for the DS96F177C/DS96F178C. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD}, V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

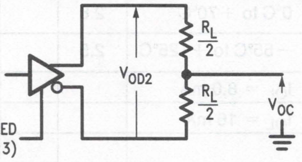
Note 6: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standards RS-485 for exact conditions.

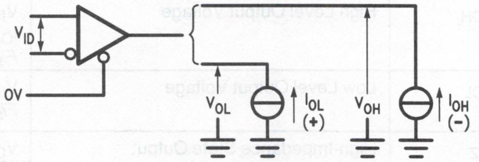
Note 9: Only one output at a time should be shorted.

Parameter Measurement Information



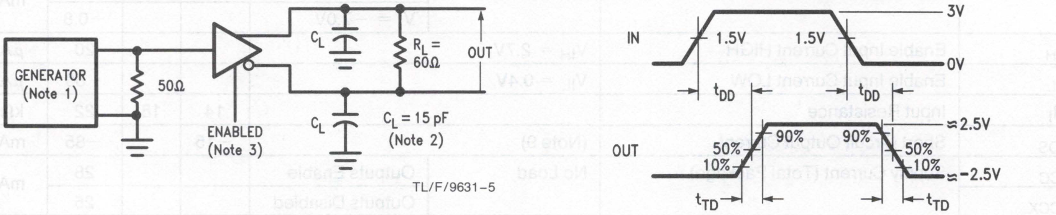
TL/F/9631-3

FIGURE 1. Driver V_{OD2} and V_{OC}



TL/F/9631-4

FIGURE 2. Receiver V_{OH} and V_{OL}

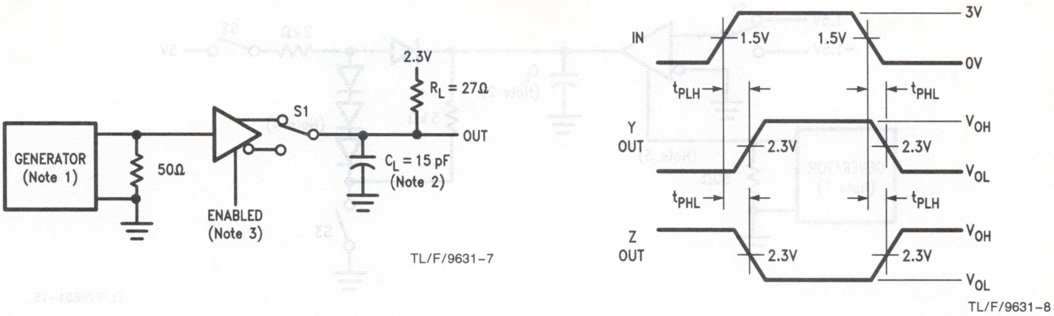


TL/F/9631-5

TL/F/9631-6

FIGURE 3. Driver Differential Output Delay and Transition Times

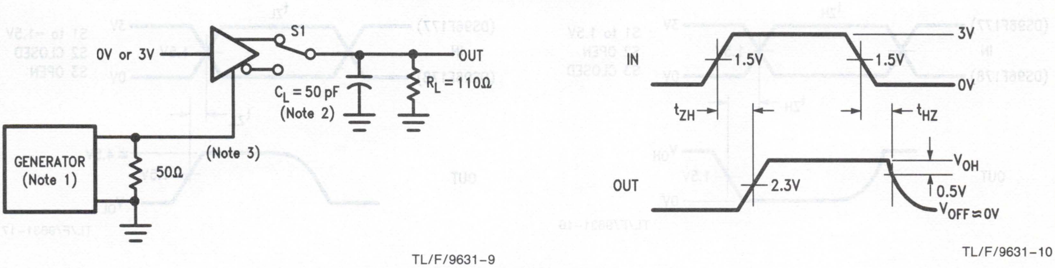
Parameter Measurement Information (Continued)


GENERATOR (Note 1)
50Ω
ENABLED (Note 3)
S1
2.3V
$R_L = 27\Omega$
OUT
$C_L = 15\text{ pF}$ (Note 2)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
2.3V
2.3V
V_{OH}
V_{OL}

TL/F/9631-7

TL/F/9631-8

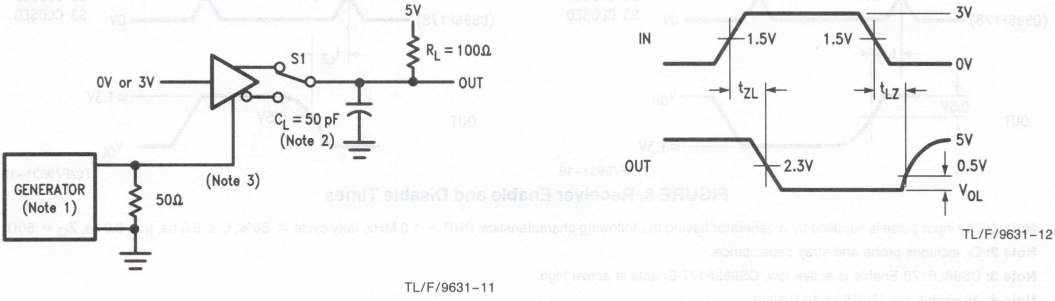
FIGURE 4. Driver Propagation Times


0V or 3V
S1
OUT
$C_L = 50\text{ pF}$ (Note 2)
$R_L = 110\Omega$
GENERATOR (Note 1)
50Ω
(Note 3)
IN
1.5V
1.5V
3V
0V
t_{ZH}
t_{HZ}
OUT
2.3V
V_{OH}
0.5V
$V_{OFF} \approx 0V$

TL/F/9631-9

TL/F/9631-10

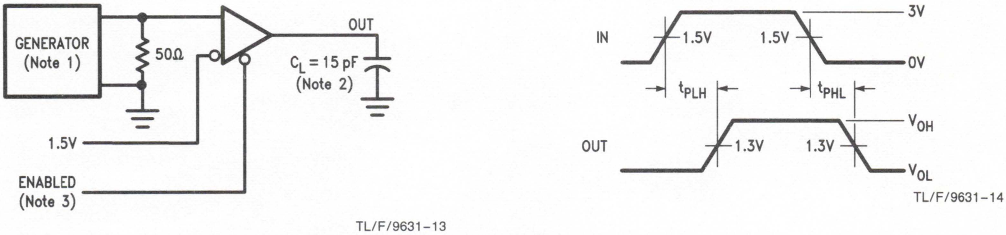
FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ})


5V
$R_L = 100\Omega$
0V or 3V
S1
OUT
$C_L = 50\text{ pF}$ (Note 2)
GENERATOR (Note 1)
50Ω
(Note 3)
IN
1.5V
1.5V
3V
0V
t_{ZL}
t_{LZ}
OUT
2.3V
5V
0.5V
V_{OL}

TL/F/9631-11

TL/F/9631-12

FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ})


GENERATOR (Note 1)
50Ω
OUT
$C_L = 15\text{ pF}$ (Note 2)
1.5V
ENABLED (Note 3)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
OUT
1.3V
1.3V
V_{OH}
V_{OL}

TL/F/9631-13

TL/F/9631-14

FIGURE 7. Receiver Propagation Delay Times

Parameter Measurement Information (Continued)

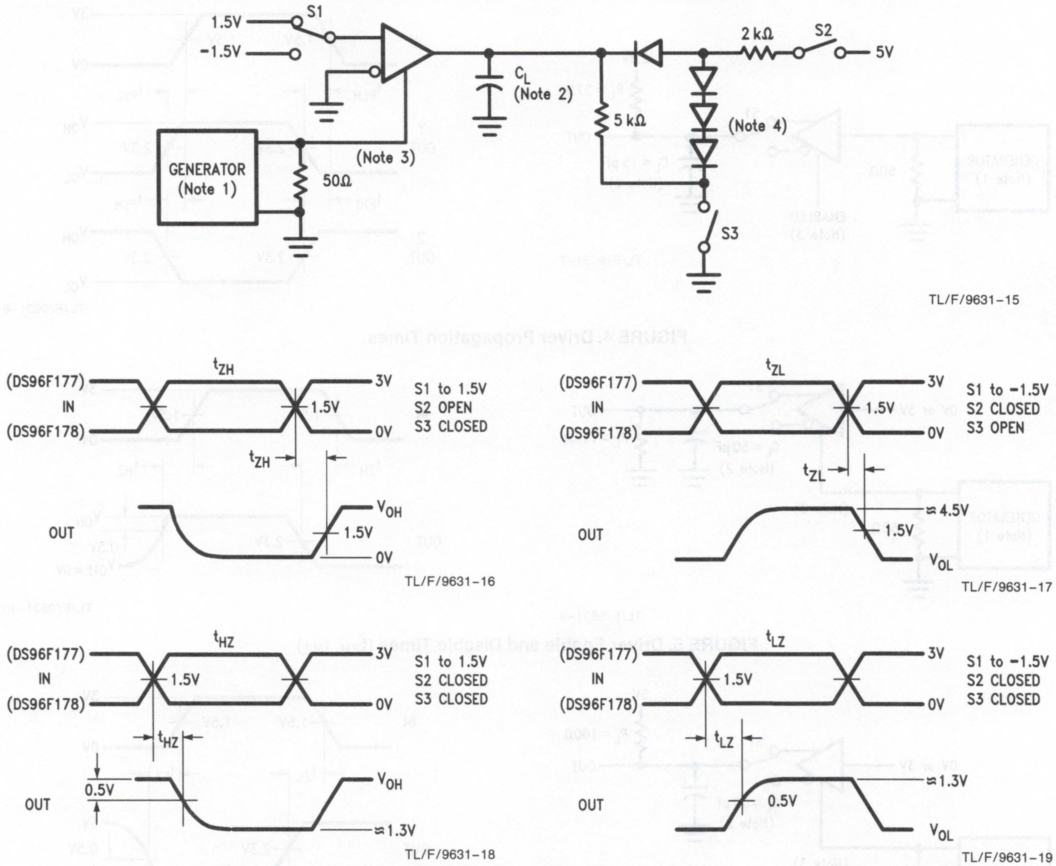

1.5V
−1.5V
S1
GENERATOR (Note 1)
50Ω
(Note 3)
C_L (Note 2)
5 kΩ
2 kΩ
S2
5V
(Note 4)
S3
TL/F/9631-15
t_ZH
(DS96F177) IN (DS96F178)
3V
1.5V
0V
S1 to 1.5V
S2 OPEN
S3 CLOSED
OUT
V_OH
TL/F/9631-16
t_ZL
S1 to −1.5V
S2 CLOSED
S3 OPEN
≈4.5V
V_OL
TL/F/9631-17
t_HZ
S1 to 1.5V
S2 CLOSED
S3 CLOSED
0.5V
≈1.3V
TL/F/9631-18
t_LZ
S1 to −1.5V
S2 CLOSED
S3 CLOSED
TL/F/9631-19

FIGURE 8. Receiver Enable and Disable Times

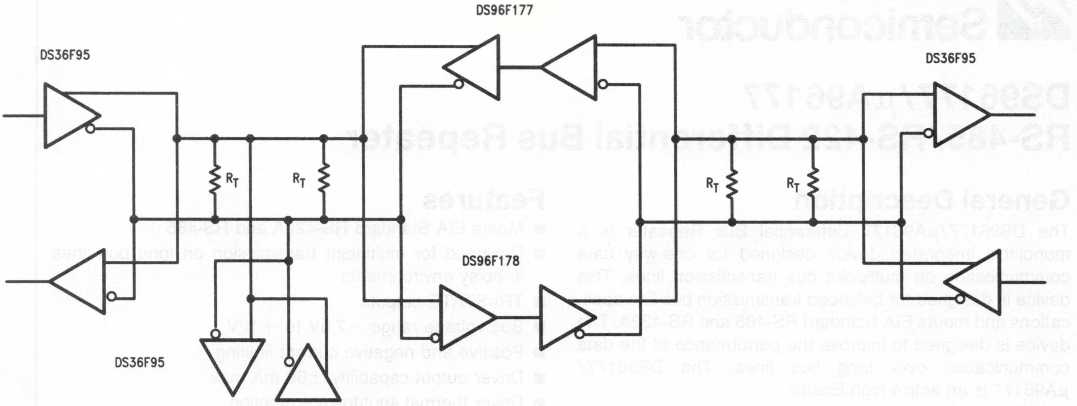
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96LF178 Enable is active low, DS96LF177 Enable is active high.

Note 4: All diodes are 1N916 or equivalent.

Typical Application


DS96F177
DS36F95
DS36F95
DS96F178
DS36F95
R_T
R_T
R_T
R_T

TL/F/9631-20

Notes:

The line length should be terminated at both ends in its characteristic impedance.

Stub lengths off the main line should be kept as short as possible.

FIGURE 9

National Semiconductor

DS96177/μA96177
RS-485/RS-422 Differential Bus Repeater

General Description

The DS96177/μA96177 Differential Bus Repeater is a monolithic integrated device designed for one-way data communication on multipoint bus transmission lines. This device is designed for balanced transmission bus line applications and meets EIA Standard RS-485 and RS-422A. The device is designed to improve the performance of the data communication over long bus lines. The DS96177/μA96177 is an active high Enable.

The DS96177/μA96177 features positive and negative current limiting and TRI-STATE® outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

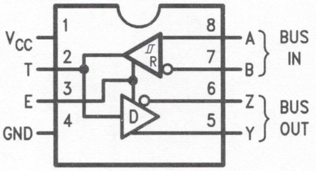
The DS96177/μA96177 is designed for optimum performance when used on transmission buses employing the DS96172/μA96172 and DS96174/μA96174 differential line drivers, DS96173/μA96173 and DS96175/μA96175 differential line receivers, or DS96176/μA96176 differential bus transceivers.

Features

- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission on long bus lines in noisy environments
- TRI-STATE outputs
- Bus voltage range −7.0V to +12V
- Positive and negative current limiting
- Driver output capability ±60 mA max
- Driver thermal shutdown protection
- Receiver input high impedance
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead Dual-In-Line Package



TL/F/9644-1

Top View

Order Number DS96177J, μA96177RC
See NS Package Number J08A*
Order Number DS96177N, μA96177TC
See NS Package Number N08E

Function Table

Differential Inputs	Enable	Outputs		
A–B	**E**	**T**	**Y**	**Z**
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

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*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP (Soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
Supply Voltage	7.0V
Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	µA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 100\Omega$, *Figure 2*	2.0	2.25		V
		$R_L = 54\Omega$, *Figure 1*	1.5	2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω, *Figure 1*			±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)				±0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0V$, $V_O = -7.0V$ to $+12V$			±100	µA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0V$ to $+12V$		±50	±200	µA
I_{IH}	Input Current HIGH	$V_I = 2.7V$			20	µA
I_{IL}	Input Current LOW	$V_I = 0.5V$			−100	µA
I_{OS}	Short Circuit Output Current (Note 9)	$V_O = -7.0V$			−250	mA
		$V_O = 0V$			−150	
		$V_O = V_{CC}$			150	
		$V_O = 12V$			250	
I_{CC}	Supply Current	No Load, Outputs Enabled			35	mA
		No Load, Outputs Disabled			40	

RECEIVER SECTION

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V$, $I_O = -0.4$ mA			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0$ mA	−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$		50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA			−1.5	V

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 3*		2.7			V
V_{OL}	Low Level Output Voltage	V_{ID} = −200 mV, *Figure 3*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V				−360	μA
		V_O = 2.4V				20	
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance			12	15		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Drive Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 6*		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 7*		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 7*		29	35	ns

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96177/μA96177. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD}, V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

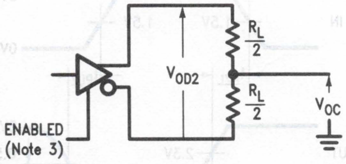
Note 6: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standards RS-485 for exact conditions.

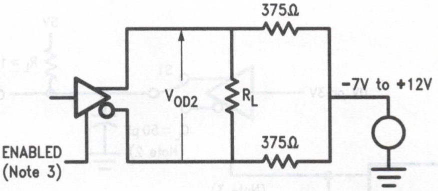
Note 9: Only one output at a time should be shorted.

Parameter Measurement Information


V_{OD2}
$\frac{R_L}{2}$
$\frac{R_L}{2}$
V_{OC}
ENABLED
(Note 3)

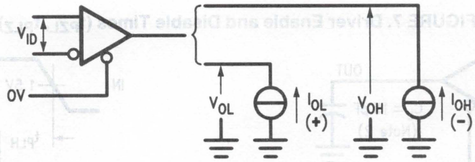
TL/F/9644-2

FIGURE 1. Driver V_{OD2} and V_{OC}


375Ω
V_{OD2}
R_L
375Ω
−7V to +12V
ENABLED
(Note 3)

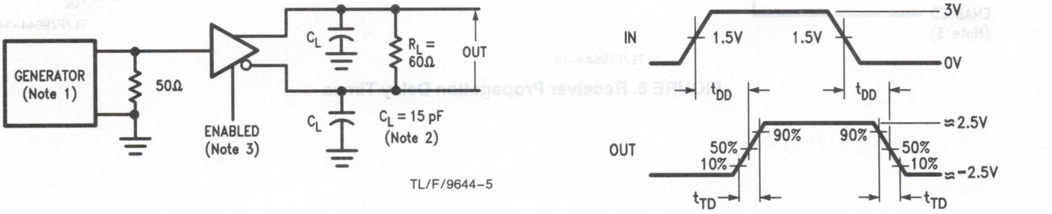
TL/F/9644-4

FIGURE 2. Driver V_{OD2} with Varying Common Mode Voltage


V_{ID}
0V
V_{OL}
I_{OL} (+)
V_{OH}
I_{OH} (−)

TL/F/9644-3

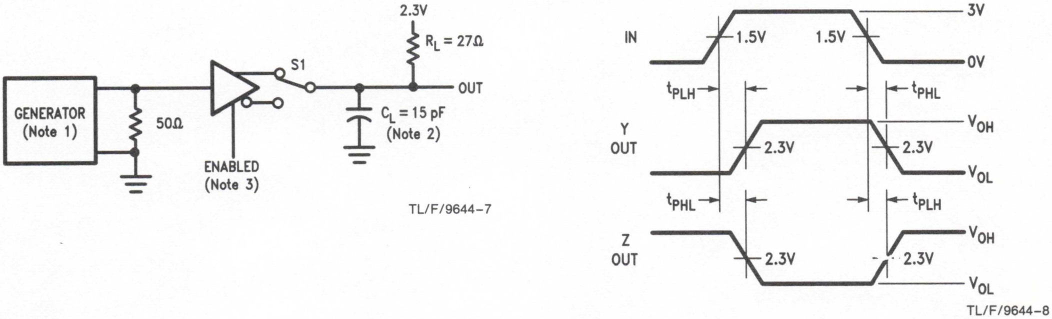
FIGURE 3. Receiver V_{OH} and V_{OL}


GENERATOR (Note 1)
50Ω
ENABLED (Note 3)
C_L
C_L
R_L = 60Ω
OUT
C_L = 15 pF (Note 2)
IN
1.5V
1.5V
3V
0V
t_{DD}
t_{DD}
OUT
90%
90%
≈2.5V
50%
10%
50%
10%
≈−2.5V
t_{TD}
t_{TD}

TL/F/9644-5

TL/F/9644-6

FIGURE 4. Driver Differential Output Delay and Transition Times

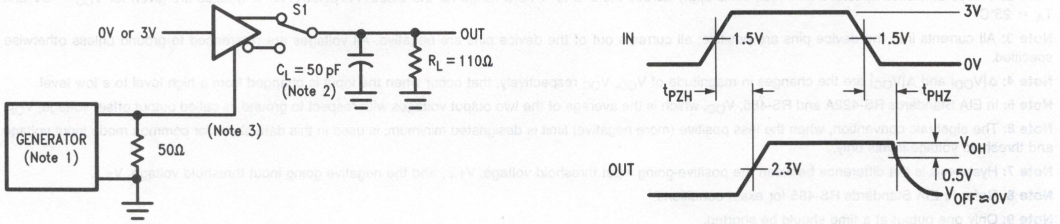

GENERATOR (Note 1)
50Ω
ENABLED (Note 3)
S1
2.3V
R_L = 27Ω
OUT
C_L = 15 pF (Note 2)
IN
1.5V
1.5V
3V
0V
t_{PLH}
t_{PHL}
Y OUT
2.3V
2.3V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Z OUT
2.3V
2.3V
V_{OH}
V_{OL}

TL/F/9644-7

TL/F/9644-8

FIGURE 5. Drive Propagation Times

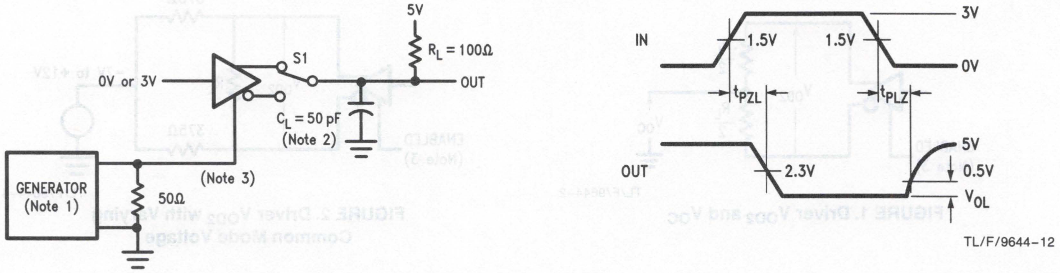
Parameter Measurement Information (Continued)


S1
0V or 3V
OUT
C_L = 50 pF
(Note 2)
R_L = 110Ω
GENERATOR
(Note 1)
50Ω
(Note 3)
3V
IN
1.5V
1.5V
0V
t_{PZH}
t_{PHZ}
V_{OH}
OUT
2.3V
0.5V
V_{OFF} ≈ 0V

TL/F/9644-9

TL/F/9644-10

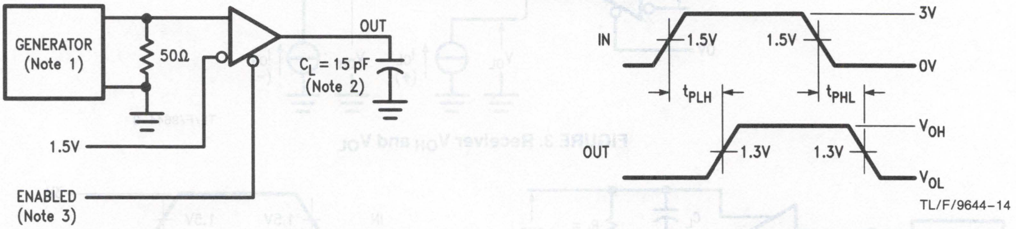
FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})


5V
R_L = 100Ω
S1
0V or 3V
OUT
C_L = 50 pF
(Note 2)
GENERATOR
(Note 1)
50Ω
(Note 3)
3V
IN
1.5V
1.5V
0V
t_{PZL}
t_{PLZ}
5V
OUT
2.3V
0.5V
V_{OL}

TL/F/9644-12

TL/F/9644-11

FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})


GENERATOR
(Note 1)
50Ω
OUT
C_L = 15 pF
(Note 2)
1.5V
ENABLED
(Note 3)
3V
IN
1.5V
1.5V
0V
t_{PLH}
t_{PHL}
V_{OH}
OUT
1.3V
1.3V
V_{OL}

TL/F/9644-14

TL/F/9644-13

FIGURE 8. Receiver Propagation Delay Times

Parameter Measurement Information (Continued)

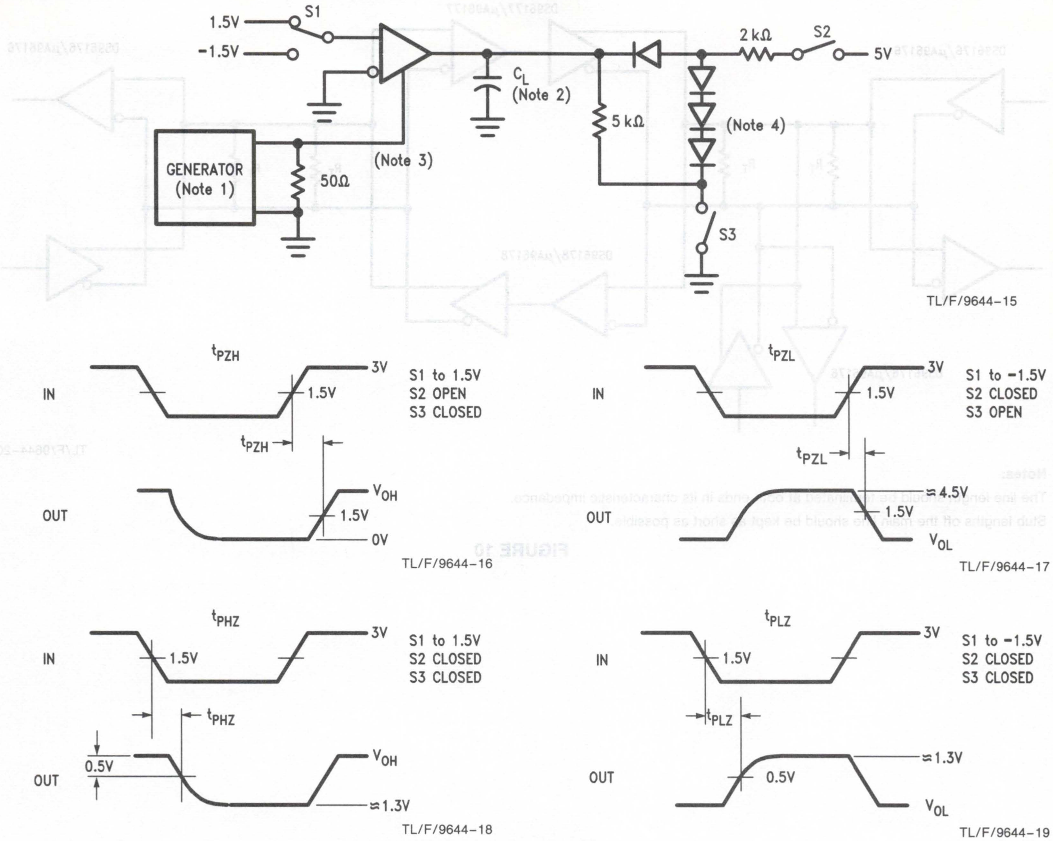

1.5V
-1.5V
S1
GENERATOR (Note 1)
50Ω
(Note 3)
C_L (Note 2)
5 kΩ
2 kΩ
S2
5V
(Note 4)
S3
TL/F/9644-15
t_{PZH}
IN
3V
1.5V
S1 to 1.5V
S2 OPEN
S3 CLOSED
t_{PZH}
OUT
V_{OH}
1.5V
0V
TL/F/9644-16
t_{PZL}
IN
3V
1.5V
S1 to -1.5V
S2 CLOSED
S3 OPEN
t_{PZL}
OUT
≈4.5V
1.5V
V_{OL}
TL/F/9644-17
t_{PHZ}
IN
3V
1.5V
S1 to 1.5V
S2 CLOSED
S3 CLOSED
t_{PHZ}
OUT
0.5V
V_{OH}
≈1.3V
TL/F/9644-18
t_{PLZ}
IN
3V
1.5V
S1 to -1.5V
S2 CLOSED
S3 CLOSED
t_{PLZ}
OUT
≈1.3V
0.5V
V_{OL}
TL/F/9644-19

FIGURE 9. Receiver Enable and Disable Times

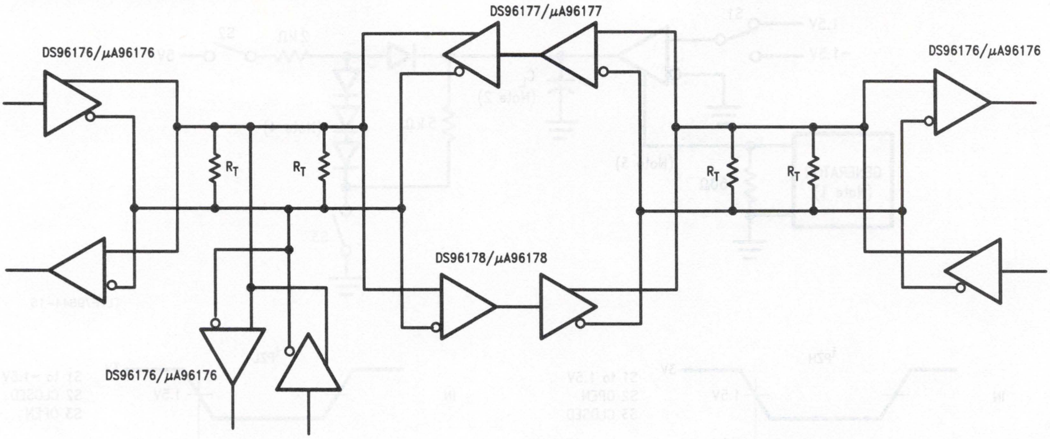
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96178/μA96178 Enable is active low, DS96177/μA96177 Enable is active high.

Note 4: All diodes are 1N916 or equivalent.

Typical Application


DS96176/μA96176
DS96177/μA96177
DS96176/μA96176
R_T
R_T
R_T
R_T
DS96178/μA96178
DS96176/μA96176

TL/F/9644-20

Notes:

The line length should be terminated at both ends in its characteristic impedance.

Stub lengths off the main line should be kept as short as possible.

FIGURE 10

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

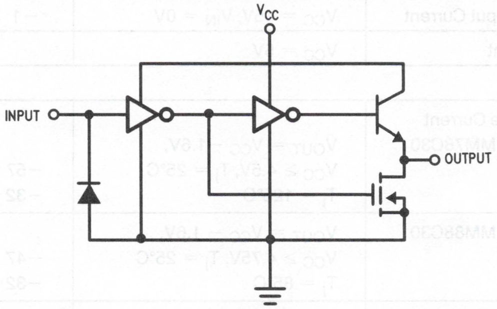
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low output ON resistance	20Ω (typ.)

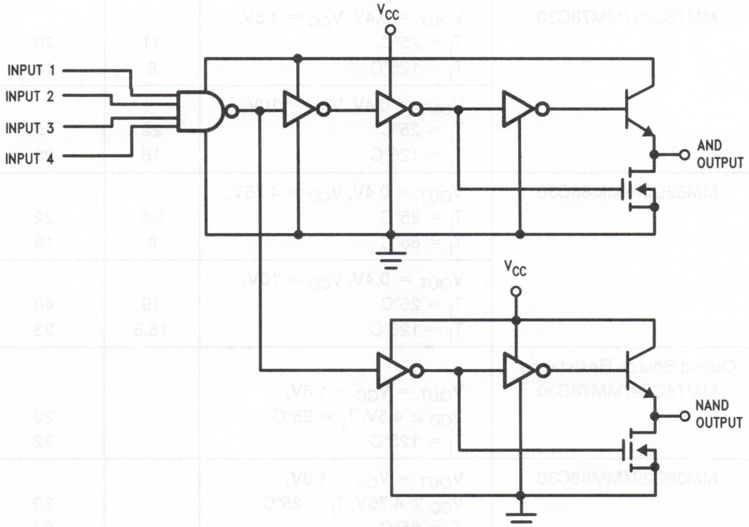
Logic Diagrams

1/4 MM78C29/MM88C29



TL/F/5908-1

1/2 MM78C30/MM88C30



TL/F/5908-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC} + 16V$
Operating Temperature Range	
MM78C29/MM78C30	$-55°C$ to $+125°C$
MM88C29/MM88C30	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$		0.05	100	mA
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.5V$, $T_j = 25°C$	−57	−80		mA
		$T_j = 125°C$	−32	−50		mA
	MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.75V$, $T_j = 25°C$	−47	−80		mA
		$T_j = 85°C$	−32	−60		mA
	MM78C29/MM88C29 MM78C30/MM88C30	$V_{OUT} = V_{CC} - 0.8V$ $V_{CC} \geq 4.5V$	−2	−20		mA
I_{SINK}	Output Sink Current MM78C29/MM78C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.5V$, $T_j = 25°C$	11	20		mA
		$T_j = 125°C$	8	14		mA
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$, $T_j = 25°C$	22	40		mA
		$T_j = 125°C$	16	28		mA
	MM88C29/MM88C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.75V$, $T_j = 25°C$	9.5	22		mA
		$T_j = 85°C$	8	18		mA
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$, $T_j = 25°C$	19	40		mA
		$T_j = 125°C$	15.5	33		mA
I_{SOURCE}	Output Source Resistance MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.5V$, $T_j = 25°C$		20	28	Ω
		$T_j = 125°C$		32	50	Ω
	MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.75V$, $T_j = 25°C$		20	34	Ω
		$T_j = 85°C$		27	50	Ω

DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (Continued)						
I_{SINK}	Output Sink Resistance MM78C29/MM78C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.50V$,				
		$T_j = 25°C$		20	36	Ω
		$T_j = 125°C$		28	50	Ω
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$,				
		$T_j = 25°C$		10	18	Ω
		$T_j = 125°C$		14	25	Ω
	MM88C29/MM88C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.75V$,				
		$T_j = 25°C$		18	41	Ω
		$T_j = 85°C$		22	50	Ω
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$,				
		$T_j = 25°C$		10	21	Ω
		$T_j = 85°C$		12	26	Ω
	Output Resistance Temperature Coefficient					
	Source			0.55		%/°C
	Sink			0.40		%/°C
θ_{JA}	Thermal Resistance MM78C29/MM78C30 (D-Package)			100		°C/W
	MM88C29/MM88C30 (N-Package)			150		°C/W

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50\ pF$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	(See *Figure 2*)				
	MM78C29/MM88C29	$V_{CC} = 5V$		80	200	ns
		$V_{CC} = 10V$		35	100	ns
	MM78C30/MM88C30	$V_{CC} = 5V$		110	350	ns
		$V_{CC} = 10V$		50	150	ns
t_{pd}	Differential Propagation Delay Time to Logical "1" or "0"	$R_L = 100\Omega$, $C_L = 5000\ pF$ (See *Figure 1*)				
	MM78C30/MM88C30	$V_{CC} = 5V$			400	ns
		$V_{CC} = 10V$			150	ns
C_{IN}	Input Capacitance					
	MM78C29/MM88C29	(Note 3)		5.0		pF
	MM78C30/MM88C30	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance					
	MM78C29/MM88C29	(Note 3)		150		pF
	MM78C30/MM88C30	(Note 3)		200		pF

*AC Parameters are guaranteed by DC correlated testing.

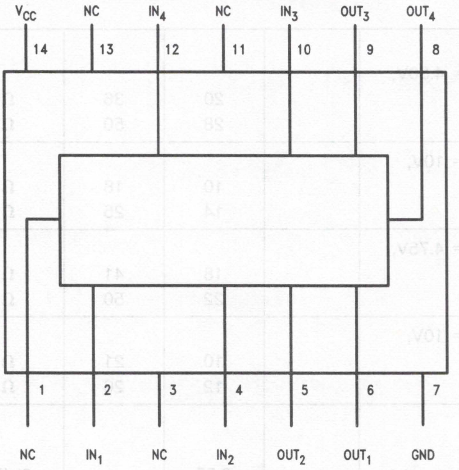
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Connection Diagrams

Dual-In-Line Package
MM78C29/MM88C29

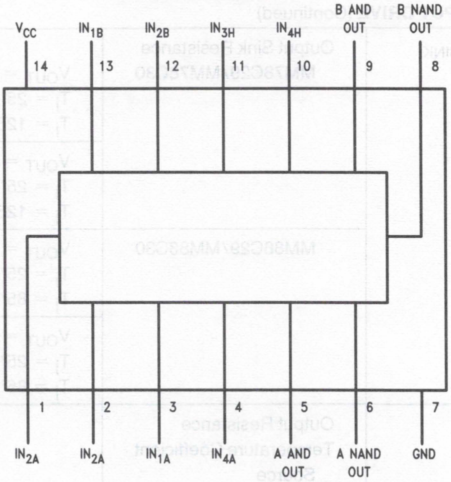

VCC
NC
IN4
NC
IN3
OUT3
OUT4
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
IN1
NC
IN2
OUT2
OUT1
GND

TL/F/5908-3

Top View

Order Number MM78C29* or MM88C29*

Dual-In-Line Package
MM78C30/MM88C30


VCC
IN1B
IN2B
IN3H
IN4H
B AND OUT
B NAND OUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
IN2A
IN2A
IN1A
IN4A
A AND OUT
A NAND OUT
GND

TL/F/5908-4

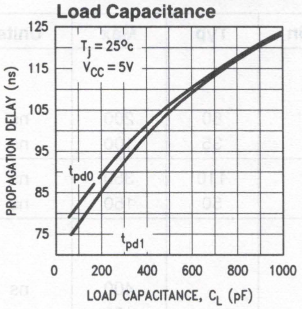
Top View

Order Number MM78C30J* or MM88C30J*

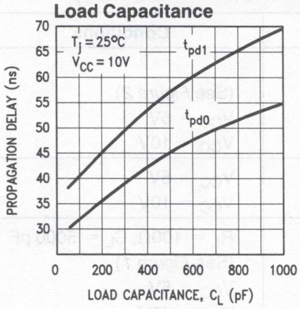
*Please look into Section 8, Appendix D for availability of various package types.

Typical Performance Characteristics

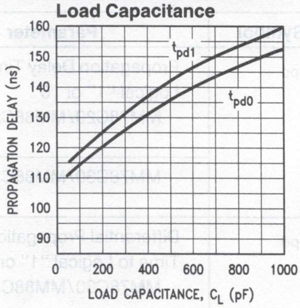
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



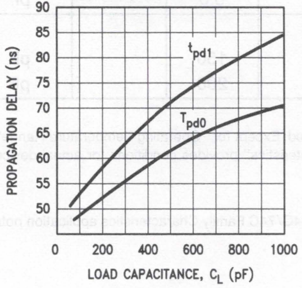
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



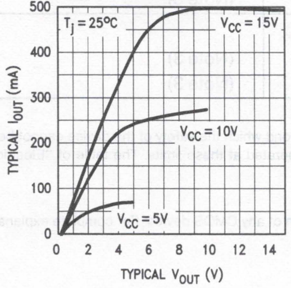
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



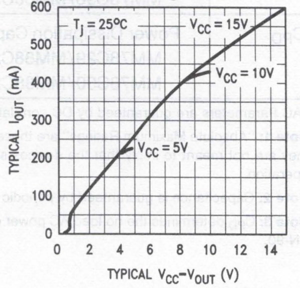
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



Typical Sink Current vs Output Voltage

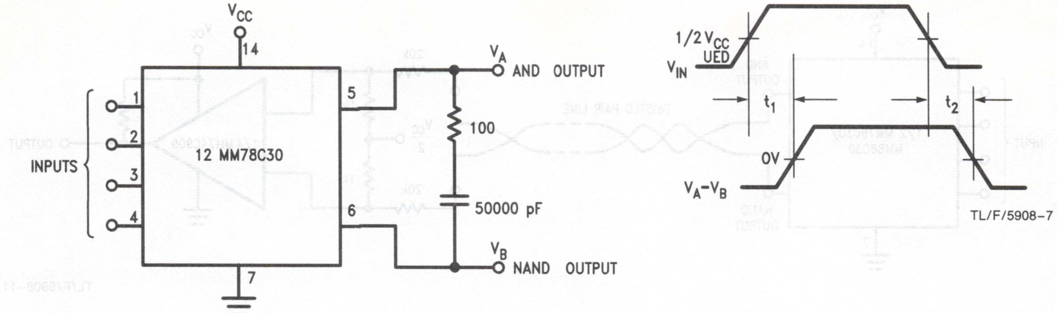


Typical Source Current vs Output Voltage



TL/F/5908-5

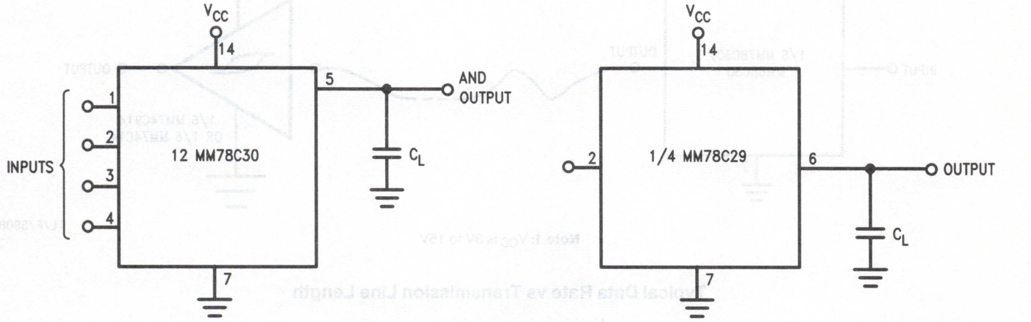
AC Test Circuits


VCC
14
1
2
3
4
INPUTS
12 MM78C30
5
6
7
VA
AND OUTPUT
100
50000 pF
VB
NAND OUTPUT
1/2 VCC
UED
VIN
t1
t2
OV
VA-VB

TL/F/5908-7

TL/F/5908-6

FIGURE 1


VCC
14
1
2
3
4
INPUTS
12 MM78C30
5
AND OUTPUT
CL
7
VCC
14
2
1/4 MM78C29
6
OUTPUT
CL
7

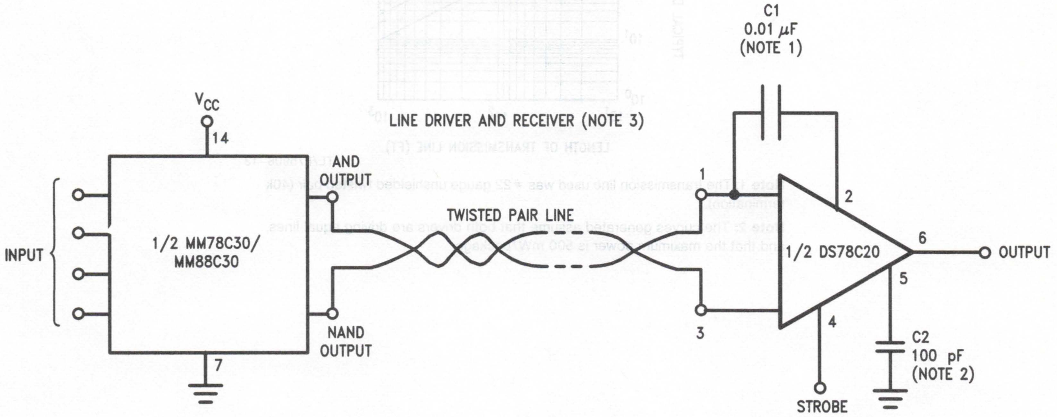
TL/F/5908-8

FIGURE 2

TL/F/5908-9

Typical Applications

Digital Data Transmission


C1
0.01 μF
(NOTE 1)
LINE DRIVER AND RECEIVER (NOTE 3)
VCC
14
INPUT
1/2 MM78C30/
MM88C30
AND OUTPUT
NAND OUTPUT
7
TWISTED PAIR LINE
1
2
3
1/2 DS78C20
4
5
6
OUTPUT
C2
100 pF
(NOTE 2)
STROBE

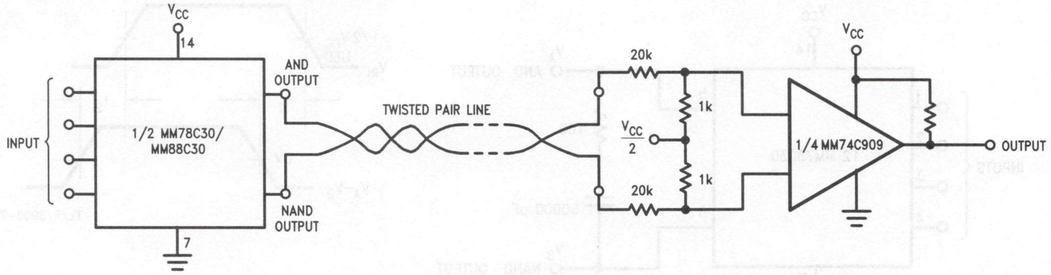
TL/F/5908-10

Note 1: Exact value depends on line length.

Note 2: Optional to control response time.

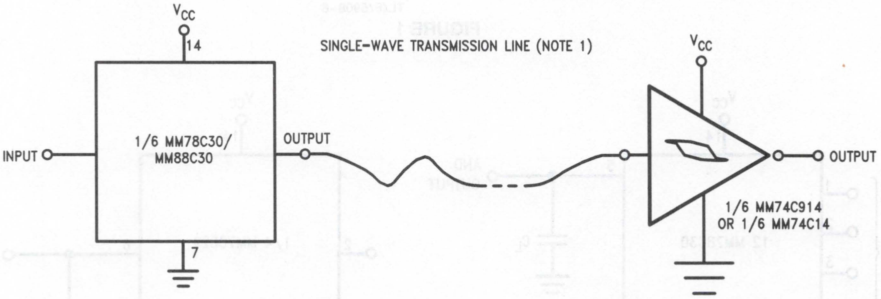
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820.

Typical Applications (Continued)


V$_{CC}$
14
AND OUTPUT
INPUT
1/2 MM78C30/ MM88C30
NAND OUTPUT
7
TWISTED PAIR LINE
20k
1k
V$_{CC}$/2
1k
20k
V$_{CC}$
1/4 MM74C909
OUTPUT

TL/F/5908-11

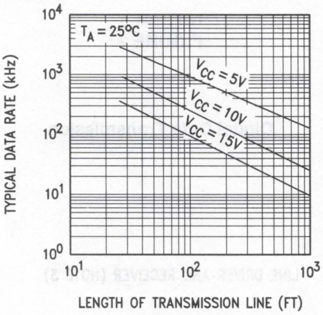
SINGLE-WAVE TRANSMISSION LINE (NOTE 1)


V$_{CC}$
14
INPUT
1/6 MM78C30/ MM88C30
OUTPUT
7
V$_{CC}$
OUTPUT
1/6 MM74C914 OR 1/6 MM74C14

TL/F/5908-12

Note 1: V$_{CC}$ is 3V to 15V

Typical Data Rate vs Transmission Line Length



TL/F/5908-13

Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

Integrated Circuits for Digital Data Transmission

National Semiconductor
Application Note 22

INTRODUCTION

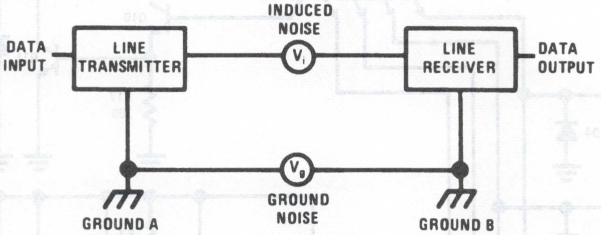
It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in *Figure 1a*, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

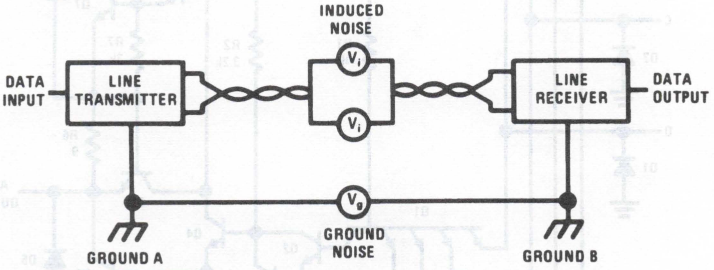
The differential transmission scheme diagrammed in *Figure 1b* solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.



a. Single-Ended System

TL/F/7188-1



TL/F/7188-2

b. Difference System

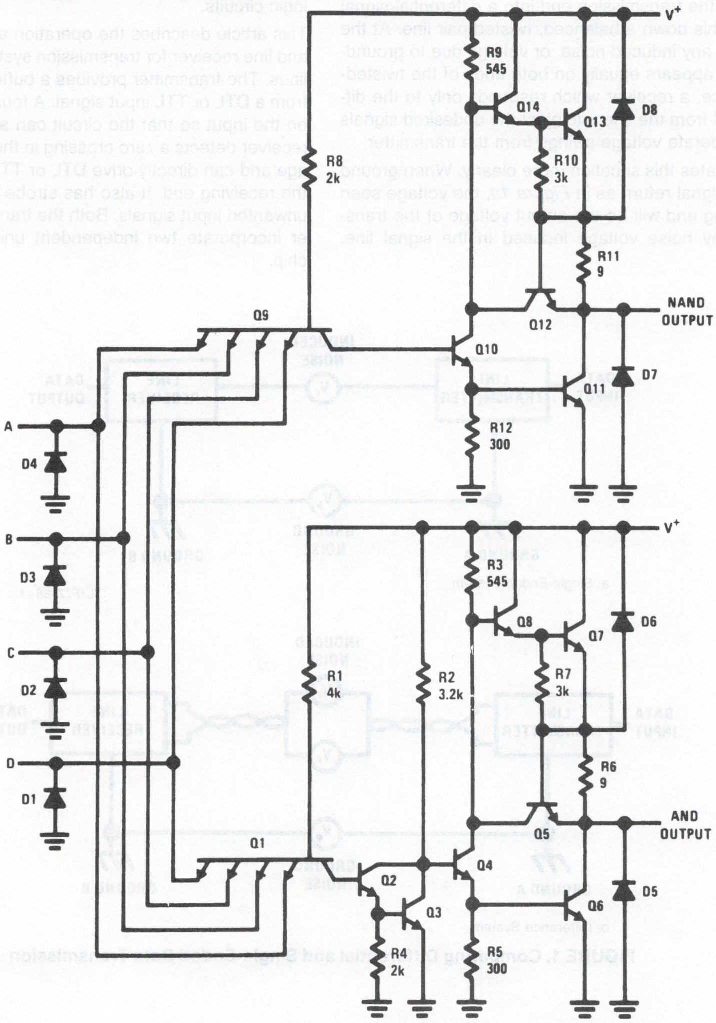
FIGURE 1. Comparing Differential and Single-Ended Data Transmission

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp sever voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

As can be seen from the upper half of *Figure 2*, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to



TL/F/7188–3

FIGURE 2. Schematic Diagram of the DS7830 Line Driver

the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

The lower half of the transmitter in *Figure 2* is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to *Figure 2*, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

The AND output is similarly protected by R6 and Q5, which limits the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the differential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

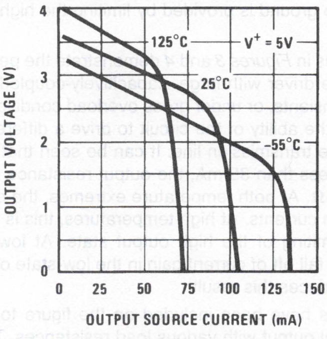


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FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. *Figure 3* shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of over-heating the integrated circuit.

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*J. Kalb, "Design Considerations for a TTL Gate", *National Semiconductor* TP-6, May, 1968.

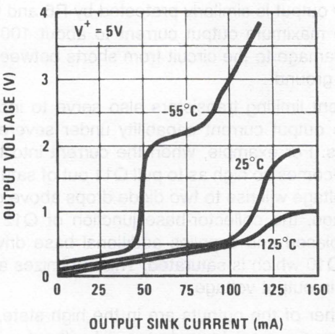

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FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is more pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in *Figures 3* and *4* demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under gross overload conditions. *Figure 5* shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the fall off of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω. This is more than adequate for practical, twisted-pair lines.

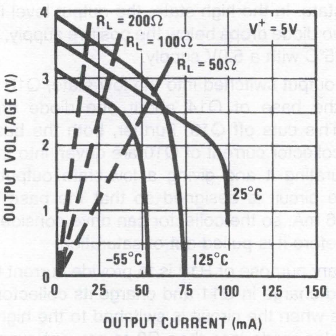

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FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

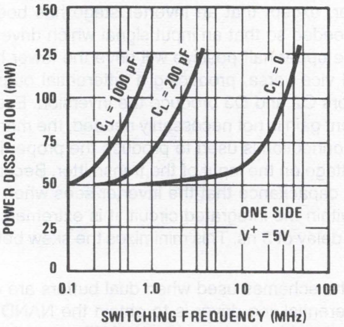

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FIGURE 6. Power Dissipation as a Function of Switching Frequency

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 kHz and 10 MHz. The figure shows that, with no capacitive loading, the power increases with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in *Figure 7*. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

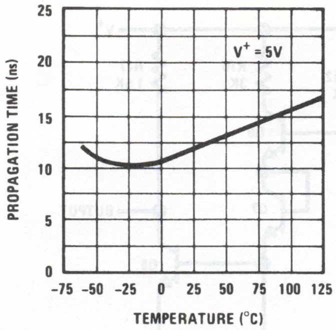

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FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in *Figure 8*.

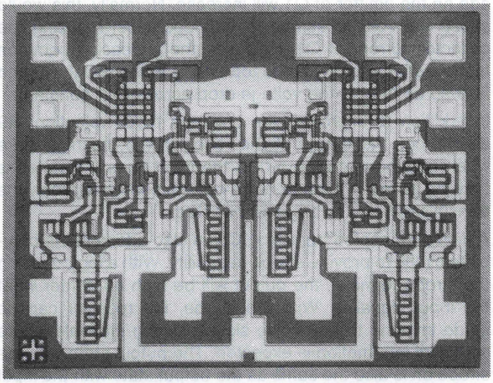

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FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receive must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handed easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced DC amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. this output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11} \qquad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \qquad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12 \qquad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}) \qquad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}$$

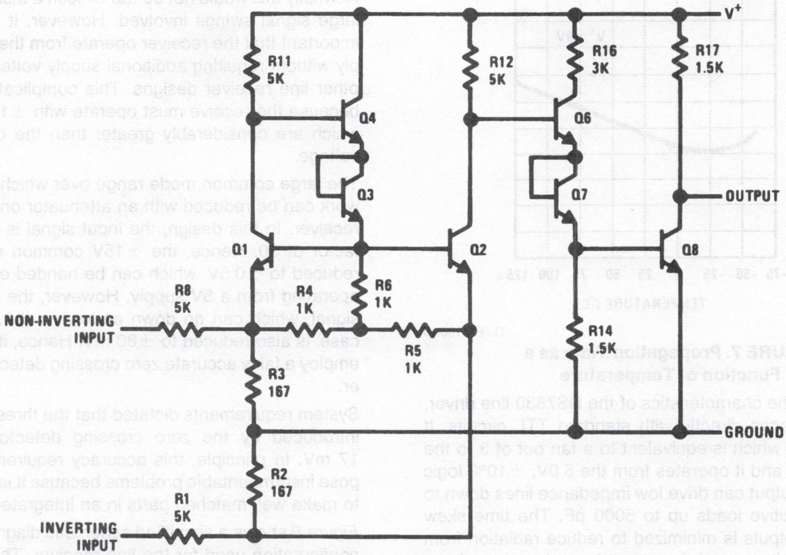

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FIGURE 9. Simplified Schematic of the Line Receiver

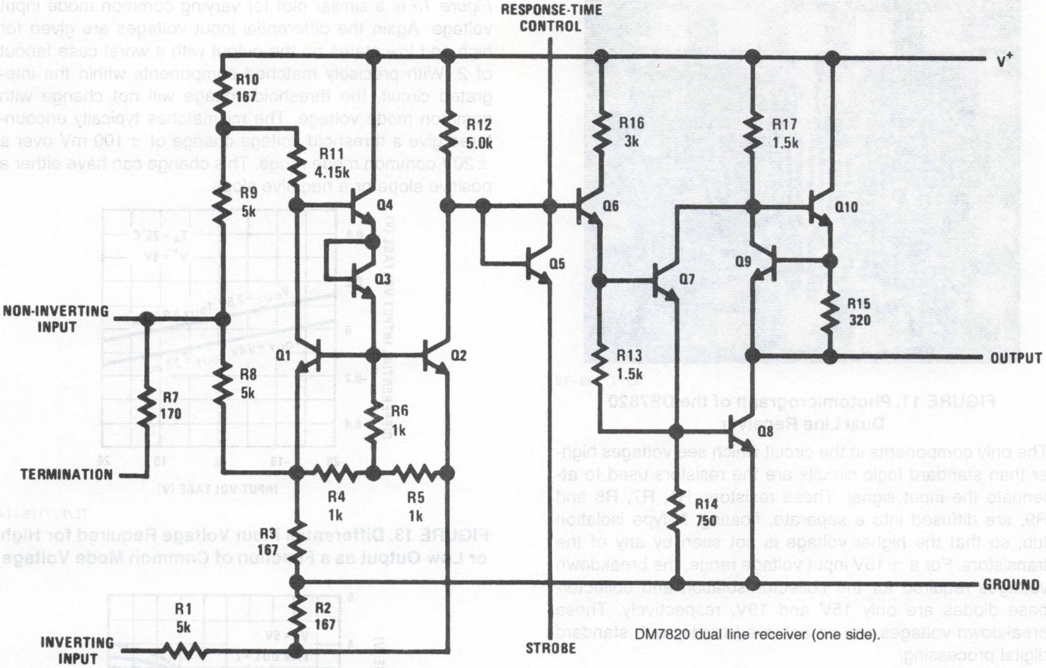
The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of this circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in *Figure 10*, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the output will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.



DM7820 dual line receiver (one side).

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FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5k, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in *Figure 11*.

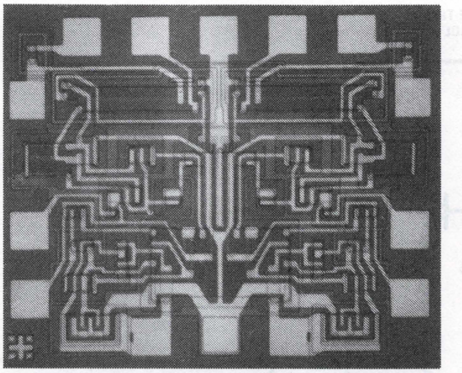

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FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in *Figures 12* through *18*. *Figure 12* illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

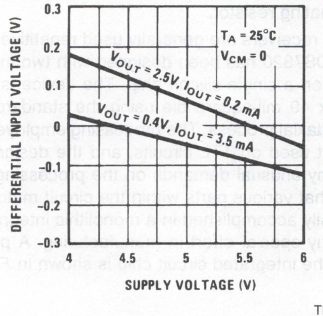

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FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

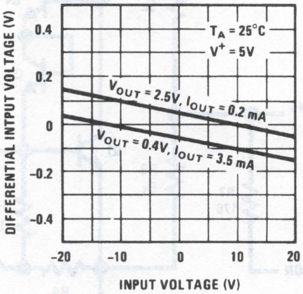

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FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

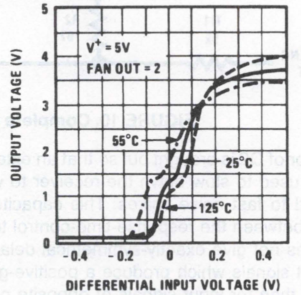

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FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in *Figure 14*. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at −55°C. However, the voltage available remains well above the 2.5V required by digital logic.

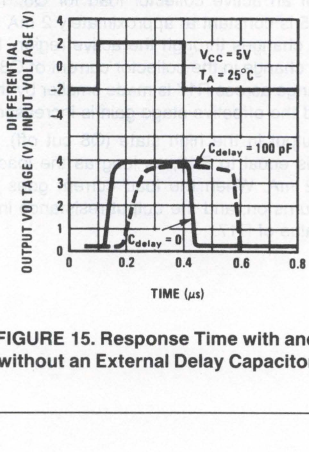

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FIGURE 15. Response Time with and without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in *Figure 16*. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a DC difference between the grounds of the transmitter and the receiver. It is important to note that *Figure 16* gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

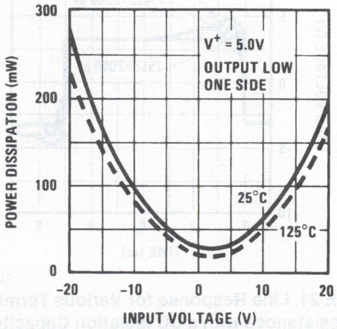

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FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

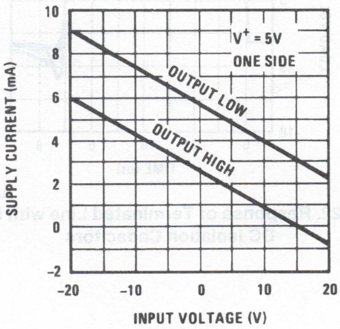

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FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in *Figure 18*. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

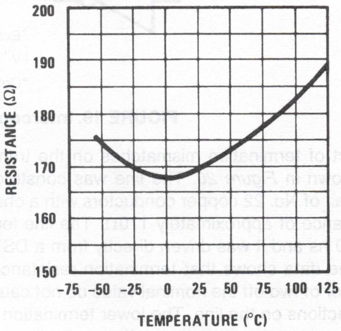

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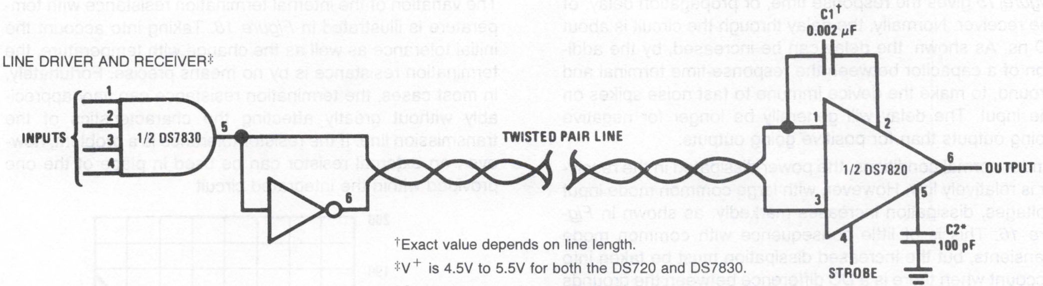
FIGURE 18. Variation of Termination Resistance with Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in *Figure 19*. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide DC isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.



†Exact value depends on line length.

‡V^+ is 4.5V to 5.5V for both the DS720 and DS7830.

*Optional to control response time.

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FIGURE 19. Interconnection of the Line Driver and Line Receiver

The effect of termination mismatches on the transmission line is shown in *Figure 20*. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

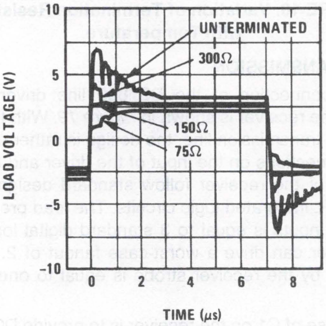

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FIGURE 20. Transmission Line Response with Various Termination Resistances

Figure 21 gives the line-transmission characteristics with various termination resistances when a DC isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient reponse is nearly the same as a DC terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the DC signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

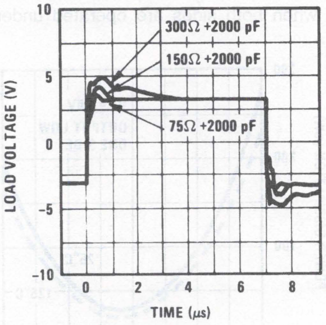

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FIGURE 21. Line Response for Various Termination Resistances with a DC Isolation Capacitor

The effect of different values of DC isolation capacitors is illustrated in *Figure 22*. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

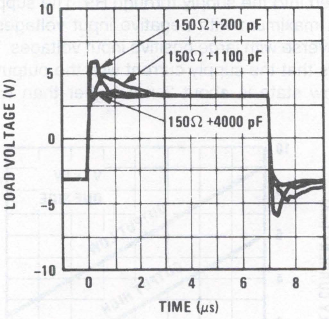

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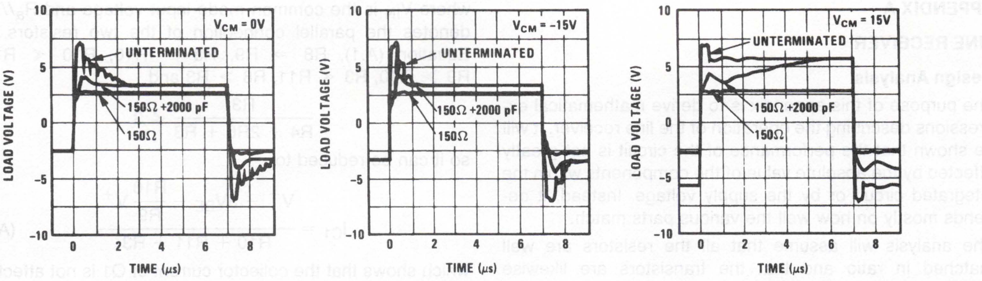
FIGURE 22. Response of Terminated Line with Different DC Isolation Capacitors



a. $V_{CM} = 0V$ b. $V_{CM} = -15V$ c. $V_{CM} = 15V$

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

In *Figure 23*, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal DC state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in *Figure 23b*. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a DC isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a DC coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in *Figure A-1*. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9//R10 + R11 + R3//R8} - \frac{\dfrac{R3}{R4 + 2R6 + R3} V_{BE1} - \dfrac{R3//R11}{R8 + R3//R1} V_{IN}}{R9//R10 + R11 + R3//R8} + \frac{(V_{IN} - V^+) \dfrac{R10//R11}{R9 + R10//R11}}{R9//R10 + R11 + R3//R8} \quad \text{(A.1)}$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A.1), $R8 = R9$, $R3 = R10$, $R10 \ll R11$, $R9 \gg R10$, $R3 \ll R11$, $R8 \gg R3$ and

$$\frac{R3}{R4 + 2R6 + R3} \ll 3$$

so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \dfrac{R10}{R9} V^+}{R10 + R11 + R3} \quad \text{(A.2)}$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2}R12 \quad \text{(A.3)}$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A.3) becomes

$$V_{C2} = V^+ - \frac{R12\left(V^+ - 3V_{BE} - \dfrac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad \text{(A.4)}$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3)\frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \dfrac{R10}{R9} V^+} \quad \text{(A.5)}$$

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A.4),

$$V_{C2} = 2.83V_{BE} + 0.081V^+ \quad \text{(A.6)}$$

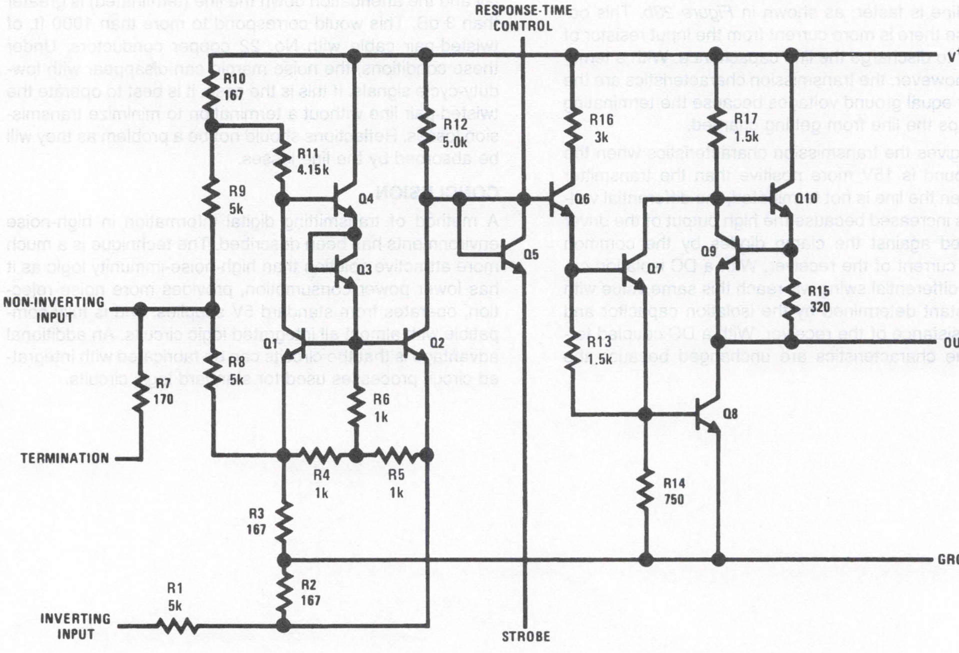


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FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

An equivalent circuit of the input stage is given in *Figure A-2.* Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\,R2}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \qquad (A.7)$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\,\alpha\,R2\,R12}{R1\,(0.9\,R2 + R_{E2}}\,\Delta V_{IN} \qquad (A.8)$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})} \qquad (A.9)$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}} \qquad (A.10)$$

where

$$I_{C2} = \frac{V^+ - 3V_{BE}}{R12} \qquad (A.11)$$

so

$$R_{E2} = \frac{kT\,R12}{q\,(V^+ - 3V_{BE})} \qquad (A.12)$$

Therefore, at 25°C where V_{VE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A.6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q}\log_e\frac{I_{C1}}{I_{C2}} \qquad (A.13)$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^+ - V_{OL} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}, \qquad (A.14)$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^+ - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} + I_{SINK} \qquad (A.15)$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^+ - V_{OH} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14}$$

$$+ \frac{V_{BE7}}{R13} - I_{SOURCE}, \qquad (A.16)$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A.15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} - I_{SOURCE} \qquad (A.17)$$

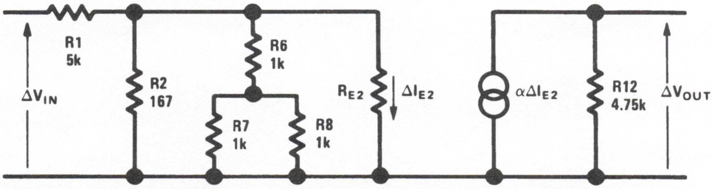

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FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

From (A.13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.18)$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{v1}} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.19)$$

where A_{v1} is the input stage gain. With a worst case fanout of 2, where $V_{OH} = 2.5V$, $V_{OL} = 0.4V$, $I_{SOURCE} = 40\ \mu A$ and $I_{SINK} = 3.2$ mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A.18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Characteristics

National Semiconductor
Application Note 108
Bill Fowler

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise sources which will require more noise immunity than required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solutions used vary considerably. Two widely used example methods of the solution are shown in *Figure 1.* The two methods illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

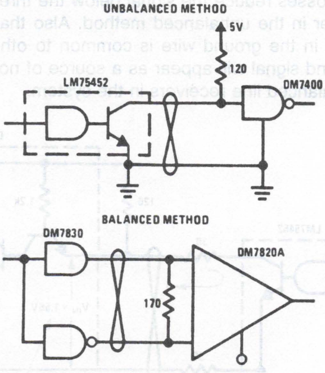

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FIGURE 1

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2.*

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3.* Some noise may be induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

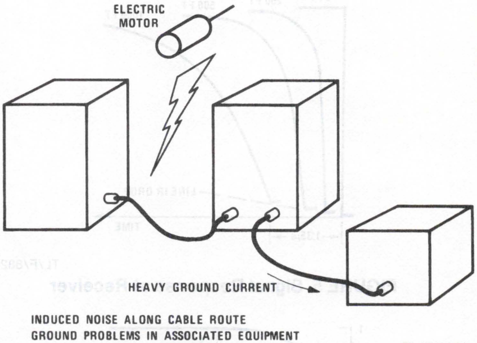
ELECTRIC MOTOR
HEAVY GROUND CURRENT
INDUCED NOISE ALONG CABLE ROUTE
GROUND PROBLEMS IN ASSOCIATED EQUIPMENT

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FIGURE 2. External Noise Sources

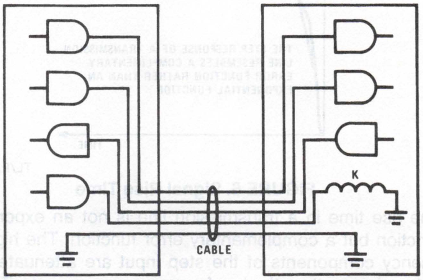

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FIGURE 3. Internal Noise Sources

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and the timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

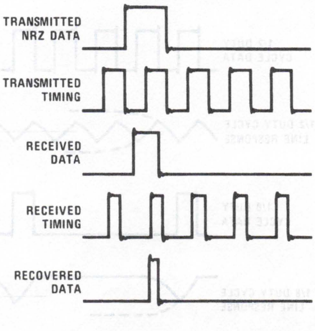

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FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

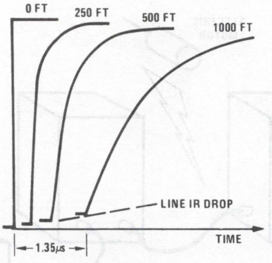

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FIGURE 5. Signal Response at Receiver

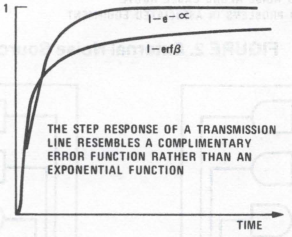

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FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final DC value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7.* The signal doesn't reach one logic level before the signal changes to another level. If the signal has a ½ (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is ⅛ as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

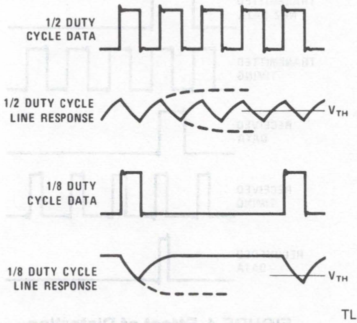
1/2 DUTY CYCLE DATA
1/2 DUTY CYCLE LINE RESPONSE
V_TH
1/8 DUTY CYCLE DATA
1/8 DUTY CYCLE LINE RESPONSE
V_TH

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FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8,* the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

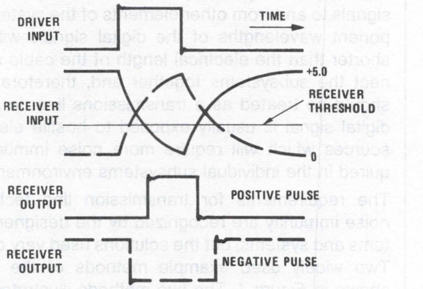
DRIVER INPUT
TIME
+5.0
RECEIVER THRESHOLD
RECEIVER INPUT
0
RECEIVER OUTPUT
POSITIVE PULSE
RECEIVER OUTPUT
NEGATIVE PULSE

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FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

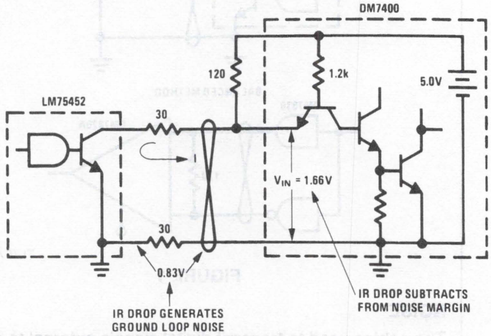
DM7400
120
1.2k
5.0V
LM75452
30
I
V_IN = 1.66V
30
0.83V
IR DROP GENERATES GROUND LOOP NOISE
IR DROP SUBTRACTS FROM NOISE MARGIN

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FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

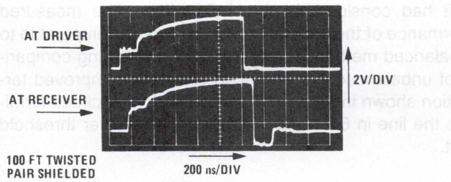

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FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left then is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final DC value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final DC value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

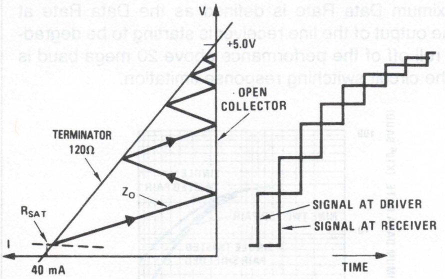
V
+5.0V
OPEN COLLECTOR
TERMINATOR 120Ω
Z_O
R_{SAT}
I
40 mA
SIGNAL AT DRIVER
SIGNAL AT RECEIVER
TIME

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FIGURE 11. Line Reflection Diagram of Rise Time

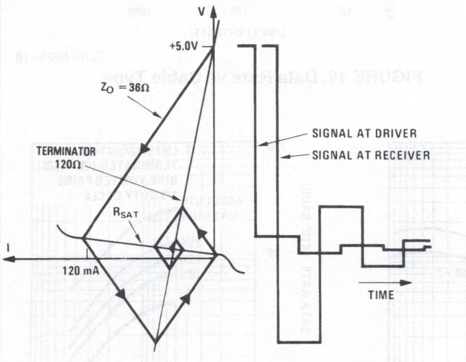
V
+5.0V
$Z_O = 38\Omega$
TERMINATOR 120Ω
R_{SAT}
I
120 mA
SIGNAL AT DRIVER
SIGNAL AT RECEIVER
TIME

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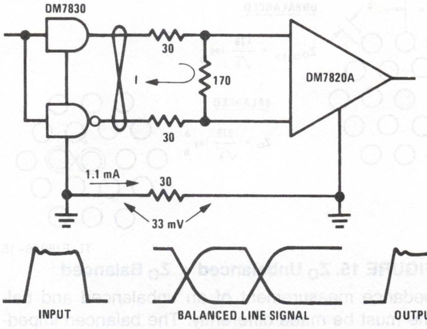
FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.


DM7830
30
I
170
DM7820A
30
1.1 mA
30
33 mV
INPUT
BALANCED LINE SIGNAL
OUTPUT

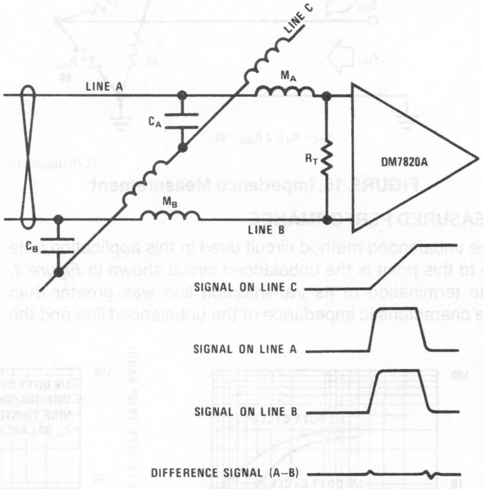
THE GROUND LOOP CURRENT IS MUCH LESS THAN SIGNAL CURRENT

TL/F/8826-13

FIGURE 13. Cross Talk of Signals

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on lines A and line B from lin C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

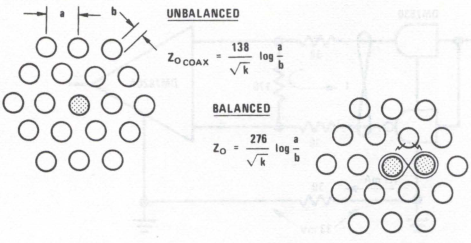
Likewise for the same reason, the differential signals on lines A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.


LINE C
LINE A
M_A
C_A
R_T
DM7820A
M_B
LINE B
C_B
SIGNAL ON LINE C
SIGNAL ON LINE A
SIGNAL ON LINE B
DIFFERENCE SIGNAL (A–B)

TL/F/8826-14

FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balanced method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.


a
b
UNBALANCED
$Z_{O\,COAX} = \frac{138}{\sqrt{k}} \log \frac{a}{b}$
BALANCED
$Z_O = \frac{276}{\sqrt{k}} \log \frac{a}{b}$

TL/F/8826-15

FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalanced and balanced line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

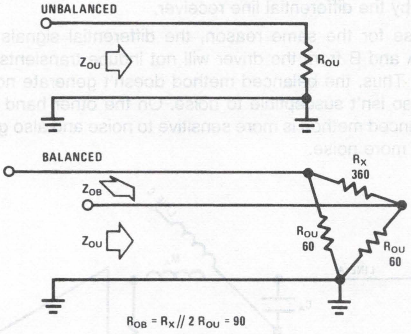


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FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1.* The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

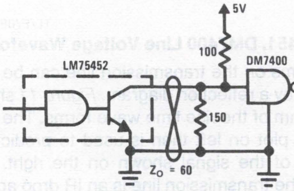

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FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18.* The graph shows the different performances of the DM7820A line receiver and the DM7830 line driver circuits with a worse case ⅛ Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

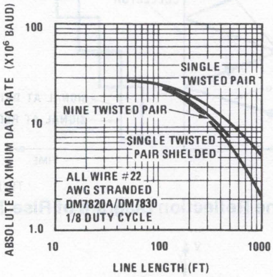

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FIGURE 18. Data Rate vs Cable Type

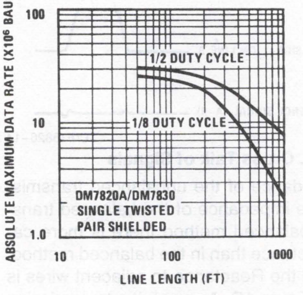

FIGURE 19. Data Rate vs Duty Cycle

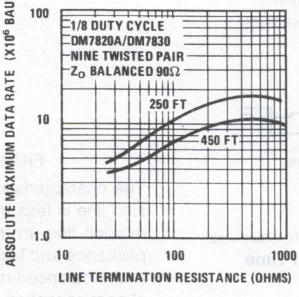

FIGURE 20. Data Rate vs Line Termination

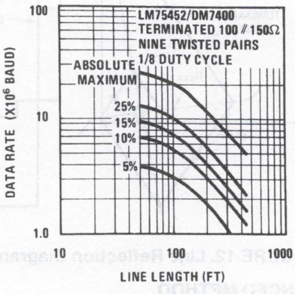

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FIGURE 21. Data Rate vs Distortion of LM75452, DM7400

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of ⅛ Duty Cycle is less than ½ Duty Cycle. The following performance curves will use ⅛ Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* show the Data Rate versus the Line Length for various percentages of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

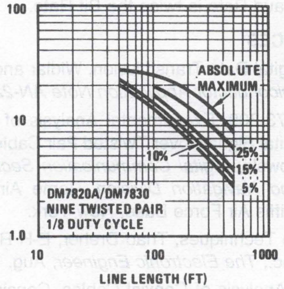

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FIGURE 22. Data Rate vs Distortion of DM7820A, DM7830

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23*. In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

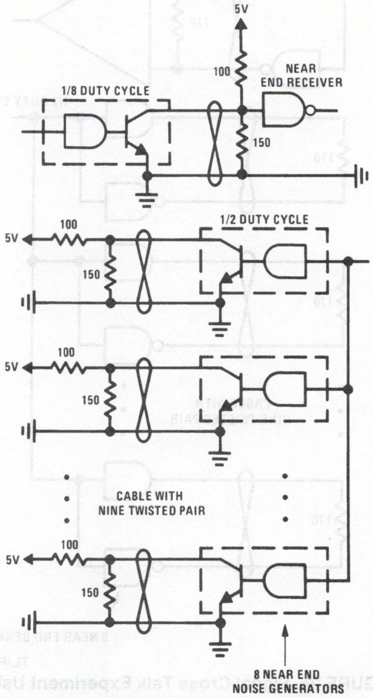

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FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

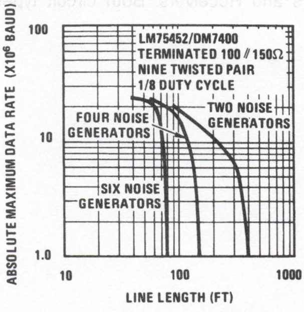

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FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

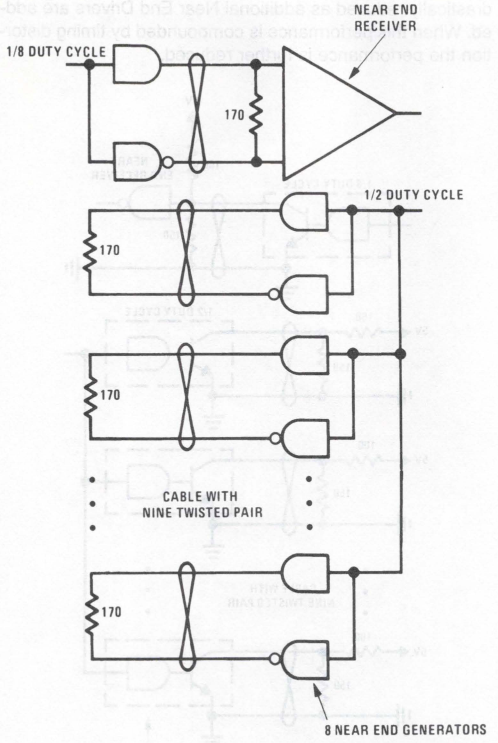

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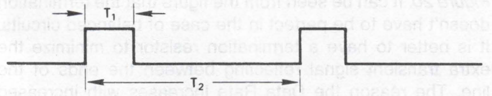
FIGURE 25. Signal Cross Talk Experiment Using DS7830, DS7820A

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitation. This application note shows that the balanced method is preferable for long lines in noisy electrical environments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates.

DEFINITION OF BAUD RATE



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$$\text{BIT RATE} = \frac{1}{\text{INTERVAL PER BIT}} = \frac{1}{T_2}$$

$$\text{BAUD RATE} = \frac{1}{\text{MINIMUM UNIT INTERVAL}} = \frac{1}{T_1}$$

The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

REFERENCES

IC's for Digital Data Transmission, Widlar and Kubinec, *National Semiconductor Application Note AN-22.*

RADC TR73-309, Experimental Analysis of the Transmission of Digital Signals over Twisted Pair Cable, Hendrickson and Evanowski, *Digital Communication Section Communications and Navigation Division,* Rome Air Development Center, Griffis Air Force Base, New York.

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Transient Analysis of Coaxial Cables, Considering Skin Effects, Wigingtom and Nahmaj, *Proceedings of the IRE,* Feb. 1957.

Relection and Crosstalk in Logic, Circuit Interconnection, John De Falco, Honeywell, Inc., *IEEE Spectrum,* July 1970.

Transmission Line Drivers and Receivers for EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and EIA standards RS-422 (balanced) and RS-423 (unbalanced). A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length
2) The modulation rate
3) The characteristic of the interconnection cable
4) The rise time of the signal

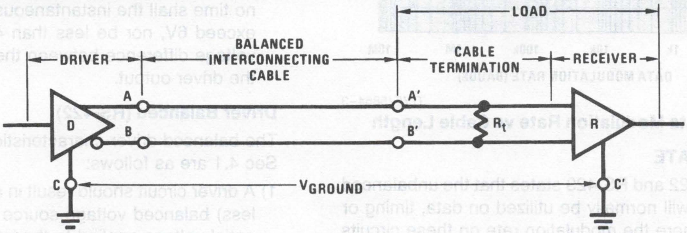
RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a* and *1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.

2) It is necessary to minimize interference with other signals, such as data versus clock.

3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*.



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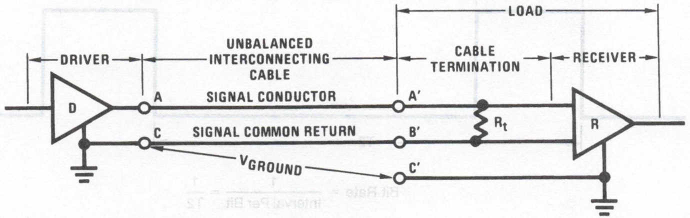
Legend:
R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A′, B′ = Load interface
C = Driver circuit ground
C′ = Load circuit ground

FIGURE 1a. RS-422 Balanced Digital Interface Circuit



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Legend:
R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A′, B′ = Load interface
C = Driver circuit ground
C′ = Load circuit ground

FIGURE 1b. RS-423 Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data modulation versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied modulation rate.

The maximum cable length between driver and load is a function of the baud rate. But it is influenced by:

1) A maximum common noise range of ±7 volts
    A) The amount of common-mode noise

       Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
    B) Ground potential differences between driver and load.
    C) Cable balance

       Differential noise caused by imbalance between the signal conductor and the common return (ground)
2) Cable termination

   At rates above 200 kilobaud or where the rise time is 4 times the one way propagation delay time of the cable (RS-422 Sec 7.1.2)
3) Tolerable signal distortion

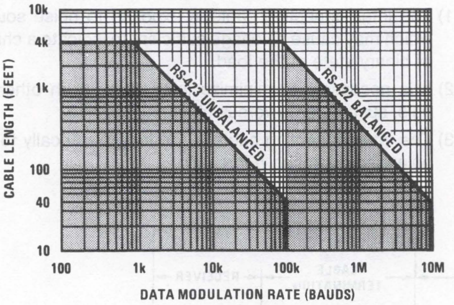

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FIGURE 2. Data Modulation Rate vs Cable Length

MODULATION RATE

Section 3 of RS-422 and RS-423 states that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the modulation rate on these circuits is below 100 kilobauds, and balanced voltage digital interface on circuits up to 10 megabauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates.

As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

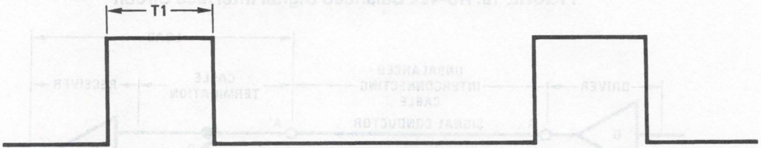
The unbalanced driver characteristics as specified by RS-423 Sec 4.1 are as follows:

1) A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.
2) With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the magnitude for either binary state.
3) During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed 6V, nor be less than 4V. V_{SS} is defined as the voltage difference between the 2 steady state values of the driver output.

Driver Balanced (RS-422)

The balanced driver characteristics as specified by RS-422 Sec 4.1 are as follows:

1) A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 6V.



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$$\text{Bit Rate} = \frac{1}{\text{Interval Per Bit}} = \frac{1}{T2}$$

$$\text{Baud Rate} = \frac{1}{\text{Minimum Unit Interval}} = \frac{1}{T1}$$

FIGURE 3a. Definition of Baud Rate

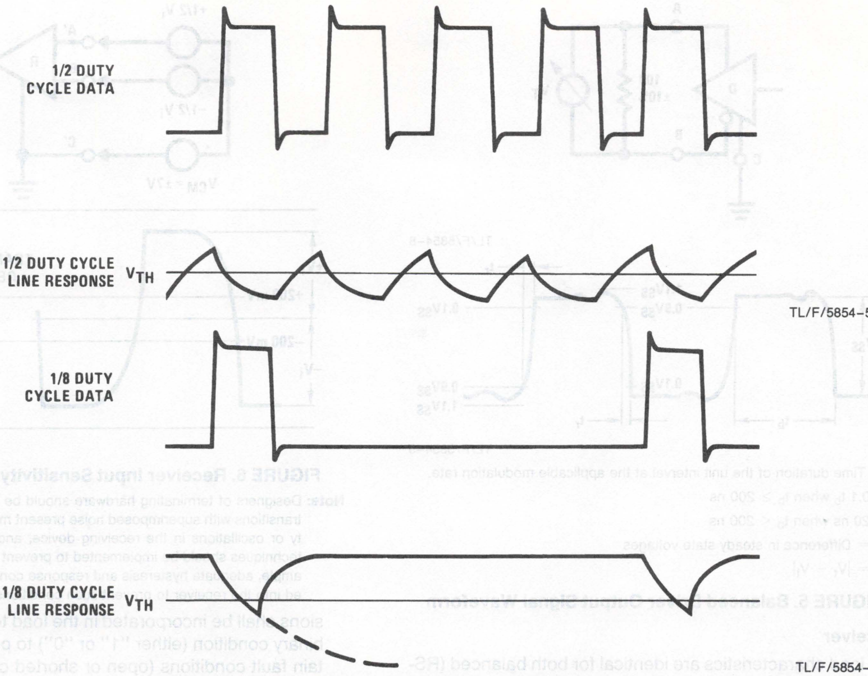

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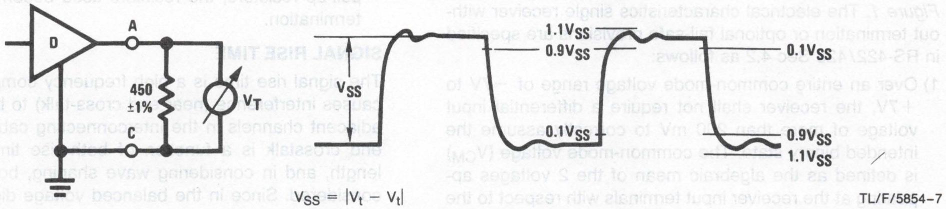
FIGURE 3b. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_{\bar{t}}|$

V_{SS} = Difference in steady state voltages

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FIGURE 4. Unbalanced Driver Output Signal Waveform

2) With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.

3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

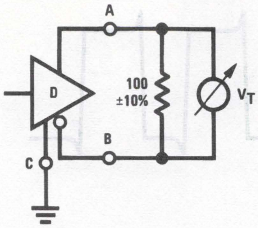
Interconnecting Cable

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) possessing the characteristics specified in RS-422 Sec 4.3 as follows:

1) Conductor size of the 2 wires shall be 24 AWG or larger with wire resistance not to exceed 30Ω per 1000 feet per conductor.

2) Mutual pair capacitance between 1 wire in the pair to the other shall not exceed 20 pF per foot.

3) Stray capacitance between 1 wire in the pair with all other wires connected to ground, shall not exceed 40 pF per foot.



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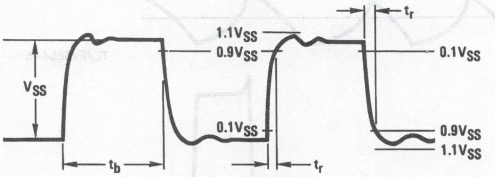

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t_b = Time duration of the unit interval at the applicable modulation rate.

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - V_{\bar{t}}|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The load characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. Each consists of a receiver and optional termination resistance as shown in *Figure 1*. The electrical characteristics single receiver without termination or optional fail-safe provisions are specified in RS-422/423 Sec 4.2 as follows:

1) Over an entire common-mode voltage range of −7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2) To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance greater than 90Ω for balanced, and 400Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.
5) Fail-safe operation per RS-423 Sec 4.2.5 states that other standards and specifications using the electrical characteristics of the unbalanced interface circuit may require that specific interchange leads be made fail-safe to certain fault conditions. Where fail-safe operation is required by such referencing standards and specifications, provisions shall be incorporated in the load to provide a steady binary condition (either "1" or "0") to protect against certain fault conditions (open or shorted cable).

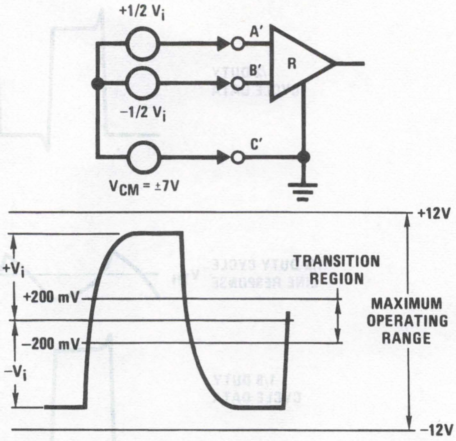

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FIGURE 6. Receiver Input Sensitivity Measurement

Note: Designers of terminating hardware should be aware that slow signal transitions with superimposed noise present may give rise to instability or oscillations in the receiving device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis and response control may be incorporated into the receiver to prevent such conditions.

The designer should be aware that in circuits employing pull-up resistors, the resistors used become part of the termination.

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 Sec 4.1.6, the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum modulation rate. Below 1 kilobaud the time to reach 90% V_{SS} shall be between 100 μs and 300 μs. If a driver is to operate over a range of modulation rates and employ a fixed amount of wave shaping which meets the specification for the maximum modulation rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

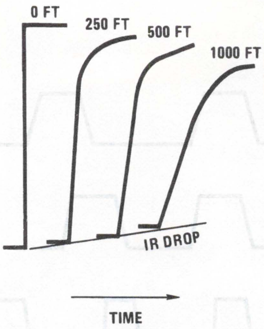

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FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

DS1691A, DS78LS120

The Driver

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of EIA standard RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping.

The DS3691 configured for RS-422 is connected $V_{CC} = 5V$ $V_{EE} = 0V$, and configured for RS-423 connected $V_{CC} = 5V$ $V_{EE} = -5V$. For applications outside RS-422 conditions and for greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1692/DS3692 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 12*, bottom waveform).

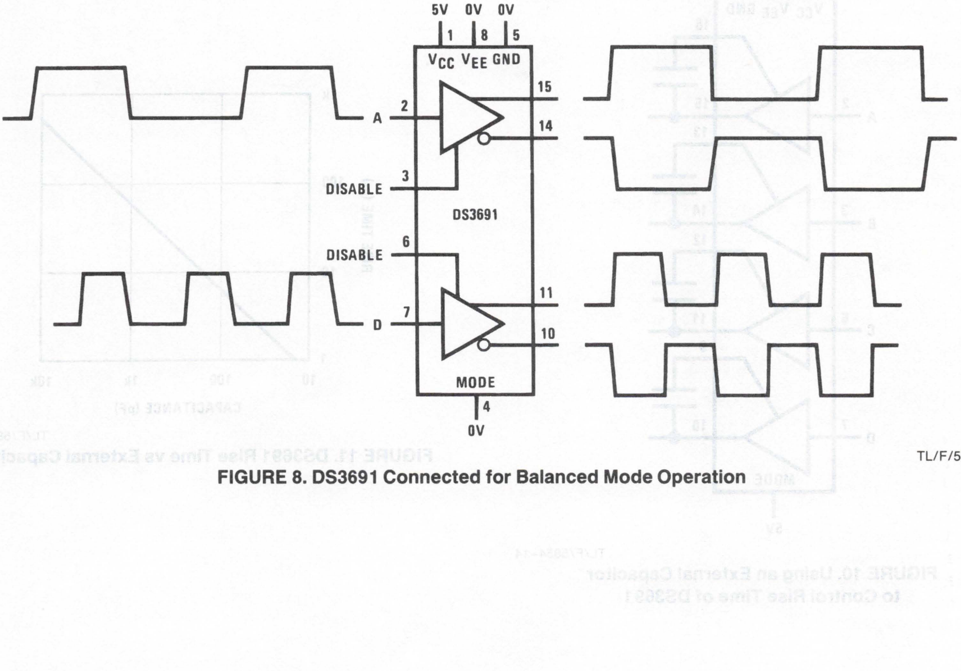

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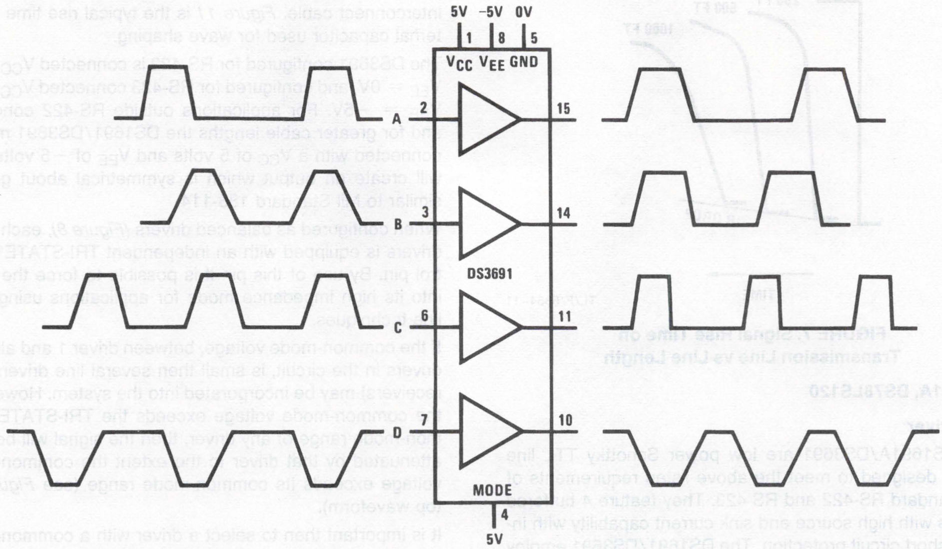
FIGURE 8. DS3691 Connected for Balanced Mode Operation


5V
−5V
0V
1
8
5
VCC
VEE
GND
A
2
15
B
3
14
DS3691
C
6
11
D
7
10
MODE
4
5V

TL/F/5854–13

FIGURE 9. DS3691 Connected for Unbalanced Mode Operation

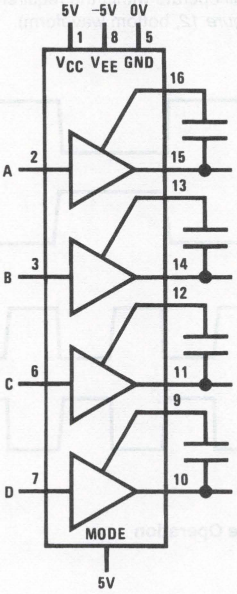

5V
−5V
0V
1
8
5
VCC
VEE
GND
16
A
2
15
13
B
3
14
12
C
6
11
9
D
7
10
MODE
5V

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FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

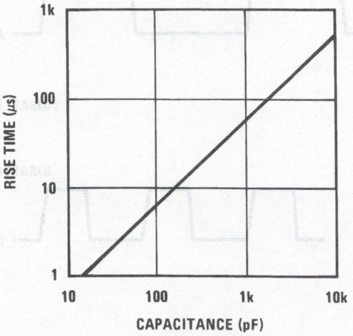

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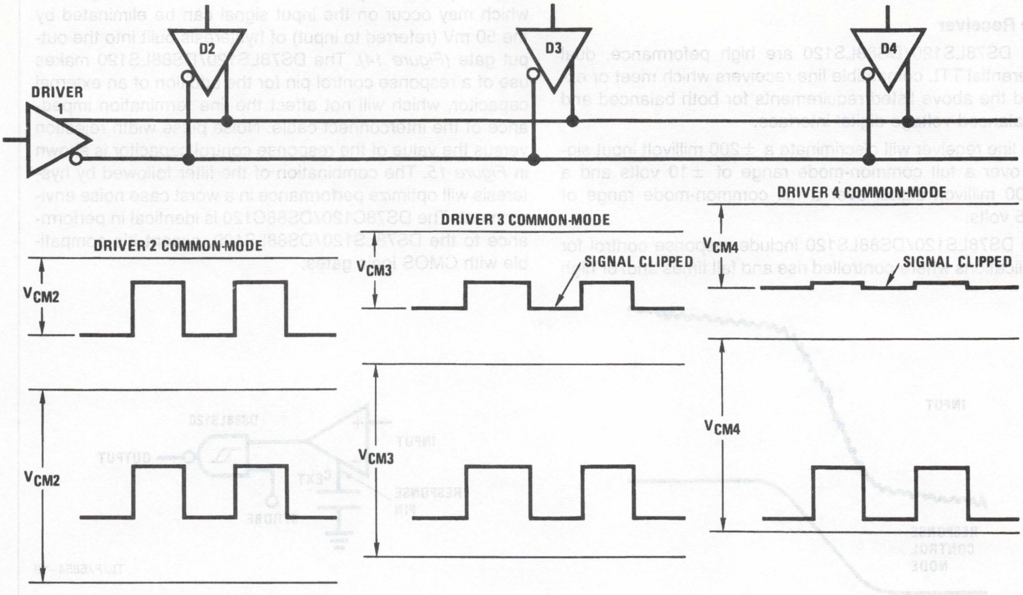
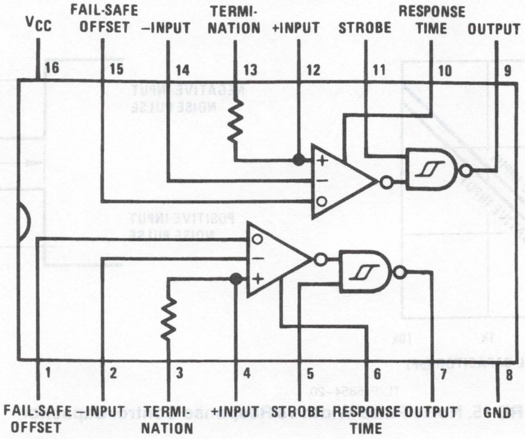
FIGURE 11. DS3691 Rise Time vs External Capacitor


DRIVER
D2
D3
D4
DRIVER 2 COMMON-MODE
DRIVER 3 COMMON-MODE
DRIVER 4 COMMON-MODE
V_{CM2}
V_{CM3}
V_{CM4}
SIGNAL CLIPPED
SIGNAL CLIPPED
V_{CM2}
V_{CM3}
V_{CM4}

TL/F/5854-16

FIGURE 12. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)


V_{CC}
FAIL-SAFE OFFSET
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
FAIL-SAFE OFFSET
−INPUT
TERMI-NATION
+INPUT
STROBE
RESPONSE TIME
OUTPUT
GND

TL/F/5854-17

Top View

FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

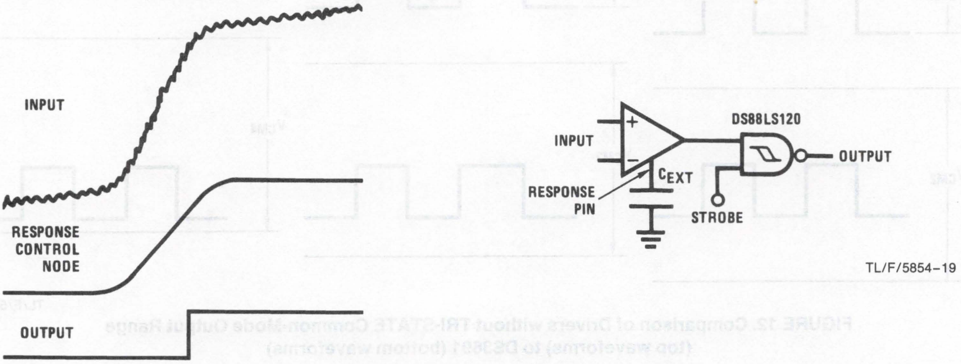
DS78LS120/DS88LS120

The Receiver

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

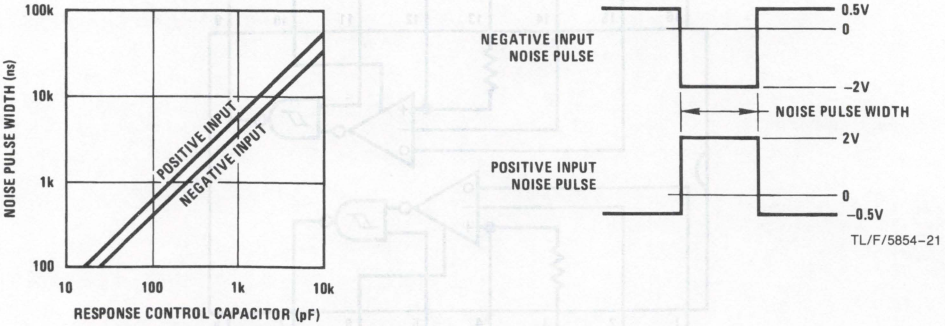
The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate *(Figure 14).* The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15.* The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.



TL/F/5854-18

TL/F/5854-19

FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis



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TL/F/5854-21

FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

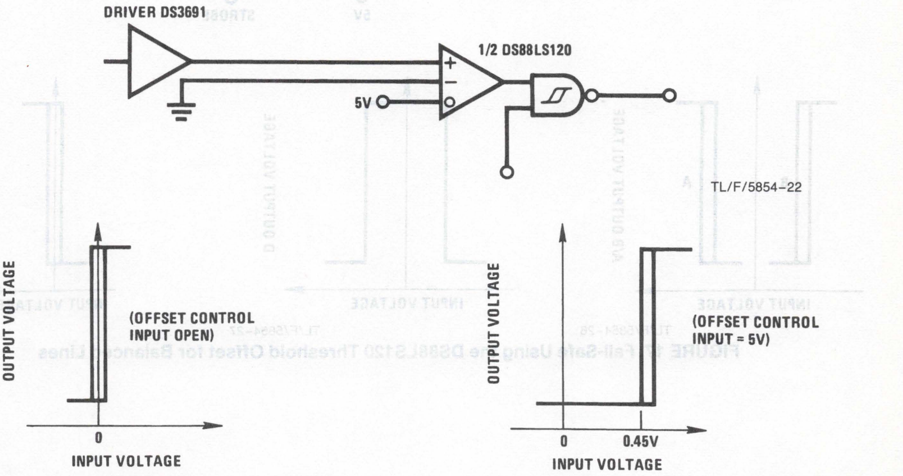
Communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a $V_{CC} = 5V$, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 16*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (see *Figure 17*).



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TL/F/5854–23

TL/F/5854–24

FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines

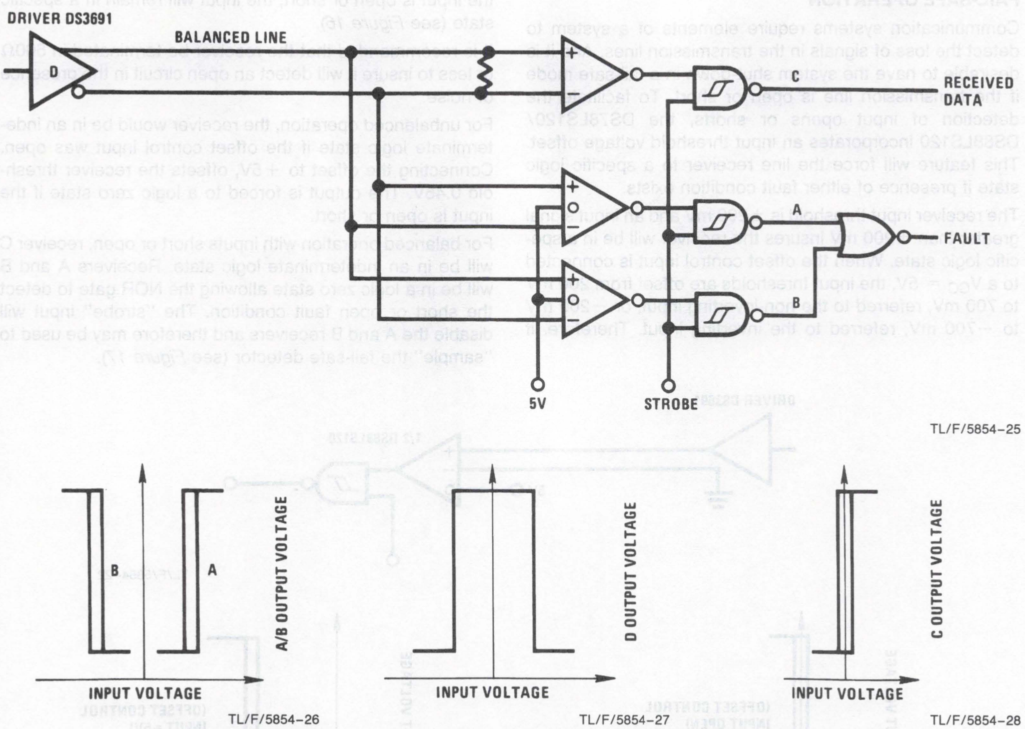
DRIVER DS3691
D
BALANCED LINE
+
−
C
RECEIVED DATA
+
o
−
A
FAULT
+
o
−
B
5V
STROBE
TL/F/5854-25
B
A
A/B OUTPUT VOLTAGE
INPUT VOLTAGE
TL/F/5854-26
D OUTPUT VOLTAGE
INPUT VOLTAGE
TL/F/5854-27
C OUTPUT VOLTAGE
INPUT VOLTAGE
TL/F/5854-28

FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Summary of Electrical Characteristics of Some Well Known Digital Interface Standards

National Semiconductor
Application Note 216
Don Tarver

FOREWORD

Not the least of the problems associated with the design or use of data processing equipment is the problem of providing for or, actually interconnecting the differing types and models of equipment to form specific processing systems.

The magnitude of the problem becomes apparent when one realizes that every aspect of the electrical, mechanical and architectural format must be specified. The most common of the basic decisions confronting the engineer include:

- Type of logic (negative or positive)
- Threshold levels
- Noise immunity
- Form of transmission
  - Balanced/unbalanced, terminated/unterminated
  - Unidirectional/bidirectional, simplex/multiplexed
- Type of transmission line
- Connector type and pin out
- Bit or byte oriented
- Baud rate

If each make and/or model of equipment presented a unique interface at its I/O ports, "interface" engineering would become a major expenditure associated with the use of data processing equipment.

Fortunately, this is not the case as various interested or cognizant groups have analyzed specific recurring interface areas and recommended "official" standards around which common I/O ports could be structured. Also, the I/O specifications of some equipment with widespread popularity such as the IBM 360/370 computer and DEC minicomputer have become "defacto" standards because of the desire to provide/use equipment which interconnect to them.

Compliance with either the "official" or "defacto" standards on the part of equipment manufacturers is voluntary. However, it is obvious that much can be gained and little lost by providing equipment that offers either the "official" or "defacto" standard I/O ports.

As can be imagined, the entire subject of interface in data processing systems is complicated and confusing, particularly to those not intimately involved in the day-to-day aspects of interface engineering or management. However, at the component level the questions simplify to knowing what standards apply and what circuits or components are available to meet the standards.

This application note summarizes the important electrical characteristics of the most commonly accepted interface standards and offers recommendations on how to use National Semiconductor integrated circuits to meet those standards.

1.0 INTRODUCTION

The interface standards covered in this application note are listed in Table I. The body of the text expands upon the scope and application of each listed standard and summarizes important electrical parameters.

Table II summarizes the National Semiconductor IC's applicable to each standard.

TABLE I. Common Line Driver/Receiver Interface Standards Summary

Interface Area	Application	Standard	Origin	Comments
Data Communications Equipment (DCE*) to Data Terminal Equipment (DTE)	U.S.A. Industrial	RS-232C RS-422 RS-423	EIA EIA EIA	Unbalanced, Short Lines Balanced, Long Lines Unbalanced, RS-232 Up-Grade
		RS-449	EIA	System Standard Covering Use of RS-422, RS-423
		RS-485	EIA	Balanced, Long Line Multipoint
	International	CCITT Vol. VIII V. 24 CCITT No. 97 X. 26 CCITT No. 97 X. 27	International Telephone and Telegraph Consultative Committee	Similar to RS-232 Similar to RS-423 Similar to RS-422
	U.S.A. Military	MIL-STD-188C MIL-STD-188-114 MIL-STD-1397 (NTDS–Slow)	D.O.D. D.O.D. Navy	Unbalanced, Short Lines Similar to RS-422, RS-423 42k bits/sec.
		MIL-STD-1397 (NTDS–Fast)	Navy	250k bits/sec
	U.S. Government, Non-Military	FED-STD-1020 FED-STD-1030	GSA GSA	Identical to RS-423 Identical to RS-422

TABLE I. Common Line Driver/Receiver Interface Standards Summary (Continued)

Interface Area	Application	Standard	Origin	Comments
Computer to Peripheral	IBM 360/370	System 360/370 Channel I/O	IBM	Unbalanced Bus
	DEC Mini-Computer	DEC Unibus®	DEC	Unbalanced Bus
Instrument to Computer	Nuclear Instrumentation	CAMAC (IEEE Std. 583-1975)	NIM (AEC)	DTL/TTL Logic Levels
	Laboratory Instrumentation	488	IEEE	Unbalanced Bus
Microprocessor to Interface Devices	Microprocessor Circuits	Microbus™	National Semiconductor	Short Line; 8-Bit Parallel, Digital Transmission
Facsimile Equipment to DTE	Facsimile Transmission	RS-357	EIA	Incorporates RS-232
Automatic Calling Equipment to DTE	Impulse Dialing and Multi-Tone Keying	RS-366	EIA	Incorporates RS-232
Numerically Controlled Equipment to DTE	Numerically Controlled Equipment	RS-408	EIA	Short Lines (<4 Ft.)

* Changed to "Data Circuit-Terminating Equipment"

TABLE II. Line Driver/Receiver Integrated Circuit Selection Guide for Digital Interface Standards

Standard Designation	Part Number			
	Line Driver		Line Receiver	
	0°C to +70°C	−55°C to +125°C	0° to +70°C	−55°C to +125°C
U.S. INDUSTRIAL STANDARDS				
RS-232C	DS1488 DS75150	Not Applicable Not Applicable	DS1489 (A) DS75154	Not Applicable Not Applicable
RS-357	See RS-232C			
RS-366	See RS-232C			
RS-408	DS75453 DS75454	DS55454 DS55454	DS7820A DS75115	DS7820A DS55115
RS-422	DS3691 DS26LS31C DS3487	DS1691A DS26LS31M DS3587	DS88LS120 DS26LS32C DS3486 DS26LS33C DS88C20 DS88C120	DS78LS120 DS26LS32M DS26LS33M DS78C20 DS78C120
RS-423	DS3691 DS3692	DS1691A DS1692	DS88LS120 DS88C20 DS88C120	DS78LS120 DS78C20 DS78C120
RS-449	See RS-422, RS-423			
RS-485 Transceivers	DS3695 DS3696 DS3697 DS3698 DS75176A		DS3695 DS3696 DS3697 DS3698 DS75176A	
IEEE 488	DS3666 DS75160A DS75161A DS75162A		DS3666 DS75160A DS75161A DS75162A	
CAMAC	See RS-232C, RS-422, RS-423 or IEEE 488			
IBM 360/370 I/O Port	DS75123	Not Applicable	DS75124	Not Applicable

TABLE II. Line Driver/Receiver Integrated Circuit Selection Guide for Digital Interface Standards (Continued)

Standard Designation	Part Number			
	Line Driver		Line Receiver	
	0°C to +70°C	−55°C to +125°C	0° to +70°C	−55°C to +125°C
DEC Unibus®	DS36147 DS8641 Transceiver	DS16147 DS7641 Transceiver	DS8640 DS8641 Transceiver	DS7640 DS7641 Transceiver
Microbus™	DS3628 DP8228 DP8216 DP8212 DP8340B Transceiver	DS1628 DP8228M DP8216M DP8212M	DP8304B Transceiver	
GOVERNMENT STANDARDS				
MIL-STD-188C	DS3692	DS1692	DS88LS120	DS78LS120
MIL-STD-188-114	DS3692	DS1692	DS88LS120	DS78LS120
FED-STD-1020	See RS-423			
FED-STD-1030	See RS-422			
MIL-STD-1397 (NTDS–Slow)	Use Discrete Components and/or Comparators			
MIL-STD-1397 (NTDS–Fast)	Use Discrete Components and/or Comparators			
INTERNATIONAL STANDARDS (CCITT)				
1969 White Book Vol. VIII, V. 24	See RS-232C			
Circular No. 97, X. 26	See RS-422			
Circular No. 97, X. 27	See RS-423			

2.0 (DTE) (DCE)

Data terminal equipment (DTE) to data communications equipment (DCE) interface standards

2.1 Application

The DTE/DCE standards cover the electrical, mechanical and functional interface between or among terminals (i.e., teletypewriters, CRT's etc.) and communications equipment (i.e., modems, cryptographics sets, etc.).

2.2 U.S. Industrial DTE/DCE Standards

2.2.1 EIA RS-232

RS-232C is the oldest and most widely known DTE/DCE interface standard. Viewed by many as a complete standard, it provides for one-way/non-reversible, single ended (unbalanced) non terminated line, serial digital data transmission. *Figure 1* shown below illustrates a typical application. See Table III for Specification Summary.

Important features are:

- * Positive logic (±5V min to ±15V max)
- * Fault protection
- * Slew-rate control
- * 50 feet recommended cable length
- * 20k bits per second data rate

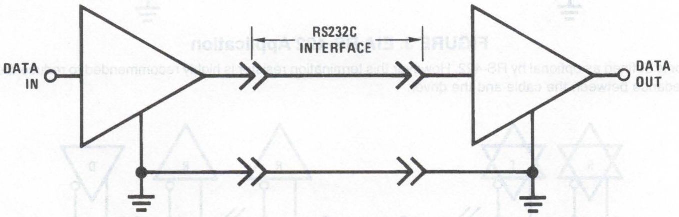

FIGURE 1. EIA RS-232C Application

2.2.2 EIA RS-422, RS-423 and RS-485

In a move to upgrade system capabilities by using state-of-the-art devices and technology the EIA in 1975, introduced two new specifications covering RS-422 balanced and RS-423 unbalanced data transmission. Both of these standards offered major advantages over the popular RS-232C interface. Understanding the advantages of the balanced interface RS-422, the EIA introduced in 1983 the RS-485 Multipoint Systems standard that eliminates several limitations of RS-422.

2.2.2.1 RS-423

RS-423 closely resembles RS-232C in that, it too specifies a one-way/non-reversible, data transmission. Several key advantages of the standard include a 100k Baud data rate at 30 feet and a balanced receiver offering an input voltage common mode (VCM) of ±7V. As shown in *Figure 2* the receiver input is referenced to the driver ground permitting ground differences between the driver and receiver. See Table IV for Specification Summary.

Important features are:

- Positive logic (±4V min to ±6V max)
- Fault protected driver outputs
- Controlled Slew-rate reduces crosstalk and reflections
- 30 feet maximum cable length at 100k Baud
- Differential receiver with ±7V VCM and ±200 mV sensitivity

2.2.2.2 RS-422

RS-422 provides for balanced data tranmission with unidirectional/non-reversible, terminated or non-terminated transmission lines. Several key advantages offered by this standard include the differential receiver defined in RS-423, a differential driver and data rates as high as 10M Baud at 40 feet. *Figure 3* shows a typical interconnect application. See Table V for Specification Summary.

2.2.2.3 RS-485

RS-485 standards accommodates the requirements on a balanced transmission line used in party-line circuit configurations. This standard is similar to RS-422 and is considered to be an extension permitting multipoint applications where multiple drivers and receivers share the same line in data transmission.

Several key characteristics of the standard that differentiate it from RS-422 are; the expanded common mode range of both the driver and receiver, (VCM range +12 to −7V), and characteristics that permit 32 drivers and receivers on the line. *Figure 4* shows a typical party-line application. Note that the transmission line which is intended to be 120Ω twisted pair is terminated at both ends. See Table VI for Specifications Summary.

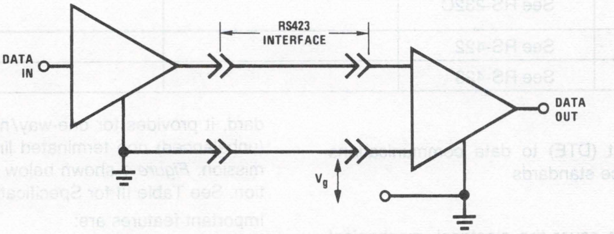

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FIGURE 2. EIA RS-423 Application

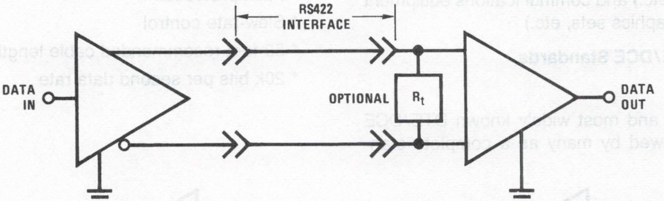

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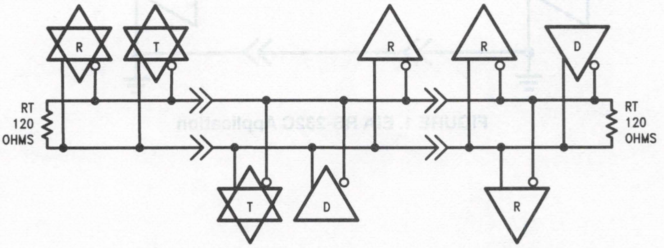
FIGURE 3. EIA RS-422 Application

Note: The termination resistor is defined as optional by RS-422. However this termination resistor is highly recommended to reduce the possibility of line reflections caused by mis-matched impedance between the cable and the driver.



D—Driver
R—Receiver
T—Transceiver

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FIGURE 4. A Typical RS-485 Party-Line Configuration

TABLE III. EIA RS-232C Specification Summary

Symbol	Parameter	Conditions	EIA RS-232C Min	EIA RS-232C Typ	EIA RS-232C Max	Units
V_{OH}	Driver Output Voltage Open				25	V
V_{OL}	Circuit		−25			V
V_{OH}	Driver Output Voltage Loaded	$3\ k\Omega \leq R_L \leq 7\ k\Omega$	5		15	V
V_{OL}	Output		−15		−5	V
R_O	Driver Output Resistance Power Off	$-2V \leq V_O \leq 2V$			300	Ω
I_{OS}	Driver Output Short-Circuit Current		−500		500	mA
	Driver Output Slew Rate					
	All Interchange Circuits				30	V/μs
	Control Circuits		6			V/ms
	Rate and Timing Circuits		6			V/ms
		% of Unit Interval	4			%
R_{IN}	Receiver Input Resistance	$3V \leq V_{IN} \leq 25V$	3000		7000	Ω
	Receiver Open Circuit Input Bias Voltage		−2		2	V
	Receiver Input Threshold					
	Output = MARK		−3			V
	Output = SPACE				3	V

TABLE IV. EIA RS-423 Specification Summary

Symbol	Parameter	Conditions	EIA RS-423 Min	EIA RS-423 Typ	EIA RS-423 Max	Units
V_O	Driver Unloaded Output Voltage		4		6	V
$\overline{V_O}$			−4		−6	V
V_T	Driver Loaded Output Voltage	$R_L = 450\Omega$	3.6			V
$\overline{V_T}$			−3.6			V
R_S	Driver Output Resistance				50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			±150	mA
	Driver-Output Rise and Fall Time	Baud Rate ≤ 1k Baud			300	μs
		Baud Rate ≥ 1k Baud			30	% Unit Interval
I_{OX}	Driver Power OFF Current	$V_O = \pm 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} \leq \pm 7V$			±200	mV
V_{CM}	Receiver Common-Mode Range				±10	V
R_{IN}	Receiver Input Resistance		4000			Ω
	Receiver Common-Mode Input Offset				±3	V

TABLE V. EIA RS-422 Specification Summary

Symbol	Parameter	Conditions	EIA RS-422 Min	EIA RS-422 Typ	EIA RS-422 Max	Units
V_O	Driver Unloaded Output Voltage				6	V
$\overline{V_O}$					−6	V
V_T	Driver Loaded Output Voltage	$R_T = 100\Omega$	2			V
$\overline{V_T}$			−2			V
R_S	Driver Output Resistance	Per Output			50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			150	mA
	Driver Output Rise Time				10	% Unit Interval
I_{OX}	Driver Power OFF Current	$-0.25V \leq V_O \leq 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} = \pm 7V$			200	mV
V_{CM}	Receiver Common-Mode Voltage		−12		12	V
	Receiver Input Offset		±3			V
R_{IN}	Receiver Input Resistance		4000			Ω

TABLE VI. EIA RS-485 Specification Summary

Symbol	Parameter	Conditions	EIA RS-485			Units
			Min	Typ	Max	
V_O $\overline{V_O}$	Driver Unloaded Output Voltage					V
V_T $\overline{V_T}$	Driver Loaded Output Voltage	$R_T = 100\Omega$ RS-422	2 −2			V V
		$R_T = 54\Omega$, CL = 50 pF RS-485	1.5 −1.5			V V
I_{OS}	Driver Output Short-Circuit Current	$V_O = \pm 12V$ $V_O = -7V$			250 −250	mA mA
V_{OS}	Driver Common Mode Output Voltage				3	V
$V_{OS} - V_{\overline{OS}}$	Difference in Common Mode Offset				0.2	V
V_{TH}	Receiver Sensitivity	$-7V \leq V_{CM} \leq +12V$			200	mV
V_{CM}	Receiver Common Mode Voltage		−7		+12	V
R_{IN}	Receiver Input Resistance		12k			Ω

2.3 International Standards

2.3.1 CCITT 1969 White Book Vol. VIII, V.24. This standard is identical to RS-232C.

2.3.2 CCITT circular No. 97 Com SPA/13, X. 26. This standard is similar to RS-422 with the exception that the receiver sensitivity at the specified maximum common-mode voltage (±7V) shall be ±300 mV vs ±200 mV for RS-422.

2.3.3 CCITT circular No. 97 Com SPA/13, X. 27. This standard is similar to RS-423 with 2 exceptions:

a) The receiver sensitivity is as specified in paragraph X.26, and

b) The driver output voltage is specified at a load resistance of 3.9 kΩ.

2.4 U.S. Military Standards

2.4.1 MIL-STD-188C (Low Level)

The military equivalent to RS-232C is MIL-STD-188C. Devices intended for RS-232C can be applied to MIL-STD-188C by use of external wave shaping components on the driver end and input resistance and threshold tailoring on the receiver end.

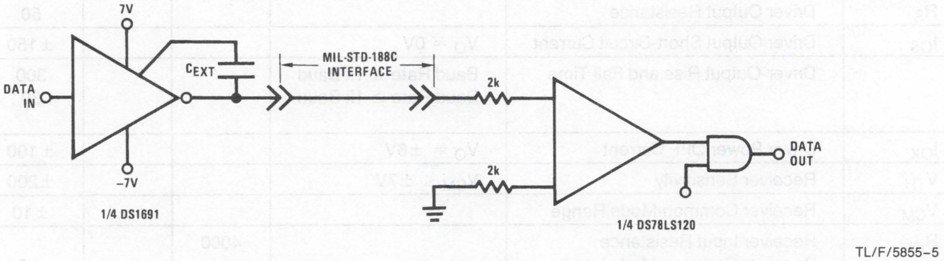


FIGURE 5. MIL-STD-188C Application

TABLE VII. MIL-STD-188C Specification Summary

Symbol	Parameter	Conditions	MIL-STD-188C Low Level Limits			Units
			Min	Typ	Max	
V_{OL}	Driver Output Voltage Open Circuit	(Note 1)	5		7	V
V_{OL}			−7		−5	V
R_O	Driver Output Resistance Power ON	$I_{OUT} \leq 10$ mA			100	Ω
I_{OS}	Driver Output Short-Circuit Current		−100		100	mA
	Driver Output Slew Rate All Interchange Circuits Control Circuits Rate and Timing Circuits	(Note 2)	5		15	% IU
R_{IN}	Receiver Input Resistance	Mode Rate ≤ 200k Baud	6			kΩ
	Receiver Input Threshold					
	Output = MARK	(Note 3)			100	µA
	Output = SPACE		−100			µA

Note 1: Ripple <0.5%, V_{OH}, V_{OL} matched to within 10% of each other.

Note 2: Waveshaping required on driver output such that the signal rise or fall time is 5% to 15% of the unit interval at the applicable modulation rate.

Note 3: Balance between marking and spacing (threshold) currents actually required shall be within 10% of each other.

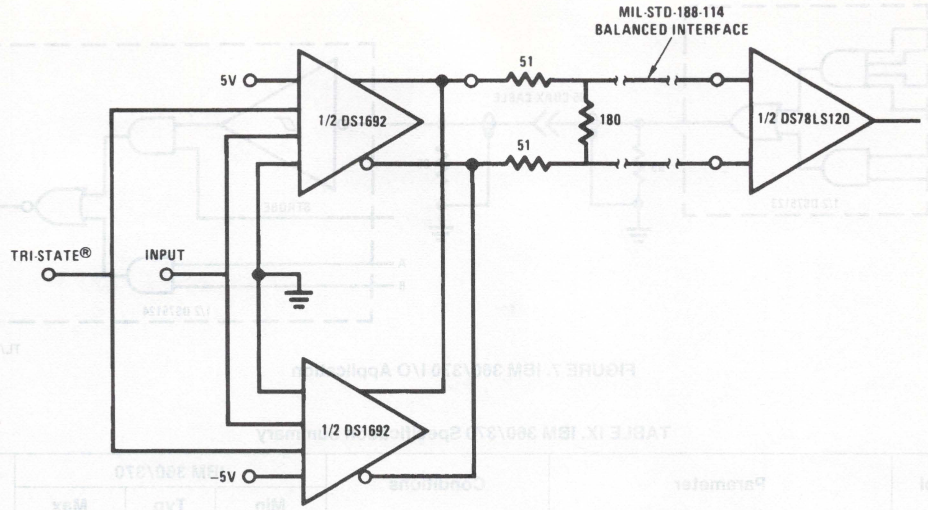


FIGURE 6. MIL-STD-188-114 (Balanced Applications)

2.4.2 MIL-STD-188-114 Balanced

This standard is similar to RS-422 with the exception that the driver offset voltage level is limited to ±0.4V vs ±3V allowed in RS-422.

2.4.3 MIL-STD-188-114 Unbalanced.

This standard is similar to RS-423 with the exception that loaded circuit driver output voltage at $R_L = 450\Omega$ must be 90% of the open circuit output voltage vs ±2V at $R_S = 100\Omega$ for RS-422.

2.4.4 MIL-STD-1397 (Slow and Fast)

2.5 FED-STD-1020/1030

U.S. Government (non-military) standards FED-STD-1020 and 1030 are identical without exception to EIA RS-423 and RS-422, respectively.

3.0 COMPUTER TO PERIPHERAL INTERFACE STANDARDS

To date, the only standards dealing with the interface between processors and other equipment are the "defacto" standards in the form of specifications issued by IBM and DEC covering the models 360/370 I/O ports and the Unibus, respectively.

3.1 GA-22-6974-0

IBM specification GA-22-6974-0 covers the electrical characteristics, the format of information and the control sequences of the data transmitted between 360/370's and up to 10 I/O ports.

The interface is an unbalanced bus using 95Ω, terminated, coax cables. Devices connected to the bus should feature short-circuit protection, hysteresis in the receivers, and open-emitter drivers. Careful attention should be paid to line lengths and quality in order to limit cable noise to less than 400 mV.

TABLE VIII. MIL-STD-1397 Specification Summary

Symbol	Parameter	Conditions	Comparison Limits (MIL-STD)		Units
			1397 (Slow)	1397 (Fast)	
	Data Transmission Rate		42	250	k Bits/Sec
V_{OH} V_{OL}	Driver Output Voltage		±1.5 −10 to −15.5	0 −3	V V
I_{OH} I_{OL}	Driver Output Current		≥ −4 1		mA mA
R_S	Driver Power OFF Impedance		≥100		kΩ
V_{IH} V_{IL}	Receiver Input Voltage	Fail-Safe Open Circuit	≤4.5 ≥ −7.5	≤ −1.1 ≥ −1.9	V V

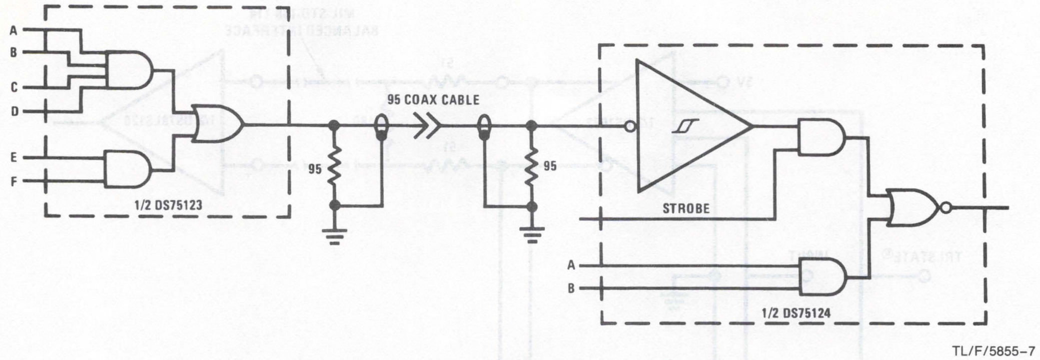

A
B
C
D
E
F
1/2 DS75123
95
95 COAX CABLE
95
STROBE
A
B
1/2 DS75124
TL/F/5855-7

FIGURE 7. IBM 360/370 I/O Application

TABLE IX. IBM 360/370 Specification Summary

Symbol	Parameter	Conditions	IBM 360/370			Units
			Min	Typ	Max	
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA			7	V
V_{OH}		I_{OH} = 30 µA			5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11			V
V_{OL}		I_{OL} = −240 µA			0.15	V
V_{IH} V_{IL}	Receiver Input Threshold Voltage		0.7		1.7	V V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V			−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24			mA
	Receiver Input Voltage Range					
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
R_{IN}	Receiver Input Impedance	0.15V ≤ V_{IN} ≤ 3.9V	7400			Ω
I_{IN}	Receiver Input Current	V_{IN} = 0.15V			240	µA
Z_O	CABLE Impedance		83		101	Ω
R_O	CABLE Termination	P_D ≥ 390 mW	90		100	Ω
	Line Length (Specified as Noise on Signal and Ground Lines)				400	mV

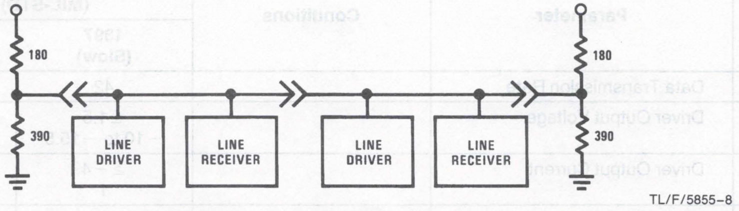

5V
180
390
LINE DRIVER
LINE RECEIVER
LINE DRIVER
LINE RECEIVER
180
390
TL/F/5855-8

FIGURE 8. DEC Unibus Application

TABLE X. DEC Unibus Specification Summary

Symbol	Parameter	Conditions	DEC Unibus			Units
			Min	Typ	Max	
V_{OL}	Driver Output Voltage	$I_{OL} = 50$ mA			0.7	V
V_O		Absolute Maximum			7	V
V_{IH}	Receiver Input Voltage		1.7			V
V_{IL}					1.3	V
I_{IH}	Receiver Input Current	$V_{IN} = 4V$			100	μA
I_{IL}		$V_{IN} = 4V$ Power OFF			100	μA

3.2 DEC UNIBUS

Another example of an unofficial industry standard is the interface to a number of DEC minicomputers. This interface, configured as a 120Ω double-terminated data bus is given the name Unibus. Devices connected to the bus should feature hysteresis in the receivers and open-collector driver outputs. Cable noise should be held to less than 600 mV.

4.0 INSTRUMENTATION TO COMPUTER INTERFACE STANDARDS

4.1 INTRODUCTION

The problem of linking instrumentation to processors to handle real-time test and measurement problems was largely a custom interface problem. Each combination of instruments demanded unique interfaces, thus inhibiting the wide spread usage of small processors to day-to-day test, measurement and control applications.

Two groups addressed the problem for specific environments. The results are:

a) IEEE 488 bus standard based upon proposals made by HP, and

b) The CAMAC system pioneered by the nuclear physics community.

4.2 IEEE 488

IEEE 488 covers the functional, mechanical and electrical interface between laboratory instrumentation (i.e., signal generators, DPM's, counters, etc.) and processors such as programmable calculators and minicomputers. Equipment with IEEE 488 I/O ports can be readily daisy chained in any combination of up to 15 equipments (including processor) spanning distances of up to 60 feet. 16 lines (3 handshake, 5 control and 8 data lines) are required.

4.3 CAMAC

The CAMAC system is the result of efforts by those in the nuclear physics community to standardize the interface between laboratory instruments and computers before the introduction of IEEE 488.

It allows either serial or parallel interconnection of instruments via a "crate" controller.

The electrical requirements of the interfaces are compatible with DTL and TTL logic levels.

5.0 MICROPROCESSOR SYSTEMS INTERFACE STANDARDS

5.1 Microprocessor Systems

Microprocessor systems are bus organized systems with two types of bus requirements:

a) Minimal system: for data transfer over short distances (usually on 1 PC board), and,

b) Expanded system: for data transfer to extend the memory or computational capabilities of the system.

5.2 Minimal Systems and Microbus

Microbus considers the interface between MOS/LSI microprocessors and interfacing devices in close physical proximity which communicate over 8-bit parallel unified bus systems. It specifies both the functional and electrical characteristics of the interface and is modeled after the 8060, 8080 and 8090 families of microprocessors as shown in *Figures 10, 11* and *12*.

The electrical characteristics of Microbus are shown in Table XII.

TABLE XI. IEEE 488 Specification Summary

Symbol	Parameter	Conditions	IEEE 488			Units
			Min	Typ	Max	
V_{OH}	Driver Output Voltage	$I_{OH} = -5.2$ mA	2.4			V
V_{OL}		$I_{OL} = 48$ mA			0.4	V
	Driver Output Current					
I_{OZ}	TRI-STATE®	$V_O = 2.4V$			±40	μA
I_{OH}	Open Collector	$V_O = 5.25V$			250	μA
V_{IH}	Receiver Input Voltage	0.4V Hysteresis Recommended	2.0			V
V_{IL}					0.8	V
I_{IH}	Receiver Input Current	$V_{IN} = 2.4V$			40	μA
I_{IL}		$V_{IN} = 0.4V$			−1.6	mA
	Receiver Clamp Current	$V_{IN} = -1.5V$			12	mA
R_{L1}	Termination Resistor	$V_{CC} = 5V\ (\pm 5\%)$	2850		3150	
R_{L2}		V = Gnd	5890		6510	

TABLE XII. Microbus Electrical Specification Summary

Symbol	Parameter	Driver	Receiver		Units
			Standard	Hysteresis (Recommended)	
V_{OL}	Output Voltage (At 1.6 mA)	≤0.4V			
V_{OH}	(At −100 µA)	≥2.4V			
V_{IL}	Input Voltage		0.8	0.6	V
V_{IH}			2.0	2.0	V
	Internal Capacitive Load at 25°C	15	10	10	pF
t_r	Rise Time (Maximum)	100			ns
t_f	Fall Time (Maximum)	100			ns

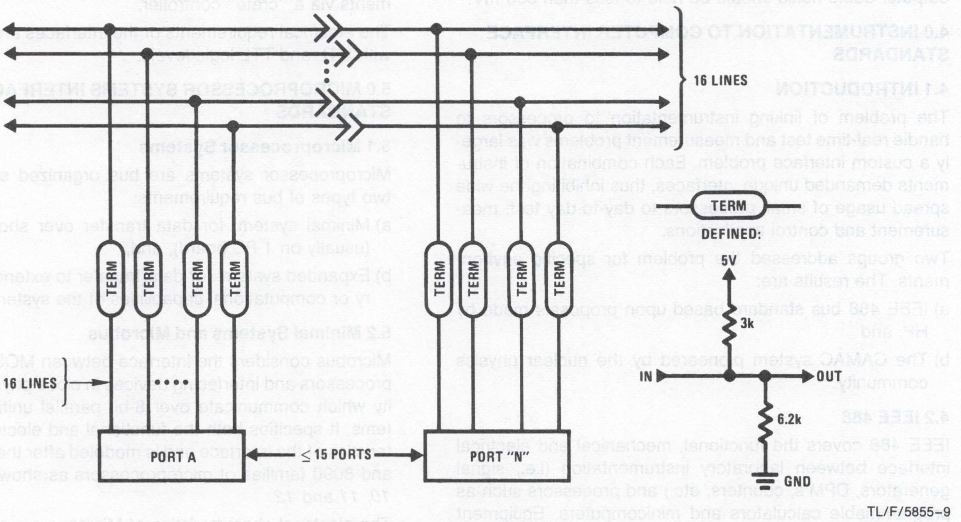

16 LINES
TERM
TERM
TERM
TERM
TERM
TERM
TERM
TERM
16 LINES
PORT A
≤15 PORTS
PORT "N"
TERM
DEFINED:
5V
3k
IN
OUT
6.2k
GND
TL/F/5855-9

FIGURE 9. IEEE 488 Application

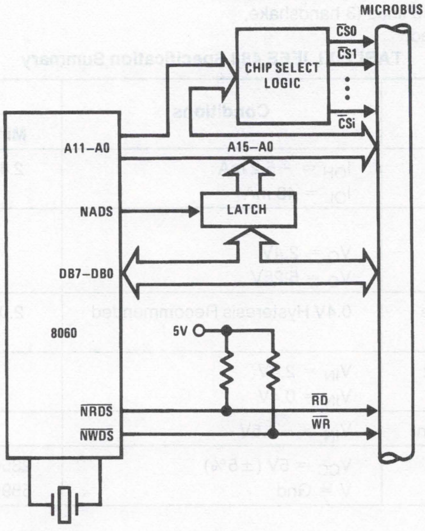
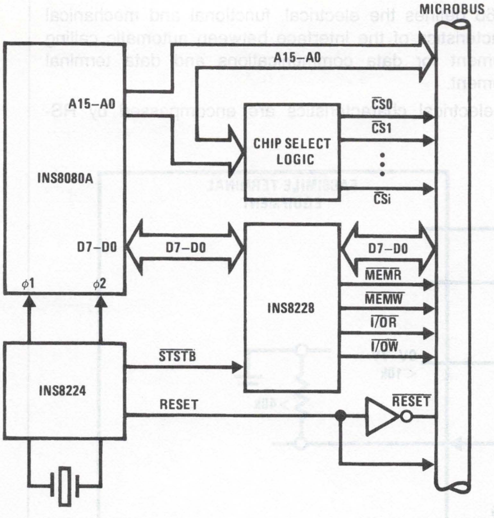

MICROBUS
$\overline{CS0}$
$\overline{CS1}$
$\overline{CSi}$
CHIP SELECT LOGIC
A11–A0
A15–A0
NADS
LATCH
DB7–DB0
8060
5V
$\overline{NRDS}$
$\overline{NWDS}$
$\overline{RD}$
$\overline{WR}$
TL/F/5855-10

FIGURE 10. 8060 SC/MP II System Moldel


MICROBUS
A15–A0
A15–A0
CS0
CS1
CHIP SELECT LOGIC
CSi
INS8080A
D7–D0
D7–D0
D7–D0
MEMR
MEMW
I/OR
I/OW
INS8228
φ1
φ2
STSTB
INS8224
RESET
RESET

TL/F/5855–11

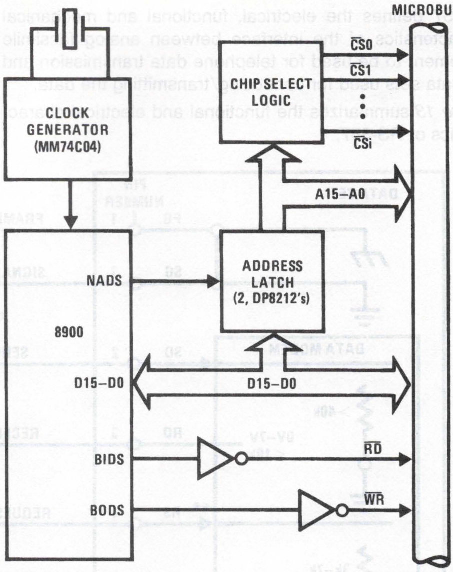
FIGURE 11. 8080 System Model for the Basic Microbus Interface

5.3 Expanded Microprocessor System Interfaces

Since the outputs of most microprocessor devices are limited to a loading of one relative to a TTL load, expanded system will require buffers on both their address and data lines.

To date, no formal standards exist which govern this interface. However, "defacto" standards are emerging in the form of the specifications for "recommended devices" which are mentioned in the data sheets and application notes for the widely sourced microprocessor devices. Here, the answer to the question of how to provide a "standard" interface is simplified to that of proper usage of recommended devices.

Table XIII summarizes the important electrical characteristics of recommended bus drivers for expanded microprocessor systems.


MICROBUS
CLOCK GENERATOR (MM74C04)
CS0
CS1
CHIP SELECT LOGIC
CSi
A15–A0
NADS
ADDRESS LATCH (2, DP8212's)
8900
D15–D0
D15–D0
BIDS
RD
BODS
WR

TL/F/5855–12

FIGURE 12. 8900 System Model

6.0 OTHER INTERFACE STANDARDS

Some other commonly occurring interfaces which have become standardized are:

a) Interface between facsimile terminals and voice frequency communication terminals,

b) Interface between terminals and automatic calling equipment used for data communications, and

c) Interface between numerically controlled equipment and data terminals.

TABLE XIII. Recommended Specification of Bus Drivers for Expanded Microprocessor Systems

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}			2			V
V_{IL}					0.8	V
V_{OH}	Driver Output Voltage	$I_{OH} = -10$ mA	2.4			V
V_{OL}		$I_{OL} = 48$ mA			0.5	V
I_{OS}	Short-Circuit Current	$V_{CC} = 5.25$V			−150	mA
C_L	Bus Drive Capability		300			pF

6.1 EIA RS-357

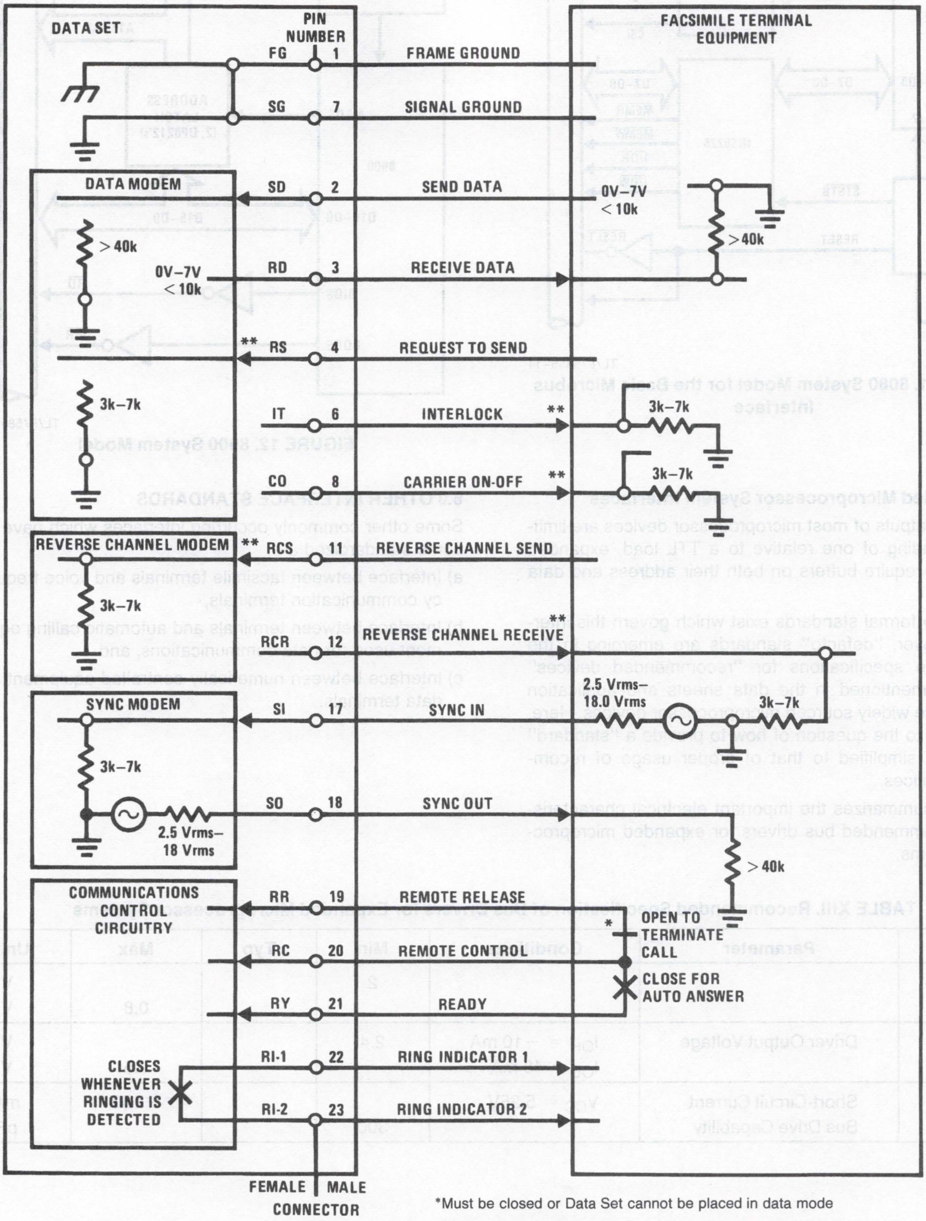
RS-357 defines the electrical, functional and mechanical characteristics of the interface between analog facsimile equipment to be used for telephone data transmission and the data sets used for controlling/transmitting the data.

Figure 13 summarizes the functional and electrical characteristics of RS-357.

6.2 EIA RS-366

RS-366 defines the electrical, functional and mechanical characteristics of the interface between automatic calling equipment for data communications and data terminal equipment.

The electrical characteristics are encompassed by RS-232C.



DATA SET
PIN NUMBER
FACSIMILE TERMINAL EQUIPMENT
FG 1 FRAME GROUND
SG 7 SIGNAL GROUND
DATA MODEM
SD 2 SEND DATA
0V–7V < 10k
> 40k
RD 3 RECEIVE DATA
0V–7V < 10k
> 40k
** RS 4 REQUEST TO SEND
3k–7k
IT 6 INTERLOCK **
3k–7k
CO 8 CARRIER ON-OFF **
3k–7k
REVERSE CHANNEL MODEM ** RCS 11 REVERSE CHANNEL SEND
3k–7k
RCR 12 REVERSE CHANNEL RECEIVE **
SYNC MODEM
SI 17 SYNC IN
2.5 Vrms– 18.0 Vrms
3k–7k
3k–7k
SO 18 SYNC OUT
2.5 Vrms– 18 Vrms
> 40k
COMMUNICATIONS CONTROL CIRCUITRY
RR 19 REMOTE RELEASE
RC 20 REMOTE CONTROL
RY 21 READY
* OPEN TO TERMINATE CALL
CLOSE FOR AUTO ANSWER
CLOSES WHENEVER RINGING IS DETECTED
RI-1 22 RING INDICATOR 1
RI-2 23 RING INDICATOR 2
FEMALE | MALE
CONNECTOR

*Must be closed or Data Set cannot be placed in data mode

**Receive	Sensitivity	Source
ON	3V–25V	5V–25V
OFF	3V–25V	5V–25V

TL/F/5855–13

FIGURE 13. Functional and Electrical Characteristics RS-357

6.3 EIA RS-408

RS-408 recommends the standardization of the 2 interfaces shown in *Figure 14*.

The electrical characteristics of NCE to DTE interface are, in summary, those of conventional TTL drivers (series 7400) with:

$V_{OL} \leq 0.4V$ at $I_{OL} = 48$ mA

$V_{OH} \geq 2.4V$ at $I_{OH} \leq -1.2$ mA, and

$C_L \leq 2000$ pF.

Short circuit protection should be provided.

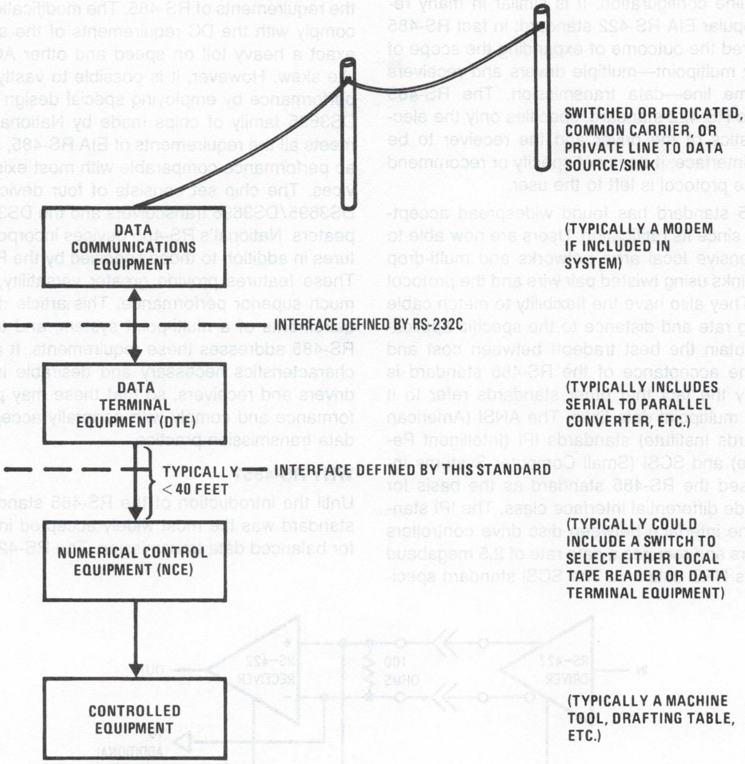

SWITCHED OR DEDICATED, COMMON CARRIER, OR PRIVATE LINE TO DATA SOURCE/SINK
DATA COMMUNICATIONS EQUIPMENT
(TYPICALLY A MODEM IF INCLUDED IN SYSTEM)
INTERFACE DEFINED BY RS-232C
DATA TERMINAL EQUIPMENT (DTE)
(TYPICALLY INCLUDES SERIAL TO PARALLEL CONVERTER, ETC.)
TYPICALLY <40 FEET
INTERFACE DEFINED BY THIS STANDARD
(TYPICALLY COULD INCLUDE A SWITCH TO SELECT EITHER LOCAL TAPE READER OR DATA TERMINAL EQUIPMENT)
NUMERICAL CONTROL EQUIPMENT (NCE)
CONTROLLED EQUIPMENT
(TYPICALLY A MACHINE TOOL, DRAFTING TABLE, ETC.)
TL/F/5855-14

FIGURE 14. EIA RS-408 Interface Applications

Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard

National Semiconductor
Application Note 409
Sivakumar Sivasothy

INTRODUCTION

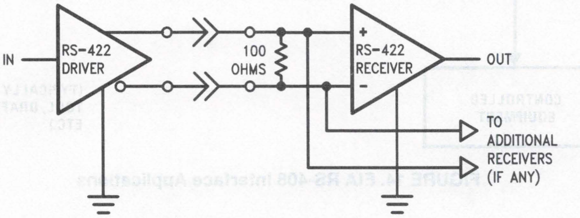
The Electronics Industries Association (EIA), in 1983, approved a new balanced transmission standard called RS-485. The EIA RS-485 standard addresses the problem of data transmission, where a balanced transmission line is used in a party-line configuration. It is similar in many respects to the popular EIA RS-422 standard; in fact RS-485 may be considered the outcome of expanding the scope of RS-422 to allow multipoint—multiple drivers and receivers sharing the same line—data transmission. The RS-485 standard, like the RS-422 standard, specifies only the electrical characteristics of the driver and the receiver to be used at the line interface; it does not specify or recommend any protocol. The protocol is left to the user.

The EIA RS-485 standard has found widespread acceptance and usage since its ratification. Users are now able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice. They also have the flexibility to match cable quality, signalling rate and distance to the specific application and thus obtain the best tradeoff between cost and performance. The acceptance of the RS-485 standard is also reflected by the fact that other standards refer to it when specifying multipoint data links. The ANSI (American National Standards Institute) standards IPI (Intelligent Peripheral Interface) and SCSI (Small Computer Systems Interface) have used the RS-485 standard as the basis for their voltage mode differential interface class. The IPI standard specifies the interface between disc drive controllers and host adapters and requires a data rate of 2.5 megabaud over a 50 meters NRZ data link. The SCSI standard specifies the interface between personal computers, disc drives and printers at data rates up to a maximum of 4 megabaud over 25 meters.

It is not possible to use standard gate structures and meet the requirements of RS-485. The modifications necessary to comply with the DC requirements of the standard, tend to exact a heavy toll on speed and other AC characteristics like skew. However, it is possible to vastly improve the ac performance by employing special design techniques. The DS3695 family of chips made by National Semiconductor meets all the requirements of EIA RS-485, and still provides ac performance comparable with most existing RS-422 devices. The chip set consists of four devices; they are the DS3695/DS3696 transceivers and the DS3697/DS3698 repeaters. National's RS-485 devices incorporate several features in addition to those specified by the RS-485 standard. These features provide greater versatility, easier use and much superior performance. This article discusses the requirements of a multi-point system, and the way in which RS-485 addresses these requirements. It also explains the characteristics necessary and desirable in the multi-point drivers and receivers, so that these may provide high performance and comply with generally accepted precepts of data transmission practice.

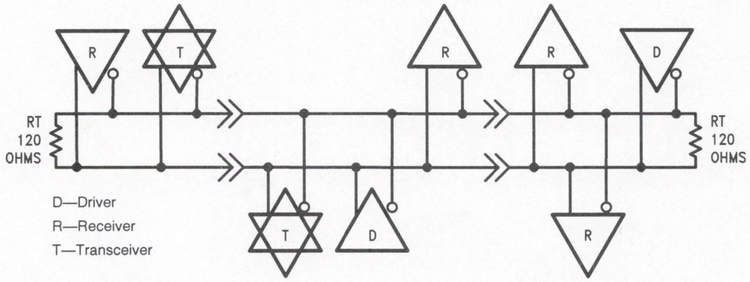
WHY RS-485?

Until the introduction of the RS-485 standard, the RS-422 standard was the most widely accepted interface standard for balanced data transmission. The RS-422 drivers and re-



TL/F/8579-1

FIGURE 1a. An RS-422 Configuration



TL/F/8579-2

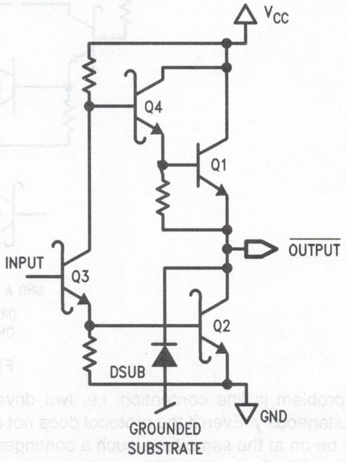
FIGURE 1b. A Typical RS-485 Party-Line Configuration

ceivers were intended for use in the configuration shown in *Figure 1a*. The driver is at one end of the line; the termination resistor (equal to 100Ω) and up to 10 receivers reside at the other end of the line. This approach works well in simplex (unidirectional) data transmission applications, but creates problems when data has to be transmitted back and forth between several pieces of equipment. If several Data Terminal Equipments (DTEs) have to communicate with one another over long distances using RS-422 links, two such balanced lines have to be established between each pair of DTEs. The hardware cost associated with such a solution would normally be unacceptable.

A party line is the most economical solution to the above problem. RS-422 hardware could conceivably be used to implement a party line if the driver is provided with TRI-STATE® capability, but such an implementation would be subjected to severe restrictions because of inadequacies in the electrical characteristics of the driver. The biggest problem is caused by ground voltage differences. The common mode voltage on a balanced line is established by the enabled driver. The common mode voltage at the receiver is the sum of the driver offset voltage and the ground voltage difference between the driver and the receiver. In simplex systems only the receiver need have a wide common mode range. Receiver designs that provide a wide common mode range are fairly straightforward. In a party-line network several hundred feet long, in which each piece of equipment is earthed at a local ac outlet, the ground voltage difference between two DTEs could be as much as a few volts. In such a case both the receiver and the driver must have a wide common mode range. Most RS-422 drivers are not designed to remain in the high impedance state over a wide enough common mode range, to make them immune to even small ground drops.

Classical line drivers are vulnerable to ground drops because of their output stage designs. A typical output stage is shown in *Figure 2a*. Two such stages driven by complementary input signals, may be used to provide the complementary outputs of a differential line driver. Transistors Q1 and Q4 form a Darlington pull up for the totem pole output stage; Q2 is the pull down transistor. The phase splitter Q3 switches current between the upper and lower transistors to obtain the desired output state. DSUB is the diode formed by the collector of Q2 and the grounded substrate of the integrated circuit. The output in *Figure 2a* can be put into the high impedance state by pulling down the bases of transistors Q3 and Q4. Unfortunately, the high impedance state cannot be maintained if the output is pulled above the power supply voltage or below ground voltage. In party-line applications, where ground voltage differences of a few volts will be common, it is essential that the drivers be able to hold the high impedance state while their outputs are taken above V_{CC} and below ground.

The output in *Figure 2a* can be taken high until the emitter-base junction of Q1 breaks down. Thereafter, the output will be clamped to a zener voltage plus a base-collector diode voltage above V_{CC}; V_{CC} could be zero if the device is powered off. If the output is taken below ground, it will cause the substrate diode, DSUB, associated with Q2 to turn on and clamp the output voltage at a diode drop below ground. If a disabled driver turns on and clamps the line, the signal put out by the active driver will get clipped and distorted. It is also possible for ground drops to cause dangerously large substrate currents to flow and damage the devices as illustrated in *Figure 2b*. *Figure 2b* depicts two drivers A and B; it shows the pull down transistors (Q2A and Q2B) and their associated substrate diodes (DSUB-A and DSUB-B) for the two drivers A and B. Here driver A is ON in the low output state; driver B is disabled, and therefore, should neither source nor sink current. The ground of driver A is 3 volts lower than that of driver B. Consequently, the substrate diode DSUB-B sees a forward bias voltage of about 2.7V (the collector-emitter voltage of Q2A will be about 0.3V), which causes hundreds of milliamperes of current to flow out of it.



TL/F/8579-3

FIGURE 2a. Driver Output Stage (not RS-485)

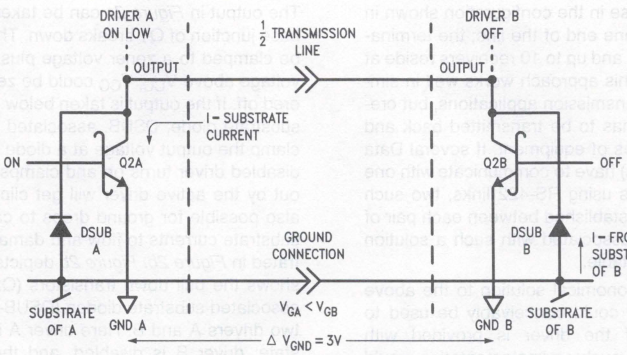


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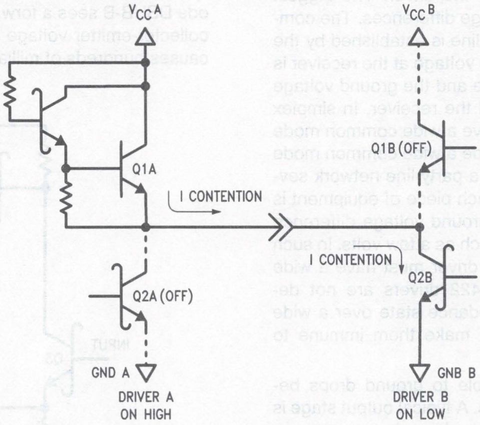
FIGURE 2b. Two DCEs Separated by a Ground Drop



TL/F/8579–5

FIGURE 2c. Bus Contention

Another problem is line contention, i.e. two drivers being 'ON' simultaneously. Even if the protocol does not allow two drivers to be on at the same time, such a contingency could arise as a result of a fault condition. A line contention situation, where two drivers are on at the same time, is illustrated in *Figure 2c*. Here, drivers A and B are 'ON' simultaneously; driver A is trying to force a high level on the line whereas driver B is trying to force a low level. Transistors Q1A and Q2B are 'ON' while transistors Q2A and Q1B are 'OFF'. As a result, a large current is sourced by Q1A and sunk by Q2B; the magnitude of this current is limited only by the parasitic resistances of the two devices and the line. The problem is compounded by any ground drop that may exist between the two contending drivers. This large contention current can cause damage to one or both of the contending drivers. Most RS-422 drivers are not designed to handle line contention.

A multi-point driver should also be capable of providing more drive than a RS-422 driver. The RS-422 driver is only required to drive one 100Ω termination resistor, and ten receivers each with an input impedance no smaller than 4 kΩ. A party-line, however, would have to be terminated at both ends; it should also be able to drive more devices to be useful and economical.

Because of the above limitations, it is quite impractical to use RS-22 hardware to interconnect systems on a party-line. Clearly, a new standard had to be generated to meet the more stringent hardware requirements of muti-point data links.

THE RS-485 STANDARD

The RS-485 standard specifies the electrical characteristics of drivers and receivers that could be used to implement a balanced milti-point transmission line (party-line). A data exchange network using these devices will operate properly in the presence of reasonable ground drops, withstand line contention situations and carry 32 or more drivers and receivers on the line. The intended transmission medium is a 120Ω twisted pair line terminated at both ends in its characteristic impedance. The drivers and receivers can be distributed between the termination resistors as shown in *Figure 1b*.

The effects of ground voltage differences are mitigated by expanding the common mode voltage (V_{CM}) range of the driver and the receiver to $-7V < V_{CM} < +12V$. A driver forced into the high impedance state, should be able to have its output taken to any voltage in the common mode range and still remain in the high impedance state, whether powered on or powered off. The receiver should respond properly to a 200 mV differential signal super-imposed on any common mode voltage in this range. With a 5V power supply, the common mode voltage range specified by RS-485 has a 7V spread from either supply terminal. The system will therefore perform properly in the presence of ground drops and longitudinally coupled extraneous noise, provided that the sum of these is less than 7 volts.

The output drive capability of the driver and the input impedance of the receiver are increased to accommodate two termination resistors and several devices (drivers, receivers and transceivers) on the line. The RS-485 standard defines a 'unit load' so that the load presented to the line by each device can be expressed in terms of unit loads (a 12 kΩ resistor, with one end tied to any voltage between ground and $V_{CC}/2$, will satisfy the requirements of a unit load). It was anticipated that most manufacturers would design their drivers and receivers such that the combined load of one receiver and one disabled driver would be less than one unit load. This would require the RS-485 receiver to have three times the input resistance of a RS-422 receiver. The required receiver sensitivity is ±200 mV—the same as for RS-422. The driver is required to provide at least 1.5V across its outputs when tied to a terminated line populated with 32 transceivers. Although this output voltage is smaller than the 2.0V specified for RS-422, a careful design of the driver, with special regard to ac performance, can allow the user to operate a multi-point network at data rates and distances comparable to RS-422.

RS-485 has additional specifications to guarantee device safety in the event of line contention or short circuits. An enabled driver whose output is directly shorted to any voltage in the common mode range, is required to limit its current output to ±250 mA. Even with such a current limit, it is possible for a device to dissipate as much as 3 Watts (if the device draws 250 mA while shorted to 12 volts). Power dissipation of such a magnitude will damage most ICs; therefore, the standard requires that manufacturers include some additional safeguard(s) to protect the devices in such situations.

The ±250 mA current limit also serves another purpose. If a contending driver is abruptly turned off, a voltage transient, of magnitude $I_CZ/2$, is reflected along the line as the line discharges its stored energy (I_C is the contention current and Z is the characteristic impedance of the line). This voltage transient must be small enough to avoid breaking down the output transistors of the drivers on the line. If the contention current is limited to 250 mA, the magnitude of this voltage transient, on a 120Ω line, is limited to 15V, a value that is a good compromise between transistor breakdown voltage and speed.

AC PERFORMANCE

To achieve reliable transmission at high data rates over long distances, the driver should have optimum ac characteristics. The response should be fast and the output transients sharp and symmetrical.

(1) **Propagation Delay:** The propagation delay through the driver should be small compared to the bit interval so that the data stream does not encounter a bottle-neck at the driver. If the propagation delay is comparable to the bit interval, the driver will not have time to reach the full voltage swing it is capable of. In lines a few hundred feet long, the line delay would impose greater limits on data throughput than the driver propagation delay. However, a fast driver would be desirable for short haul networks such as those in automobile vehicles or disc drives; in the latter case high data throughput would be essential. Driver propagation delays less than 20 ns would be very good for a wide range of applications.

(2) **Transition Time:** For distortion free data transmission, the signal at the farthest receiver must have rise and fall times much smaller than the bit interval. Signal distortion results from driver imbalance, receiver threshold offset and skew. RS-485 limits the DC imbalance in the driver output to ±0.2V i.e., 13% of worst-case signal amplitude. Usually, the greatest distortion is caused by offset in the receiver threshold. In a long line in which a 1.5V driver output signal amplitude is attenuated by the loop resistance to about 0.4V, a 200 mV offset in the receiver threshold can cause severe pulse width distortion if the rise time is comparable to the bit interval. For lines longer than about five hundred feet, the rise time would be dominated by the line and not the driver. In short-haul networks, the transient response of the driver can significantly affect signal distortion; a faster transient creates less distortion and hence permits a smaller bit interval and a higher baud rate. A rise time less than 20 ns will be a good target spec., for it will permit a baud rate of 10 Meg over 50′ of standard twisted pair wire with less than 5% distortion.

The driver should provide the above risetime and propagation delay numbers while driving a reasonable capacitance, say 100 pF from each output, in addition to the maximum resistive load of 54Ω. A properly terminated transmission line appears purely resistive to the driver. Most manufacturers take this into account and specify their driver delays with 15 pF loads. However, if any disabled transceivers are situated close to the driver (such that the round trip delay is less than the rise time), the input capacitances of these transceivers will appear as lumped circuit loads to the driver. The driver output rise time will then be affected by all other devices in such close proximity. In the case of high speed short-haul networks, where rise time and propagation delay are critical, several devices could be clustered in a short span. In such an instance, specifying propagation delays with 15 pF loads is quite meaningless. A 100 pF capacitive load is more reasonable; even if we allocate a generous 20 pF per transceiver, it allows up to six transceivers to be clustered together in an eight foot span (the eight foot span is the approximate round trip distance travelled by the wavefront in one rise time of 20 ns).

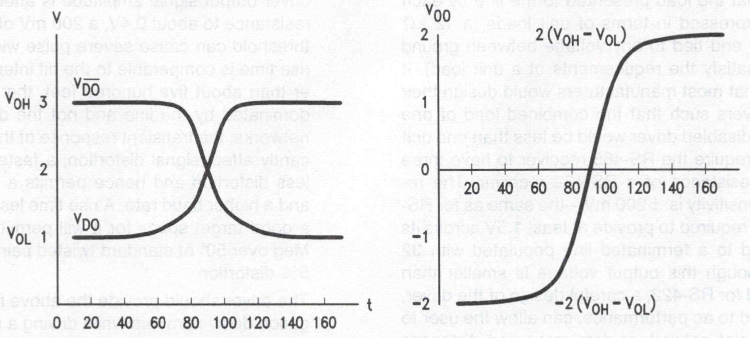
(3) **Skew:** The ideal differential driver will have the following waveform characteristics: the propagation delay times from the input to the high and low output states will be equal; the rise and fall times of the complementary outputs will be equal and the output waveforms will be perfectly symmetrical.

If the propagation delay to the low output state is different from the propagation delay to the high output state, there is said to be 'propagation skew' between output states. If a square wave input is fed into a driver with such skew, the output will be distorted in that it will no longer have a 50% duty cycle.

If the mid-points of the waveforms from the two complementary driver outputs are not identical, there is said to be SKEW between the complementary outputs. This type of skew is undesirable because it impairs the noise immunity of the system and increases the amount of electromagnetic emission.

Figure 3a shows the differential signal from a driver that has no skew. *Figure 3b* shows the case when there is 80 ns of skew. The first signal makes its transition uniformly and passes rapidly through 0V. The second waveform flattens out for tens of nanoseconds near 0V. Unfortunately, this flat region occurs near the receiver threshold. A common mode noise spike hitting the inputs of a slightly unbalanced receiver would create a small differential noise pulse at the receiver inputs. If this noise

Individual Output Signals **Differential Signal**



TL/F/8579-6

FIGURE 3a. Transients with no Skew

Individual Output Signals **Differential Signal**

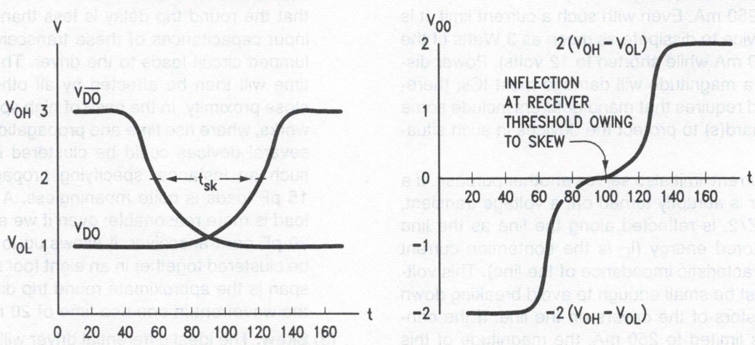


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FIGURE 3b. Skewed Transients

pulse occurs when the driver transition is flat near 0V, there will be a glitch at the receiver output. A glitch could also occur if a line reflection reaches the receiver input when the driver transition is temporarily flat. Skew is insidious in that it can cause erroneous outputs to occur at random. It can also increase the amount of electromagnetic interference (EMI) generated by the transmission system. If the complementary outputs are perfectly symmetrical, and the twisted pair medium is perfectly balanced, the radiation from one wire is cancelled exactly by the radiation from the other wire. If there is skew between the outputs, there will be net radiation proportional to the skew.

(4) **Balance:** The impedance seen looking into each of the complementary inputs of the transceiver should be identical. If there is any imbalance at these nodes, the common mode rejection will be degraded. Any DC imbalance, due to a mismatch in the receiver input resistances, will manifest itself as an offset in the receiver threshold, and can be easily detected during testing. AC imbalance is more difficult to detect, but it can hurt noise immunity at high frequencies. A sharp common mode noise spike striking an unbalanced receiver will cause a spurious differential signal. If the receiver is fast enough (as it is bound to be in most cases), it will respond to this noise signal. It is best to keep the imbalance below 4 pF. This number is reasonable to achieve; in addition, the combined imbalance of 32 transceivers will still provide sufficient immunity from h.f. interference.

DESIGN CONSIDERATIONS

The driver poses the greatest design challenge. Its speed, drive and common mode voltage requirements are best met using a bipolar process. National Semiconductor uses an established Schottky process with a 5μ deep epitaxial layer. NPN transistors are fabricated with LVCEO values greater than 15V to satisfy the breakdown requirements. It will be seen that lateral PNP transistors are crucial to the driver. The 5μ EPI process provides adequate lateral PNP transistors, and NPN transistors of sufficient speed.

Figure 4 shows the driver output circuit used by National. It is a standard totem pole output circuit modified to provide a common mode range that exceeds the supply limits. If the driver output is to be taken to −7V while the driver is in TRI-STATE, precautions must be taken to prevent the substrate diodes from turning on. This is achieved in the lower output transistor Q1 by including Schottky diode S1 in series. The only way to isolate the upper half of the totem pole from the substrate is by using a lateral PNP transistor. In *Figure 4,* a lateral PNP transistor is used to realize current source IG. Lateral PNP transistors are, however, notoriously slow; the trick therefore is not to use the PNP transistor in the switching path. In the circuit shown, the PNP transistor is a current source which feeds NPN transistor Q2 and therefore, does not participate in the switching function. This allows National's driver to have 15 ns propagation delays and 10 ns rise times. A Darlington stage cannot be used instead of Q2 because it would reduce the voltage swing below the 1.5V specification. Consequently, the rise time is bound to be significantly larger than the fall time, resulting in a large skew. National's driver uses a patented circuit with a plurality of discharge paths, to slow down the fall time so that it matches the rise time, and to keep the two transition times on track over temperature. This keeps the skew small (2 ns typical at 25°C) over the entire operating temperature range. The symmetry of the complementary outputs of National's DS3695 driver can be seen from the photographs in *Figure 5.* The lateral PNP transistor which has been kept out of the switching path has nevertheless got to be turned on or off when the driver is respectively enabled or disabled. Another patented circuit is used to hasten turn-on and turn-off of the lateral PNP transistors so that these switch in 25 ns instead of in 100 ns. Consequently, the driver can be enabled or disabled in 35 ns.

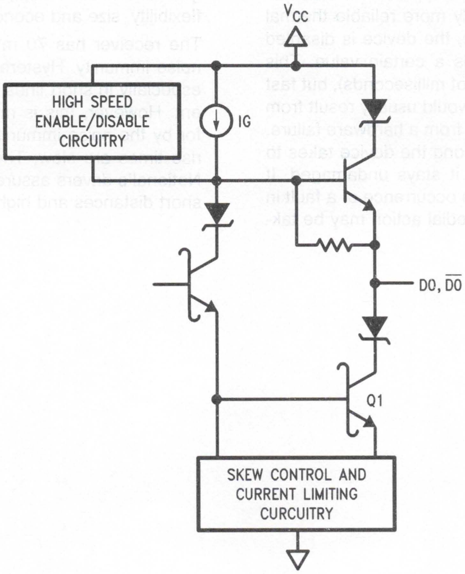
V$_{CC}$
HIGH SPEED ENABLE/DISABLE CIRCUITRY
IG
DO, $\overline{DO}$
Q1
SKEW CONTROL AND CURRENT LIMITING CURCUITRY
GND

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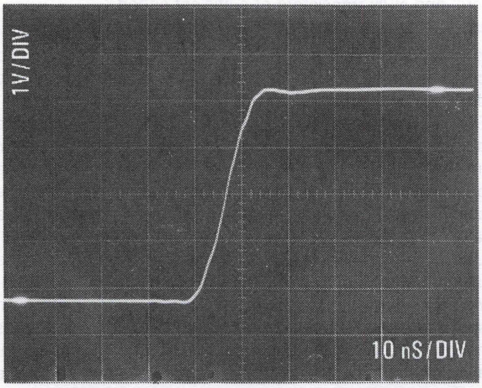
FIGURE 4


Complementary Outputs of National's RS-485 Driver

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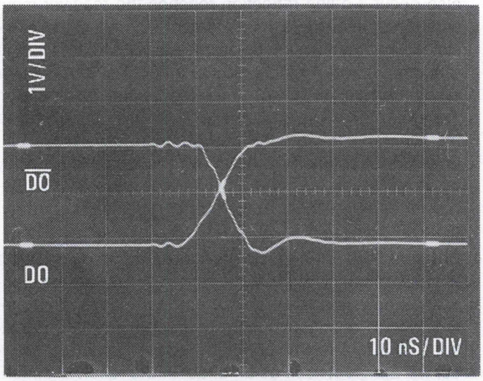
Differential Output of National's RS-485 Driver

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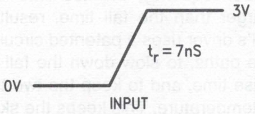

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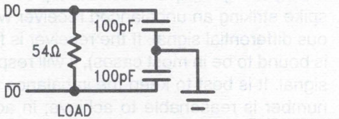

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FIGURE 5

The devices must be protected in fault conditions and contention situations. One way of doing this is by sensing current and voltage to determine power, and then if necessary, turning the device off or limiting its output current to prevent damage. This method has the advantage of fast detection of a fault and rapid recovery from one. However, too many contingencies have to be accounted for; the corresponding circuitry will increase the die size and the cost beyond what would be acceptable in many low cost applications. National preferred the simpler and inherently more reliable thermal shutdown protection scheme. Here, the device is disabled when the die temperature exceeds a certain value. This method is somewhat slower (order of milliseconds), but fast enough to protect the part. A fault would usually result from a breakdown in network protocol or from a hardware failure. In either case it is immaterial how long the device takes to shut down or recover as long as it stays undamaged. It would be useful to be notified of the occurrence of a fault in any particular channel, so that remedial action may be taken. Two of National's devices, the DS3696 receiver and the DS3698 repeater, provide a fault reporting pin which can flag the processor or drive an alarm LED in the event of a fault. National also decided to make its devices as single transceivers housed in 8 pin mini DIP packages. If thermal shutdown protection is employed, it is pointless to have dual or quad versions because a faulty channel will shut down a good one. Since most RS-485 applications will employ single channel serial data, the 8 pin package will give optimum flexibility, size and economy.

The receiver has 70 mV (typical) hysteresis for improved noise immunity. Hysteresis can contribute some distortion, especially in short lines, if the rise and fall times are different. However, this is more than adequately compensated for by the noise immunity it provides with long lines where rise times are slow. The matched rise and fall times with National's drivers assure low pulse width distortion even at short distances and high data rates.

Low Power RS-232C Driver and Receiver in CMOS

National Semiconductor
Application Note 438
Gordon W. Campbell

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.

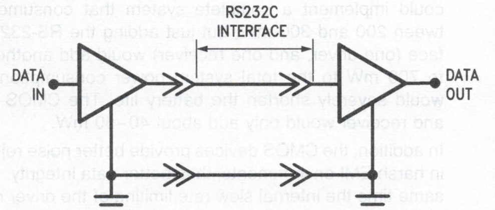

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FIGURE 1. EIA RS-232C Application

THE DRIVER

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction to 500 μA max versus 25 mA can be achieved.

The RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (−5V to −15V). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a ±5V power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/μs. The inherent slew rate of the equivalent bipolar circuit DS14C88/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/μs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

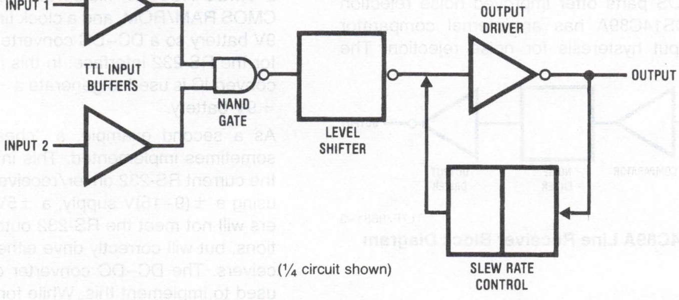

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FIGURE 2. DS14C88 Line Driver Block Diagram

THE RECEIVER

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (900 μA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

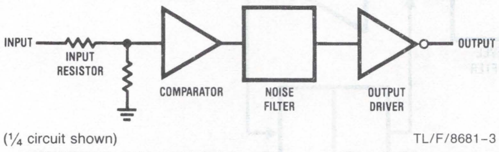
The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "0" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 μs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.



(¼ circuit shown)

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FIGURE 3. DS14C89A Line Receiver Block Diagram

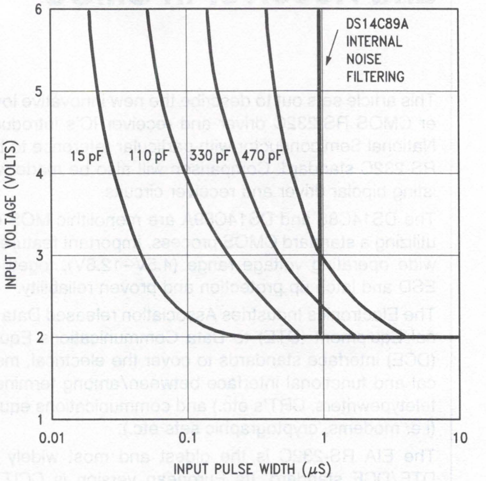

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FIGURE 4

TYPICAL APPLICATIONS

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS μP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate −9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a −9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6*. This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.

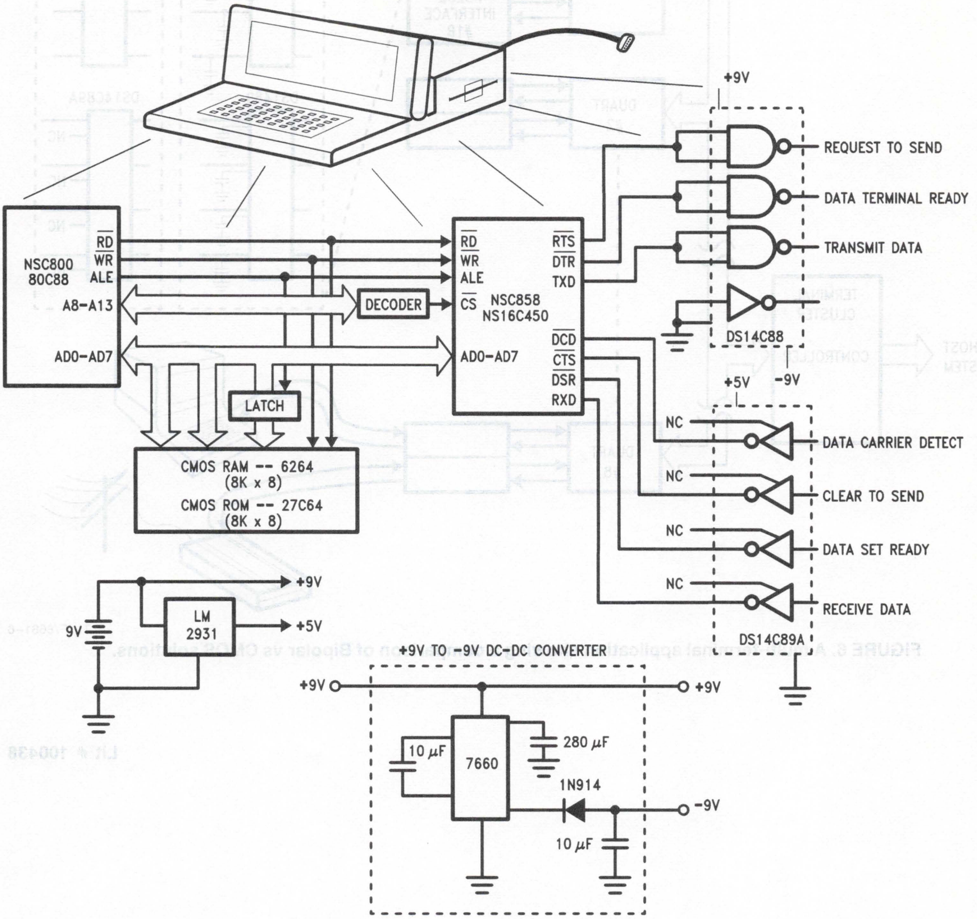
NSC800
80C88
RD
WR
ALE
A8–A13
AD0–AD7
DECODER
LATCH
RD
WR
ALE
CS
NSC858
NS16C450
AD0–AD7
RTS
DTR
TXD
DCD
CTS
DSR
RXD
CMOS RAM -- 6264
(8K x 8)
CMOS ROM -- 27C64
(8K x 8)
+9V
REQUEST TO SEND
DATA TERMINAL READY
TRANSMIT DATA
DS14C88
+5V
-9V
NC
DATA CARRIER DETECT
CLEAR TO SEND
DATA SET READY
RECEIVE DATA
DS14C89A
9V
LM
2931
+9V
+5V
+9V TO -9V DC-DC CONVERTER
+9V
+9V
10 μF
7660
280 μF
1N914
-9V
10 μF

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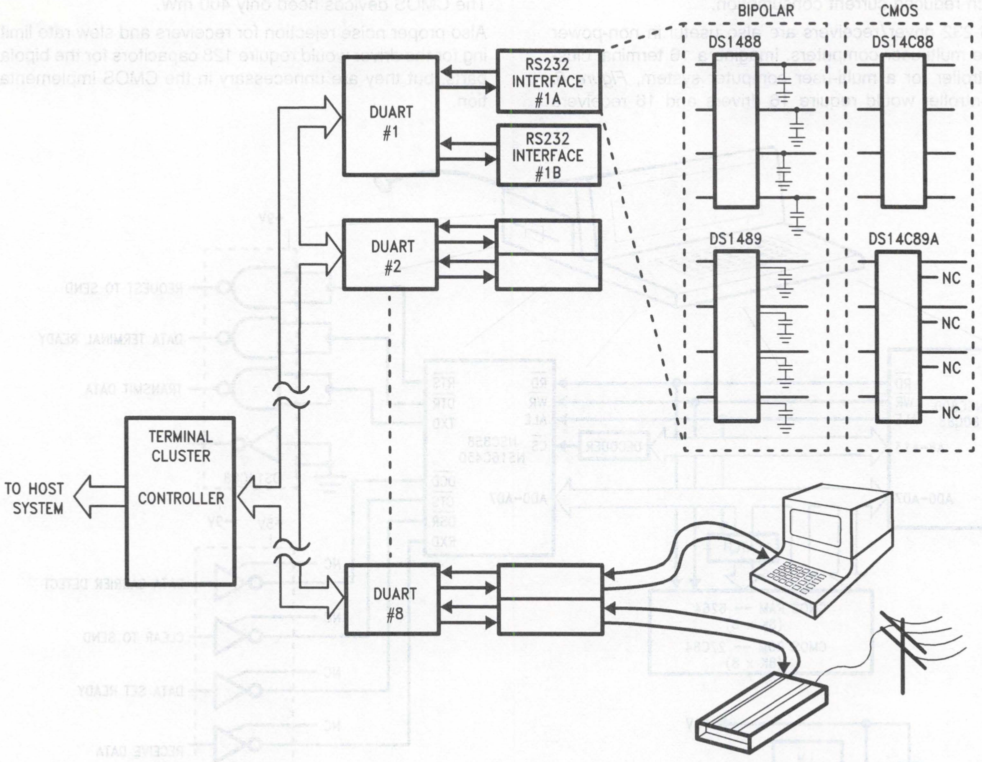
FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART. RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.


BIPOLAR
CMOS
DS1488
DS14C88
RS232 INTERFACE #1A
DUART #1
RS232 INTERFACE #1B
DS1489
DS14C89A
NC
NC
NC
NC
DUART #2
TERMINAL CLUSTER CONTROLLER
TO HOST SYSTEM
DUART #8

TL/F/8681-6

FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

Lit # 100438

High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor
Application Note 457
Toan Tran
Larry Kendall

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS (RS-422) REQUIREMENT

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s. In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 1 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

CABLE LENGTH

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* below is the guideline provided by RS-422 for data modulation rate versus cable length.

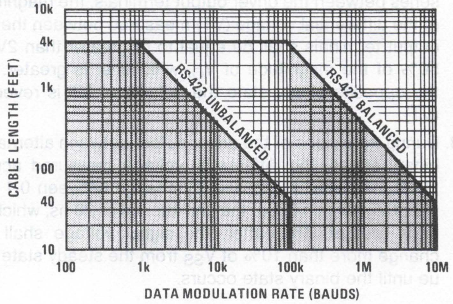


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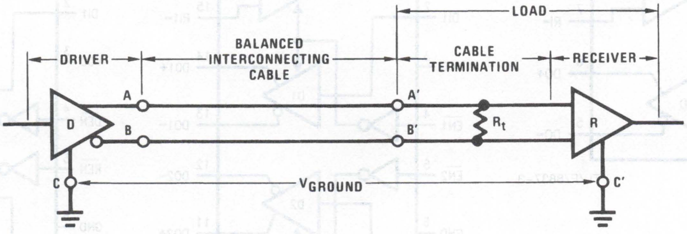
FIGURE 2. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.



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Legend:
R_t = Optional cable transmission resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load Interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1. RS-422 Balanced Digital Interface Circuit

MODULATION RATE

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 CHARACTERISTICS

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 AND DS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control *(Figure 3)*.

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input failsafe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

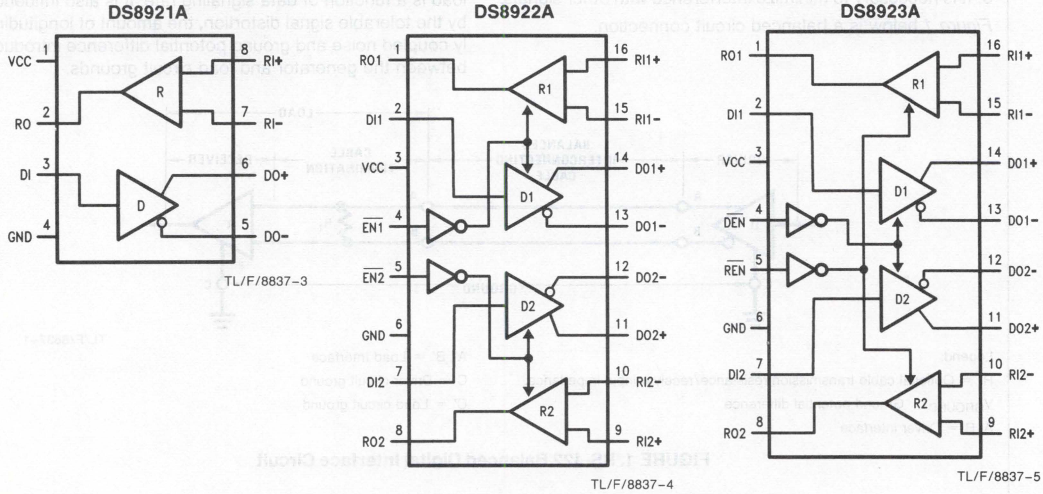
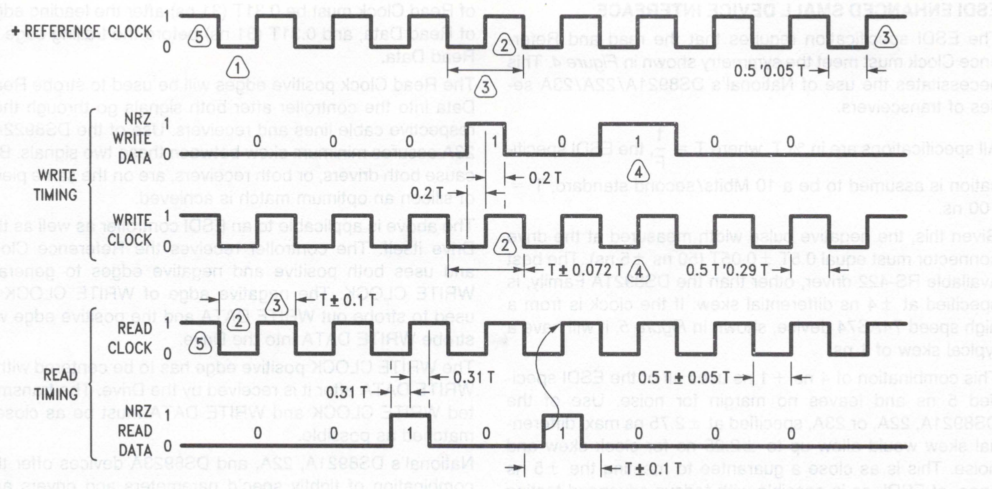


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams


+ REFERENCE CLOCK
1
0
⑤
①
②
③
③
0.5 T 0.05 T
WRITE TIMING
NRZ WRITE DATA
1
0
0
0
0
1
0
1
0
0
0.2 T
0.2 T
④
WRITE CLOCK
1
0
②
T ± 0.072 T
④
0.5 T 0.29 T
READ TIMING
③
T ± 0.1 T
②
READ CLOCK
1
0
⑤
0.31 T
0.31 T
0.5 T ± 0.05 T
NRZ READ DATA
1
0
0
0
1
0
1
0
0
0
T ± 0.1 T

TL/F/8837-6

Note 1. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

Note 2. Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

Note 3. Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

Note 4. The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

Note 5. Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

FIGURE 4. ESDI Timing Diagrams

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\Omega$ $C_L = 50$ pF	105			MHz
T_{PLH}	Preset or clear	Q or Q		3.3		7.5	ns
T_{PHL}				3.5		10.5	ns
T_{PLH}	Clock	Q or Q		3.5		8	ns
T_{PHL}				4.5		9	ns

Note 1: See Section 1 for test waveforms and output load.

FIGURE 5. 1 ns Clock Skew

ESDI ENHANCED SMALL DEVICE INTERFACE

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in *Figure 4.* This necessitates the use of National's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where $T = \frac{1}{F}$, the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T ±0.05T (50 ns ±5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 5*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 4* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

Section 2
Bus Transceivers

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National Semiconductor

Bus Transceivers

A bus is a common communication medium, such as a cable or a printed circuit trace, that is time shared by several elements of a system. Single-ended bus circuits are listed in this section and these may be further categorized into open-collector circuits and TRI-STATE circuits.

When not transmitting, a bus driver should be capable of presenting a high impedance output in order to allow other drivers to freely use the bus. This is achieved by using either an open-collector or TRI-STATE output.

Open-collector drivers may be connected in a wired-or configuration which is very useful for polling and bus arbitration. These devices require pull-up resistors, which can also serve as bus terminators.

TRI-STATE drivers, on the other hand, do not require bus termination for short bus runs on PC boards. In addition, TRI-STATE devices provide improved rise time characteristics with low power dissipation. Hence, they are popular in high-speed microcomputer systems.

A single-ended bus is highly susceptible to noise, including ground noise and crosstalk. For this reason the bus should not be extended beyond the subsystem's enclosure without special care. Line lengths in excess of 10 feet are not recommended without the use of noise reduction techniques, such as slew rate control, high receiver thresholds and noise filtering. Devices such as National Semiconductor's DS3662 and DS3862 Trapezoidal bus transceivers and DS3896 and DS3897 Future Bus transceivers are specifically designed for reducing crosstalk and noise susceptibility on high-speed buses.

FUTUREBUS TRANSCEIVERS

The DS3896 and DS3897 are the first two devices designed for driving high-speed microcomputer backplane buses. Both devices meet the proposed IEEE-P896 Future Bus standard and incorporate low output capacitance (<5 pF) with the ability to drive a bus with a loaded impedance of less than 18Ω. This excellent drive capability is achieved while still maintaining high levels of noise immunity.

POWER UP/DOWN GLITCH FREE PROTECTION

Powering a device up or down, or simply connecting or disconnecting a device from an active bus, has frequently presented the design engineer with the problem of invalid data glitches being transmitted onto the bus. National Semiconductor is the industry leader in offering bus transceivers incorporating glitch-free power up/down protection. For more detailed information on National Semiconductor's line of bus transceivers, refer to the following Selection Guide and application notes within this section.

BUS CIRCUITS

Data bus circuits are not transmission line circuits in the normal interpretation where the transmission line is electrically long (1/4 wavelength) with respect to the baud rate. Like unbalanced transmission lines, the data transmission is susceptible to common-mode noise, such as ground IR noise and induced reactive noise from crosstalk. A bus is a communications method where many elements of a system time share the same signal (address or data) bus. A bus shouldn't extend out of its subsystem's electronic enclosure without special care. Line length in excess of 10 feet is not recommended without slew rate control. Cables should be in the form of twisted pair or flat cable where a signal wire is alternated with a ground wire.

OPEN-COLLECTOR BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver		Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	Military −55°C to +125°C			Propagation Delay (ns)	V_{OL} (V)/ I_{OL} (mA)	Propagation Delay (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (V)		
DM8131	DM7131	1	Receiver			30	0.95/50	2/50	0.65	6-Bit Bus Comparator	Logic
DM8136	DM7136	1	Receiver			30	0.95/50	2/50	0.65	6-Bit Bus Comparator	Logic
DS26S10	DS26S10M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100			2-24
DS26S11	DS26S11M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100		Input to Bus is Non-Inverting	2-24
DS3662		4	Transceiver	30	0.9/100	40	1.50/400	1.9/100		Trapezoidal Transceiver	2-29
DS3862		8	Transceiver							Trapezoidal Transceiver	2-52
DS3890		8	Driver	15						Futurebus Driver	2-58
DS3892		8	Receiver			18				Futurebus Receiver	2-58
DS3893A		4	Transceiver	7		8				TURBOTRANSCEIVER	2-64
DS3896		8	Transceiver							Futurebus Transceiver	2-69
DS3897		4	Transceiver							Futurebus Transceiver	2-69
DS3898		8	Repeator	30						Futurebus Repeator	2-58
DS75450		2	Driver	20	0.7/300					AND Separate Output Transistors	3-41
DS75451	DS55451	2	Driver	18	0.7/300					AND	3-41
DS75452	DS55452	2	Driver	26	0.7/300					NAND	3-41
DS75453	DS55453	2	Driver	18	0.7/300					OR	3-41
DS75454	DS55454	2	Driver	27	0.7/300					NOR	3-41
DS8640	DS7640	4	Receiver			23	1.2/−50	1.8/50		Quad NOR Receiver	2-96
DS8641	DS7641	4	Transceiver	30	0.7/50	30	1.2/−100	1.8/100			2-98
DS8836	DS7836	4	Receiver			20	1.05/−50	2.65/50	1	Quad NOR Receiver	2-109
DS8837	DS7837	6	Receiver			20	1.05/−50	2.65/50	1		2-111
DS8838	DS7838	4	Transceiver	25	0.8/50	30	1.05/−100	2.65/100	1		2-114

TRI-STATE® BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver			Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	**Military −55°C to +125°C**			**Propagation Delay Typ (ns)**	**V_{OL} (V)/ I_{OL} (mA)**	**V_{OH} (V)/ I_{OH} (mA)**	**Propagation Delay Typ (ns)**	**V_{IL} (V)/ I_{IL} (μA)**	**V_{IH} (V)/ I_{IH} (μA)**	**Hysteresis (mV)**		
DM74S240	DM54S240	4 or 8	Transceiver	4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Non-Inverting	Logic
DM74S241	DM54S241	4 or 8	Transceiver	6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Inverting	Logic
DM74S940	DM54S940	8	Transceiver	4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Non-Inverting	Logic
DM74S941	DM54S941	8	Transceiver	6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Inverting	Logic
DP8212	DP8212M	8	Driver	20	0.45/15	3.6/−1					8080 MPU Data Latch and Service Request f/f	6-5
DP8216	DP8216M	4	Transceiver	20	0.6/55	3.6/−1	15	0.95/−250	2/10		8080 MPU Non-Inverting	6-13
DP8226	DP8226M	4	Transceiver	16	0.6/50	3.6/−1	15	0.95/−250	2/10		8080 MPU Inverting	6-13
DP8228	DP8228M	8	Transceiver	30	0.45/10	2.4/−1	20	0.8/−250	2/20		8080 MPU System Bus Controller and Bus Driver	6-24
DP8238	DP8238M	8	Transceiver	30	0.45/10	2.4/−1	20	0.8/−250	2/20		8080 MPU System Bus Controller and Bus Driver	6-24
DP8303A		8	Transceiver	10	0.5/50	3.6/−5	10	0.8/−250	2/80		Bidirectional Inverting	2-6
DP8304B	DP7304B	8	Transceiver	10	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidirectional Non-Inverting IEEE 488	2-11
DP8307A		8	Transceiver	10	0.5/50	3.6/−5	10	0.8/−250	2/80		Bidirectional Inverting	2-16
DP8308	DP7308	8	Transceiver	11	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidirectional Non-Inverting	2-20
DS3647		4	Transceiver	8	0.5/50	2.4/−5	7	0.8/−500	2/100		Quad Bidirectional I/O Register	5-28
DS3667		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400		2-47
DS75160A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-88
DS75161A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-88
DS75162A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-88
DS8T26A	DS8T26AM	4	Transceiver	14	0.5/48	2.4/−10	14	0.85/−200	2/20		Inverting	2-117
DS8T28	DS8T28M	4	Transceiver	17	0.5/48	2.4/−10	17	0.85/−200	2/20		Non-Inverting	2-117
DS8833	DS7833	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Non-Inverting TRI-STATE Receiver	2-101
DS8834	DS7834	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting	2-105
DS8835	DS7835	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting TRI-STATE Receiver	2-101
DS8839	DS7839	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Non-Inverting	2-105

Note: Unless otherwise specified, bus circuits listed above are TTL compatible and use 5V supplies.

National Semiconductor

DP8303A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

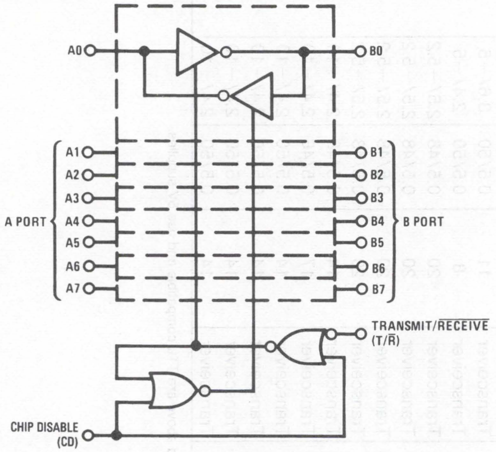
This family of high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

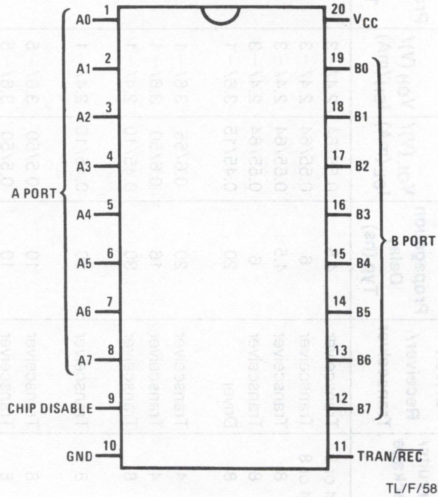
- 8-bit directional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams


A0
B0
A1
A2
A3
A4
A5
A6
A7
A PORT
B1
B2
B3
B4
B5
B6
B7
B PORT
TRANSMIT/RECEIVE (T/R)
CHIP DISABLE (CD)

TL/F/5856-1

Dual-In-Line Package


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A PORT
CHIP DISABLE 9
GND 10
20 VCC
19 B0
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
B PORT
11 TRAN/REC

TL/F/5856-2

Top View

Order Number DP8303AJ or DP8303AN

See NS Package Number J20A, N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	**Transmit/$\overline{\text{Receive}}$**	**A Port**	**B Port**
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 4 seconds)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8303A	4.75	5.25	V
Temperature (T_A)			
DP8303A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, $T/\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, $T/\overline{R}$ = 2.0V				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = $T/\overline{R}$ = V_{IL} V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} − 0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = $T/\overline{R}$ = V_{IL} V_{IL} = 0.5V	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, $T/\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, $T/\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, $T/\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	µA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	µA
			V_{IN} = 4.0V			80	µA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, $T/\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, $T/\overline{R}$ = V_{IL}				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, $T/\overline{R}$ = 2.0V V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} −0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, $T/\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, $T/\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, $T/\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, $T/\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	µA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	µA
			V_{IN} = 0.4V			+200	µA

DC Electrical Charcateristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS CD, $T/\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, $V_{IH} = 5.25V$				1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$	$T/\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12$ mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN}, V_{CC} = Max			70	100	mA
		CD = 0.4V, $V_{INA} = T/\overline{R} = 2V$, V_{CC} = Max			100	150	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, $T/\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, $T/\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, $T/\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 7	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, $T/\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	20 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PLZB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 16	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5kΩ, C4 = 45 pF		22 14	35 25	ns ns

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		23	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		23	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (*Figure B*) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 0, R3 = 300Ω, C2 = 5 pF		27	35	ns

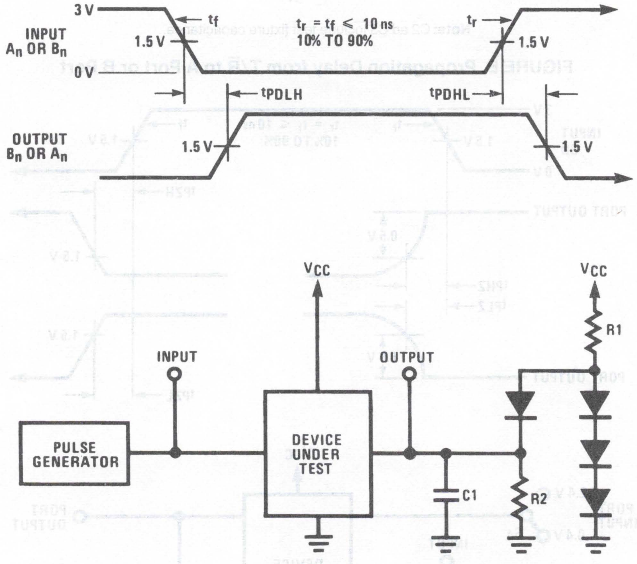
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



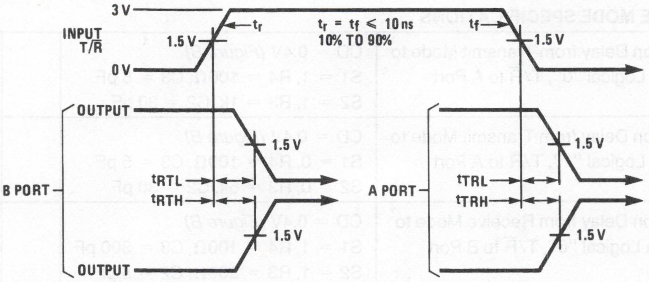
TL/F/5856-3

TL/F/5856-4

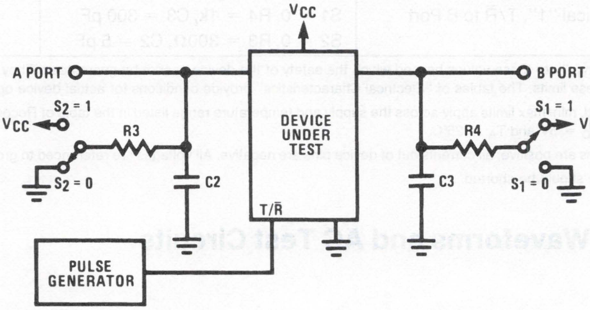
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)


3 V
INPUT T/R̄
1.5 V
0 V
tr
tr = tf ≤ 10 ns
10% TO 90%
tf
1.5 V
OUTPUT
1.5 V
B PORT
tRTL
tRTH
1.5 V
OUTPUT
A PORT
1.5 V
tTRL
tTRH
1.5 V

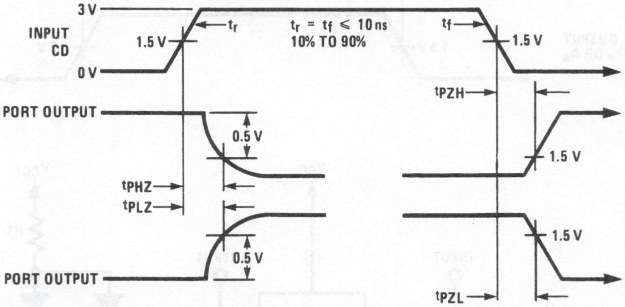
TL/F/5856-5


VCC
A PORT
B PORT
S2 = 1
VCC
R3
S2 = 0
C2
DEVICE UNDER TEST
T/R̄
S1 = 1
VCC
R4
C3
S1 = 0
PULSE GENERATOR

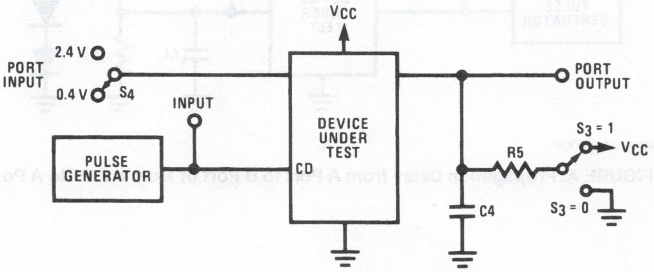
TL/F/5856-6

Note: C2 ad C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/R̄ to A Port or B Port


3 V
INPUT CD
1.5 V
0 V
tr
tr = tf ≤ 10 ns
10% TO 90%
tf
1.5 V
PORT OUTPUT
0.5 V
tPHZ
tPLZ
0.5 V
PORT OUTPUT
tPZH
1.5 V
1.5 V
tPZL

TL/F/5856-7


VCC
2.4 V
PORT INPUT
0.4 V
S4
INPUT
PULSE GENERATOR
DEVICE UNDER TEST
CD
PORT OUTPUT
S3 = 1
R5
VCC
C4
S3 = 0

TL/F/5856-8

Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

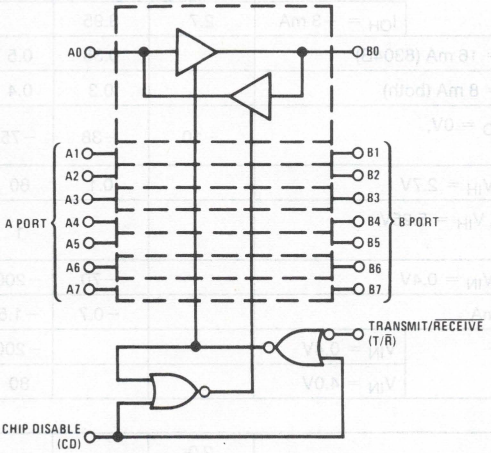
The DP73048B/DP8304B are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/Receive and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

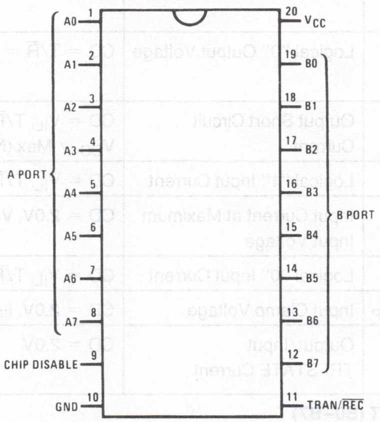
Logic and Connection Diagrams



A0
B0
A1
A2
A3
A PORT
A4
A5
A6
A7
B1
B2
B3
B4
B PORT
B5
B6
B7
TRANSMIT/RECEIVE
(T/R)
CHIP DISABLE
(CD)

TL/F/8793-1

Dual-In-Line Package



A0
1
A1
2
A2
3
A3
4
A PORT
A4
5
A5
6
A6
7
A7
8
CHIP DISABLE
9
GND
10
20
VCC
19
B0
18
B1
17
B2
16
B3
B PORT
15
B4
14
B5
13
B6
12
B7
11
TRAN/REC

TL/F/8793-2

Top View

Order Number DP7304BJ, DP8304BJ,
DP8304BN or DP8304BWM
See NS Package Number J20A, N20A or M20B

Logic Table

Inputs		Resulting Conditions	
Chip Disable	**Transmit/$\overline{\text{Receive}}$**	**A Port**	**B Port**
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$CD = V_{IL}$, $T/\overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$CD = V_{IL}$, $T/\overline{R} = 2.0V$	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$CD = T/\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8304B)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$, $V_O = 0V$, $V_{CC} = $ Max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$CD = V_{IL}$, $T/\overline{R} = 2.0V$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$CD = 2.0V$, $V_{CC} = $ Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$CD = V_{IL}$, $T/\overline{R} = 2.0V$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$CD = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$CD = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$CD = V_{IL}$, $T/\overline{R} = V_{IL}$	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	$CD = V_{IL}$, $T/\overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$CD = V_{IL}$, $T/\overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$CD = V_{IL}$, $T/\overline{R} = 2.0V$, $V_O = 0V$, $V_{CC} = $ Max (Note 4)		−25	−50	−150	mA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
B PORT (B0–B7) (Continued)							
I_{IH}	Logical "1" Input Current	CD = V_{IL}, $T/\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, $T/\overline{R} = V_{IL}$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA
CONTROL INPUTS CD, $T/\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8304B			0.8	V
			DP7304B			0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, $V_{IH} = 5.25V$				1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$	$T/\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12$ mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, $V_{IN} = 0.4V$, V_{CC} = Max			70	100	mA
		CD = $V_{INA} = 0.4V$, $T/\overline{R} = 2V$, V_{CC} = Max			90	140	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, $T/\overline{R} = 0.4V$ (*Figure A*) R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, $T/\overline{R} = 0.4V$ (*Figure A*) R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R} = 0.4V$ (*Figure C*) S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R} = 0.4V$ (*Figure C*) S3 = 0, R5 = 1k, CR = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R} = 0.4V$ (*Figure C*) S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R} = 0.4V$ (*Figure C*) S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, $T/\overline{R} = 2.4V$ (*Figure A*) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 18 11	 23 18	 ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, $T/\overline{R} = 2.4V$ (*Figure A*) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 16 11	 23 18	 ns ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATIONS (Continued)						
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 16	40 22	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		26 14	35 22	ns ns
TRANSMIT/$\overline{\text{RECEIVE}}$ MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V, *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTH}	Propagation Delay from $\overline{\text{Receive}}$ Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		28	40	ns

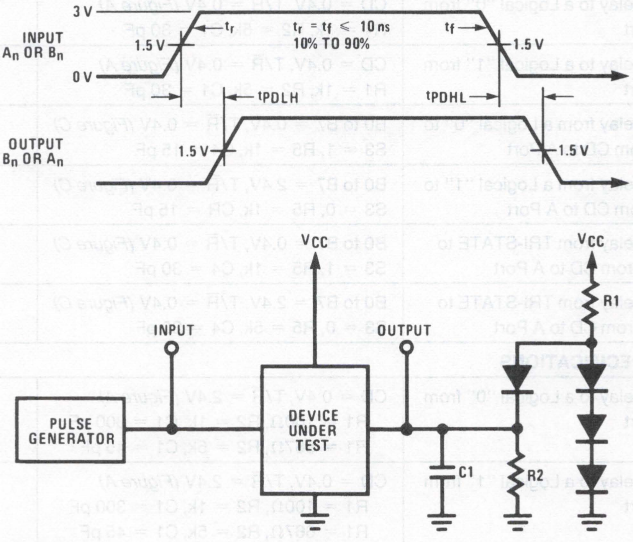
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

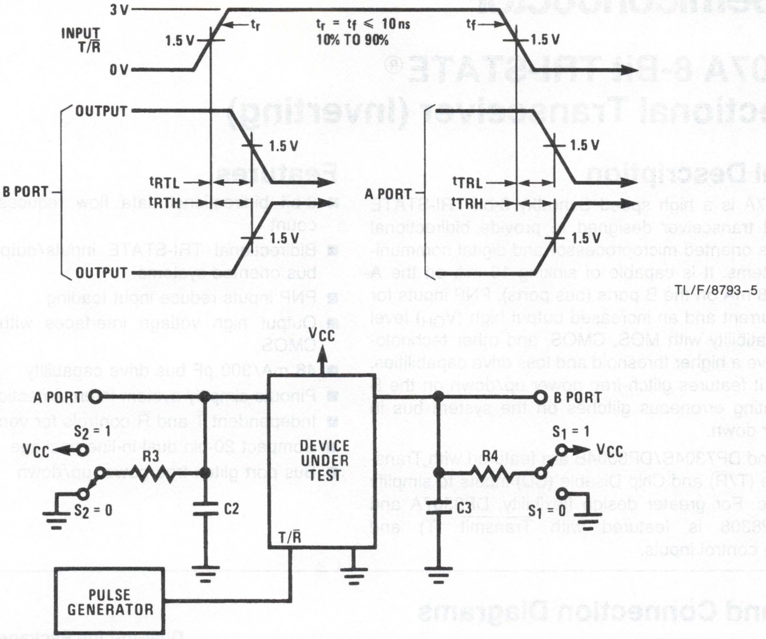
Switching Time Waveforms and AC Test Circuits



Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)

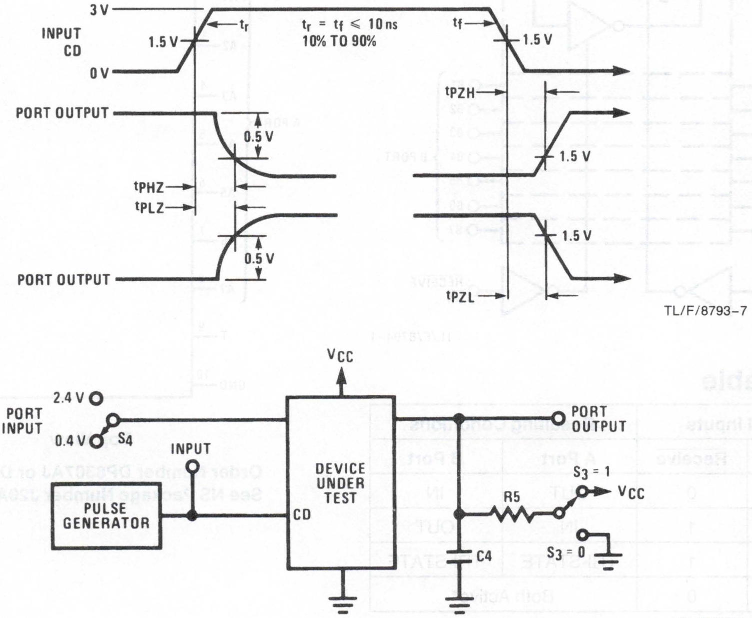

3 V
INPUT T/R̄
1.5 V
0 V
t_r
$t_r = t_f \leq 10$ ns
10% TO 90%
t_f
1.5 V
OUTPUT
B PORT
OUTPUT
1.5 V
tRTL
tRTH
1.5 V
A PORT
1.5 V
tTRL
tTRH
1.5 V
VCC
A PORT
B PORT
S2 = 1
VCC
R3
S2 = 0
C2
DEVICE UNDER TEST
T/R̄
S1 = 1
VCC
R4
C3
S1 = 0
PULSE GENERATOR

TL/F/8793-5

TL/F/8793-6

Note: C2 and C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/R̄ to A Port or B Port


3 V
INPUT CD
1.5 V
0 V
t_r
$t_r = t_f \leq 10$ ns
10% TO 90%
t_f
1.5 V
PORT OUTPUT
0.5 V
tPHZ
tPLZ
0.5 V
PORT OUTPUT
tPZH
1.5 V
1.5 V
tPZL
VCC
2.4 V
PORT INPUT
0.4 V
S4
INPUT
PULSE GENERATOR
CD
DEVICE UNDER TEST
PORT OUTPUT
S3 = 1
VCC
R5
C4
S3 = 0

TL/F/8793-7

TL/F/8793-8

Note: C4 includes test fixture capacitance.

Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor

DP8307A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

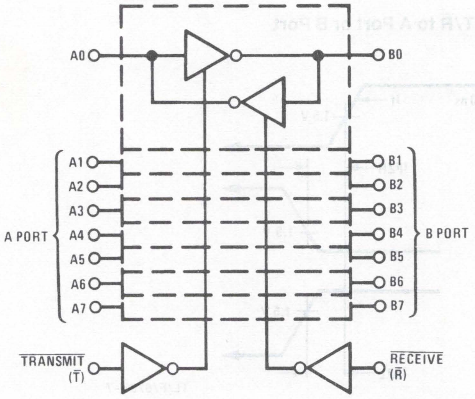
The DP8307A is a high speed Schottky 8-bit TRI-STATE bidirectional transceiver designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, it features glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 is featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

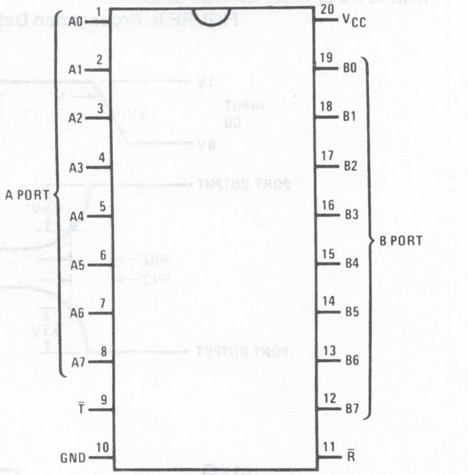
- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high votlage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{\text{T}}$ and $\overline{\text{R}}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



TL/F/8794-1

Dual-In-Line Package



TL/F/8794-2

Top View

Order Number DP8307AJ or DP8307AN
See NS Package Number J20A or N20A

Logic Table

Control Inputs		Resulting Conditions	
Transmit	**Receive**	**A Port**	**B Port**
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C
Storage Temperature	−65°C to +150°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$ $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V,$ $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA		0.35	0.5	V
			$I_{OL} = 8$ mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_O = 0V,$ $V_{CC} = $ Max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V, V_{CC} = $ Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$ $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_O = 0V,$ $V_{CC} = $ Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V, V_{CC} = $ Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$			0.5	20	µA
I_I	Maximum Input Current	V_{CC} = Max, $V_{IH} = 5.25V$				1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12$ mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T} = \overline{R} = 2.0V$, $V_{IN} = 2.0V$, V_{CC} = Max			70	100	mA
		$\overline{T} = 0.4V$, $V_{INA} = \overline{R} = 2V$, V_{CC} = Max			100	150	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T} = 2.4V$, $\overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T} = 2.4V$, $\overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T} = 0.4V$, $\overline{R} = 2.4V$ *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 8	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T} = 0.4V$, $\overline{R} = 2.4V$ *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	23 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 18	40 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		25 16	35 25	ns ns

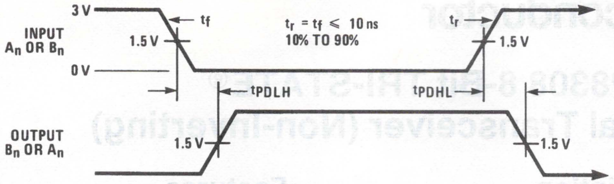
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for $V_{CC} = 5V$ and $T_A = 25°C$.

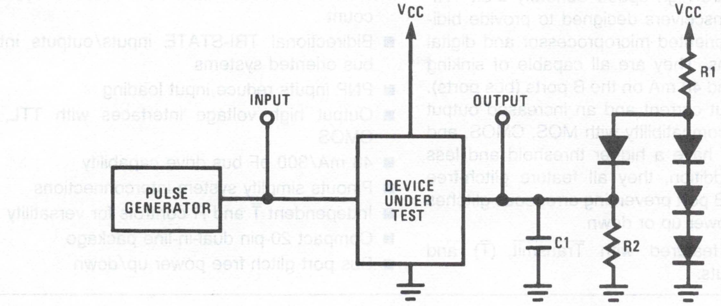
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits


3 V
INPUT
A_n OR B_n
1.5 V
0 V
t_f
$t_r = t_f \leq 10$ ns
10% TO 90%
t_r
1.5 V
t_{PDLH}
t_{PDHL}
OUTPUT
B_n OR A_n
1.5 V
1.5 V

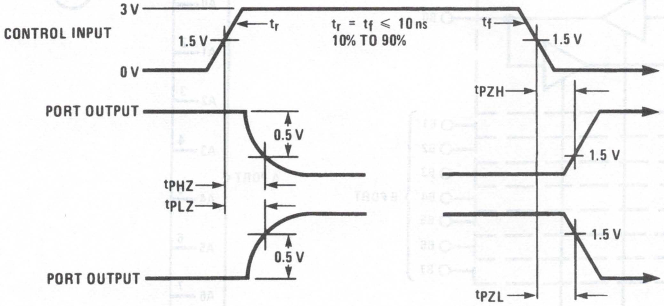
TL/F/8794-3


V_{CC}
V_{CC}
INPUT
OUTPUT
R1
PULSE GENERATOR
DEVICE UNDER TEST
C1
R2

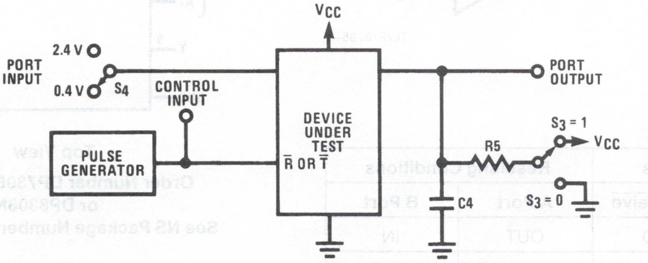
TL/F/8794-4

Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port


3 V
CONTROL INPUT
1.5 V
0 V
t_r
$t_r = t_f \leq 10$ ns
10% TO 90%
t_f
1.5 V
t_{PZH}
PORT OUTPUT
0.5 V
1.5 V
t_{PHZ}
t_{PLZ}
1.5 V
0.5 V
PORT OUTPUT
t_{PZL}

TL/F/8794-5


V_{CC}
2.4 V
PORT INPUT
0.4 V
S_4
CONTROL INPUT
PORT OUTPUT
DEVICE UNDER TEST
$\overline{R}$ OR $\overline{T}$
PULSE GENERATOR
$S_3 = 1$
V_{CC}
R5
$S_3 = 0$
C4

TL/F/8794-6

Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from R̄ to A Port and T̄ to B Port

National Semiconductor

DP7308/DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

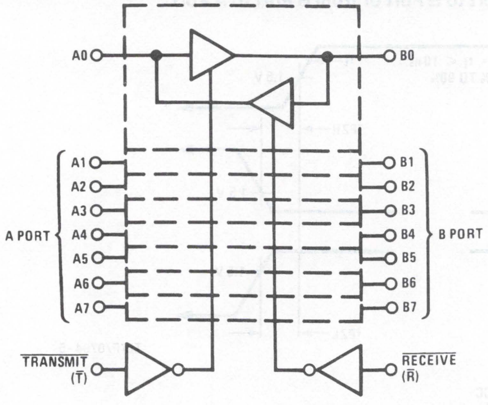
The DP7308/DP8308 are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{T}$) and $\overline{\text{Receive}}$ ($\overline{R}$) control inputs.

Features

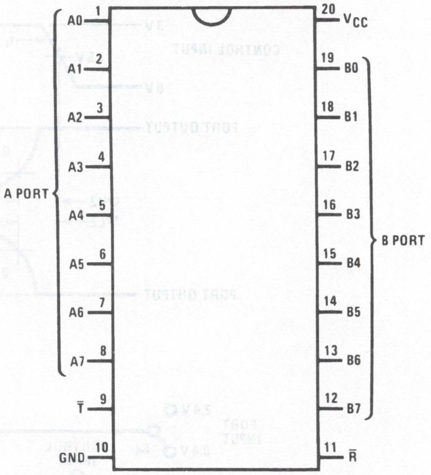
- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams


A0
B0
A1
A2
A3
A4
A5
A6
A7
A PORT
B1
B2
B3
B4
B5
B6
B7
B PORT
TRANSMIT ($\overline{T}$)
RECEIVE ($\overline{R}$)

TL/F/8795-1

Dual-In-Line Package


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A PORT
$\overline{T}$ 9
GND 10
20 V_{CC}
19 B0
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
B PORT
11 $\overline{R}$

TL/F/8795-2

Top View

Order Number DP7308J, DP8308J or DP8308N

See NS Package Number J20A or N20A

Logic Table

Control Inputs		Resulting Conditions	
Transmit	**Receive**	**A Port**	**B Port**
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7308	4.5	5.5	V
DP8308	4.75	5.25	V
Temperature (T_A)			
DP7308	−55	+125	°C
DP8308	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = 3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8308)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_O = 0V$ V_{CC} = Max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IH} = 2.7V$			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V, V_{CC}$ = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IN} = 0.4V$			−70	−200	µA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	µA
			$V_{IN} = 4.0V$			80	µA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_O = 0V,$ V_{CC} = Max (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IH} = 2.7V$			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V, V_{CC}$ = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IN} = 0.4V$			−70	−200	µA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	µA
			$V_{IN} = 4.0V$			+200	µA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8308			0.8	V
			DP7308			0.7	V
I_{IH}	Logical "1" Input Current	$V_{IH} = 2.7V$			0.5	20	µA
I_I	Maximum Input Current	$V_{CC} = Max, V_{IH} = 5.25V$				1.0	mA
I_{IL}	Logical "0" Input Current	$V_{IL} = 0.4V$	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12\ mA$			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T} = \overline{R} = 2.0V, V_{IN} = 0.4V, V_{CC} = Max$			70	100	mA
		$\overline{T} = V_{INA} = 0.4V, \overline{R} = 2V, V_{CC} = Max$			90	140	mA

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T} = 2.4V, \overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T} = 2.4V, \overline{R} = 0.4V$ *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		24	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T} = 2.4V$ *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		21	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T} = 0.4V, \overline{R} = 2.4V$ *(Figure A)*				
		R1 = 100Ω, R2 = 1k, C1 = 300 pF		18	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45 pF		11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T} = 0.4V, \overline{R} = 2.4V$ *(Figure A)*				
		R1 = 100Ω, R2 = 1k, C1 = 300 pF		16	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45 pF		11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R} = 2.4V$ *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R} = 2.4V$ *(Figure B)*				
		S3 = 1, R5 = 100Ω, C4 = 300 pF		25	35	ns
		S3 = 1, R5 = 667Ω, C4 = 45 pF		17	25	ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R} = 2.4V$ *(Figure B)*				
		S3 = 0, R5 = 1k, C4 300 pF		24	35	ns
		S3 = 0, R5 = 5k, C4 = 45 pF		17	25	ns

AC Electrical Characteristics (Continued)

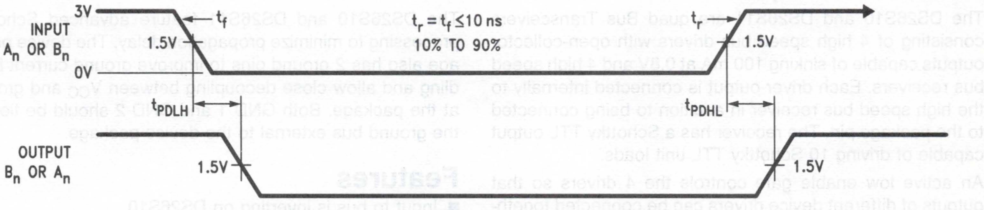
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

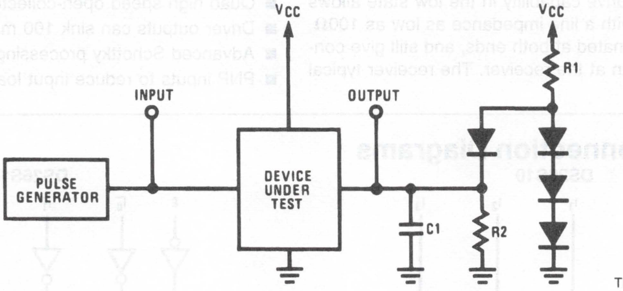
Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



3V
INPUT
A_n OR B_n
0V
1.5V
t_f
$t_r = t_f \leq 10$ ns
10% TO 90%
t_r
1.5V
t_{PDLH}
t_{PDHL}
OUTPUT
B_n OR A_n
1.5V
1.5V

TL/F/8795–3

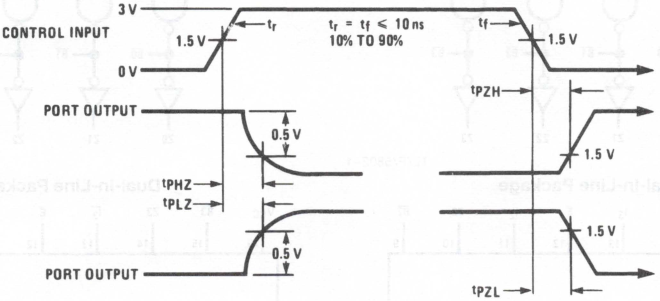


V_{CC}
V_{CC}
R1
INPUT
OUTPUT
PULSE GENERATOR
DEVICE UNDER TEST
C1
R2

TL/F/8795–4

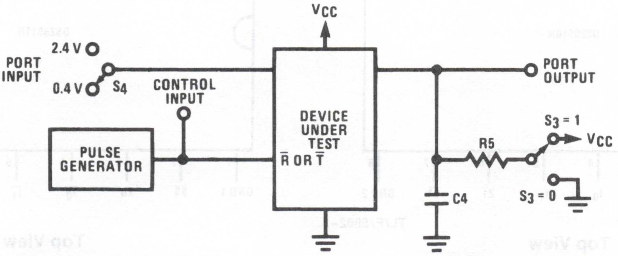
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



3 V
CONTROL INPUT
1.5 V
0 V
t_r
$t_r = t_f \leq 10$ ns
10% TO 90%
t_f
1.5 V
PORT OUTPUT
0.5 V
t_{PZH}
1.5 V
t_{PHZ}
t_{PLZ}
1.5 V
0.5 V
PORT OUTPUT
t_{PZL}

TL/F/8795–5



V_{CC}
PORT INPUT
2.4 V
0.4 V
S_4
CONTROL INPUT
PORT OUTPUT
PULSE GENERATOR
DEVICE UNDER TEST
$\overline{R}$ OR $\overline{T}$
$S_3 = 1$
V_{CC}
R5
C4
$S_3 = 0$

TL/F/8795–6

Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor

DS26S10C/DS26S10M/DS26S11C/DS26S11M Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

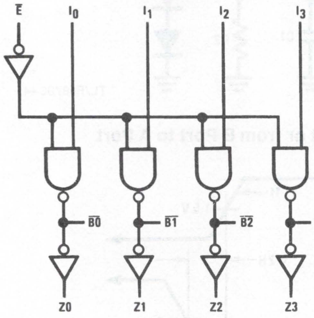
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic and Connection Diagrams

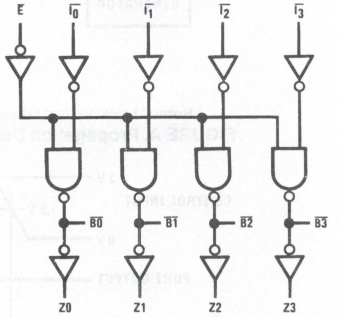
DS26S10



$\overline{E}$
I_0
I_1
I_2
I_3
$\overline{B0}$
$\overline{B1}$
$\overline{B2}$
$\overline{B3}$
Z0
Z1
Z2
Z3

TL/F/5802-1

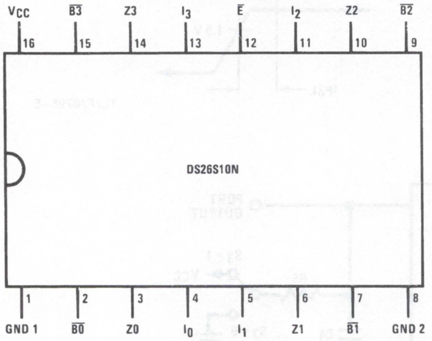
DS26S11



E
$\overline{I_0}$
$\overline{I_1}$
$\overline{I_2}$
$\overline{I_3}$
$\overline{B0}$
$\overline{B1}$
$\overline{B2}$
$\overline{B3}$
Z0
Z1
Z2
Z3

TL/F/5802-2

Dual-In-Line Package



V_{CC} 16
$\overline{B3}$ 15
Z3 14
I_3 13
$\overline{E}$ 12
I_2 11
Z2 10
$\overline{B2}$ 9
DS26S10N
1 GND 1
2 $\overline{B0}$
3 Z0
4 I_0
5 I_1
6 Z1
7 $\overline{B1}$
8 GND 2

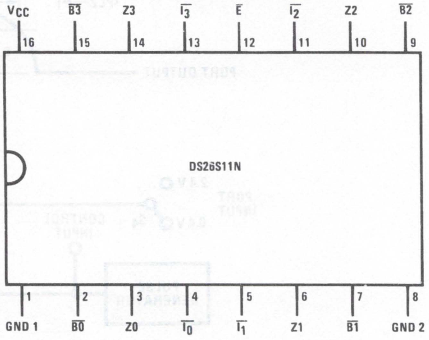
TL/F/5802-3

Top View

Order Number DS26S10CJ, DS26S10MJ or DS26S10CN

See NS Package Number J16A or N16A

Dual-In-Line Package



V_{CC} 16
$\overline{B3}$ 15
Z3 14
$\overline{I_3}$ 13
E 12
$\overline{I_2}$ 11
Z2 10
$\overline{B2}$ 9
DS26S11N
1 GND 1
2 $\overline{B0}$
3 Z0
4 $\overline{I_0}$
5 $\overline{I_1}$
6 Z1
7 $\overline{B1}$
8 GND 2

TL/F/5802-4

Top View

Order Number DS26S11CJ, DS26S11MJ or DS26S11CN

See NS Package Number J16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA

Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS26S10C, DS26S11C	4.75	5.25	V
DS26S10M, DS26S11M	4.5	5.5	V
Temperature (T_A)			
DS26S10C, DS26S11C	0	+70	°C
DS26S10M, DS26S11M	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

Symbol	Parameter	Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	µA
			Data			30	µA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	µA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = GND	DS26S10		45	70	mA
			DS26S11			80	mA

Bus Input/Output Characteristics

Symbol	Parameter	Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max	Military		2.4	2.0		V
			Commercial		2.25	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min	Military			2.0	1.6	V
			Commercial			2.0	1.75	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5V$)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	$R_B = 50\Omega$, C_B = 50 pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	Enable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	$R_B = 50\Omega$, $R_L = 280\Omega$, C_B = 50 pF (Note 1), C_L = 15 pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	$R_B = 50\Omega$, C_B = 50 pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance.

Truth Tables

DS26S10

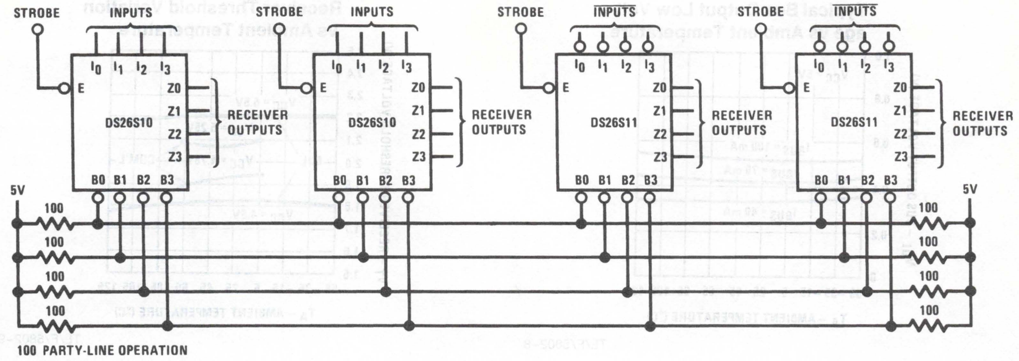
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

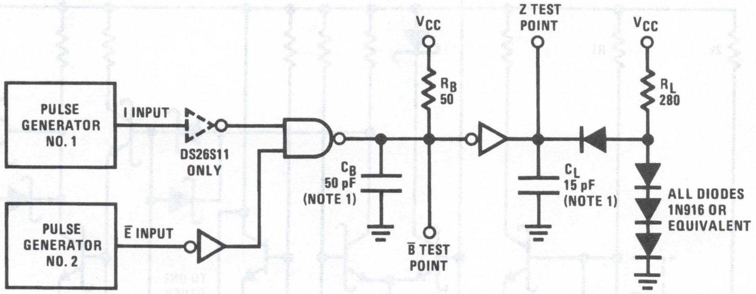
H = High voltage level
L = Low voltage level
X = Don't care
Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application


STROBE
INPUTS
I0 I1 I2 I3
E
Z0
Z1
Z2
Z3
DS26S10
RECEIVER OUTPUTS
STROBE
INPUTS
DS26S10
RECEIVER OUTPUTS
STROBE
INPUTS
DS26S11
RECEIVER OUTPUTS
STROBE
INPUTS
DS26S11
RECEIVER OUTPUTS
B0 B1 B2 B3
5V
100
100
100
100
5V
100
100
100
100
100 PARTY-LINE OPERATION

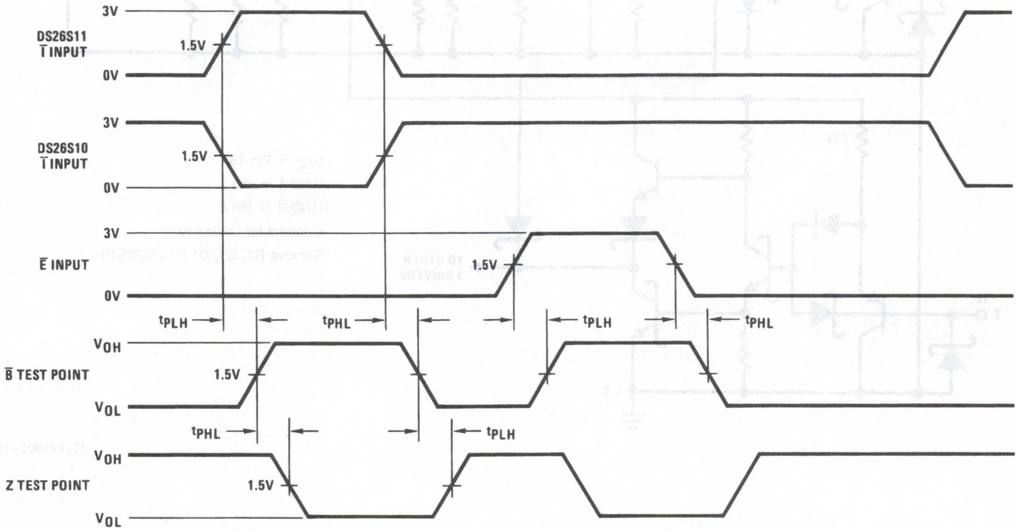
TL/F/5802-5

AC Test Circuit and Switching Time Waveforms


PULSE GENERATOR NO. 1
I INPUT
DS26S11 ONLY
PULSE GENERATOR NO. 2
Ē INPUT
VCC
RB 50
CB 50 pF (NOTE 1)
B̄ TEST POINT
Z TEST POINT
VCC
RL 280
CL 15 pF (NOTE 1)
ALL DIODES 1N916 OR EQUIVALENT

TL/F/5802-6

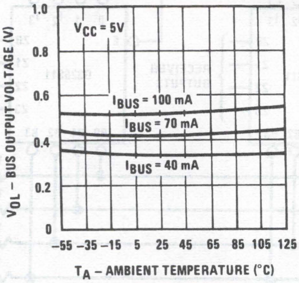
Note 1: Includes probe and jig capacitance.


3V
DS26S11 Ī INPUT
1.5V
0V
3V
DS26S10 Ī INPUT
1.5V
0V
3V
Ē INPUT
1.5V
0V
tPLH
tPHL
tPLH
tPHL
VOH
B̄ TEST POINT
1.5V
VOL
tPHL
tPLH
VOH
Z TEST POINT
1.5V
VOL

TL/F/5802-7

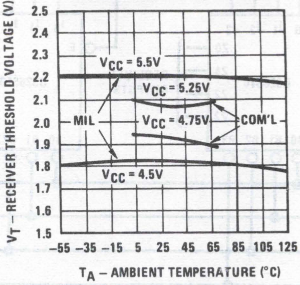
Typical Performance Characteristics

Typical Bus Output Low Voltage vs Ambient Temperature



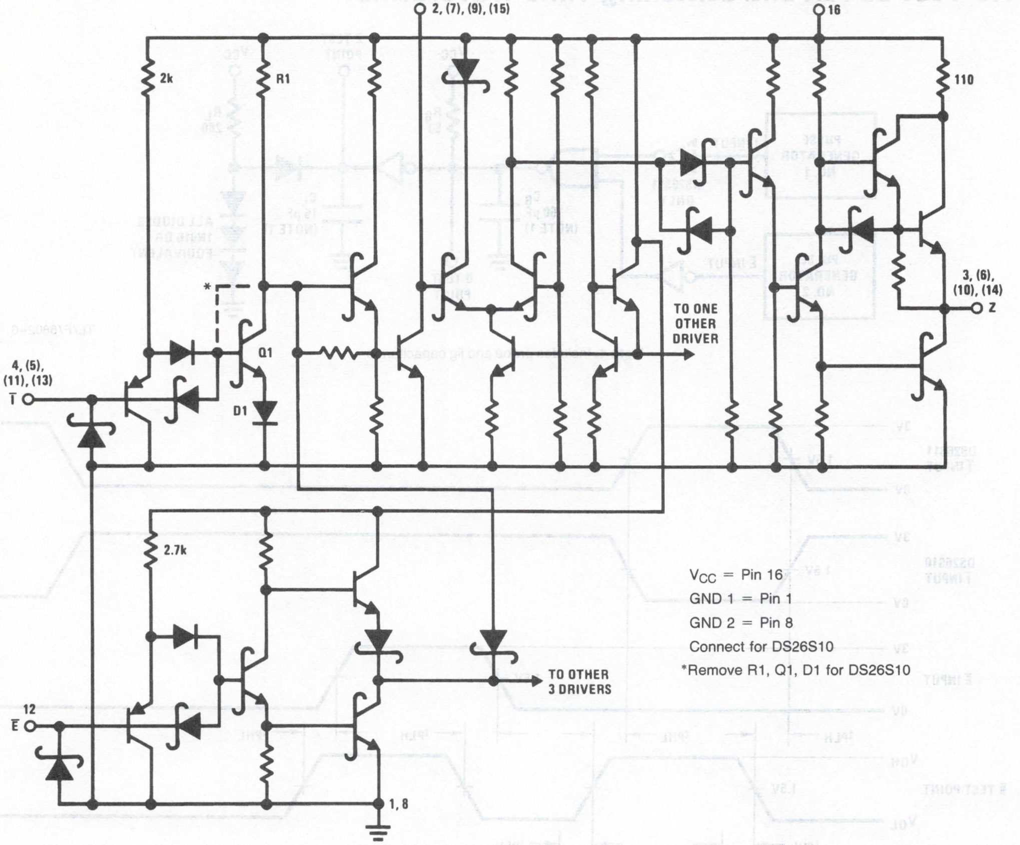
TL/F/5802-8

Receiver Threshold Variation vs Ambient Temperature



TL/F/5802-9

Schematic Diagram


B̄
2, (7), (9), (15)
V_{CC}
16
2k
R1
110
*
Q1
D1
4, (5), (11), (13)
T̄
3, (6), (10), (14)
Z
TO ONE OTHER DRIVER
2.7k
12
Ē
TO OTHER 3 DRIVERS
1, 8

V_{CC} = Pin 16
GND 1 = Pin 1
GND 2 = Pin 8
Connect for DS26S10
*Remove R1, Q1, D1 for DS26S10

TL/F/5802-10

National Semiconductor

DS3662 Quad High Speed Trapezoidal™ Bus Transceiver

General Description

The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

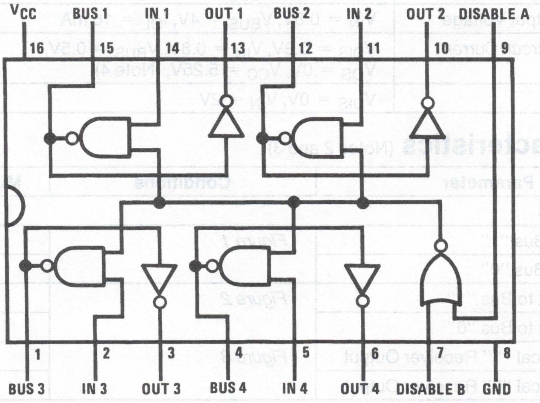
The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- 15 μA typical bus termination current with normal V_{CC} or with $V_{CC} = 0V$
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

Block and Connection Diagram

Dual-In-Line Package



TL/F/5803-1

Top View

Order Number DS3662J or DS3662N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature Range (T_A)	0	70	°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$			1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$		−1	−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA		−0.8	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT						
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 100$ mA		0.6	0.9	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 5.25V$		10	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			100	μA
V_{IH}	High Level Receiver Threshold	$V_{IN} = 0.8V$, $V_{OL} = 16$ mA	1.90	1.70		V
V_{IL}	Low Level Receiver Threshold	$V_{IN} = 0.8V$, $I_{OH} = -400$ μA		1.70	1.50	V
RECEIVER OUTPUT						
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = 5.25V$, (Note 4)	−40	−70	−100	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$		50	90	mA

Switching Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PROPAGATION DELAYS						
t_{PLHD}	Disable to Bus "1"	*Figure 1*		25	35	ns
t_{PHLD}	Disable to Bus "0"			25	35	ns
t_{PLHB}	Driver Input to Bus "1"	*Figure 2*		20	30	ns
t_{PHLB}	Driver Input to Bus "0"			20	30	ns
t_{PLHR}	Bus to Logical "1" Receiver Output	*Figure 3*		25	40	ns
t_{PHLR}	Bus to Logical "0" Receiver Output			25	40	ns
NOISE IMMUNITY						
t_{rB}, t_{fB}	Rise and Fall Times (10%–90%) of the Driver Output	*Figure 2*	10	15	20	ns
t_{nR}	Receiver Noise Rejection Pulse Width	No Response at Receiver Output as per *Figure 4*		20	10	ns

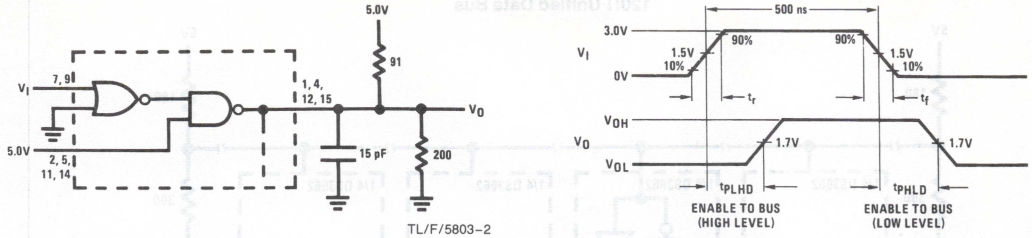
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Waveforms

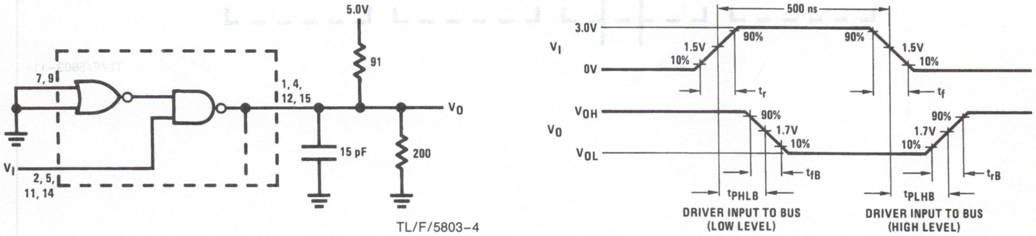

5.0V
91
V_I
7, 9
5.0V
2, 5,
11, 14
1, 4,
12, 15
V_O
15 pF
200
500 ns
3.0V
0V
1.5V
10%
90%
t_r
t_f
V_OH
V_OL
1.7V
t_PLHD
t_PHLD
ENABLE TO BUS (HIGH LEVEL)
ENABLE TO BUS (LOW LEVEL)

TL/F/5803-2

TL/F/5803-3

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 1. Disable Delays

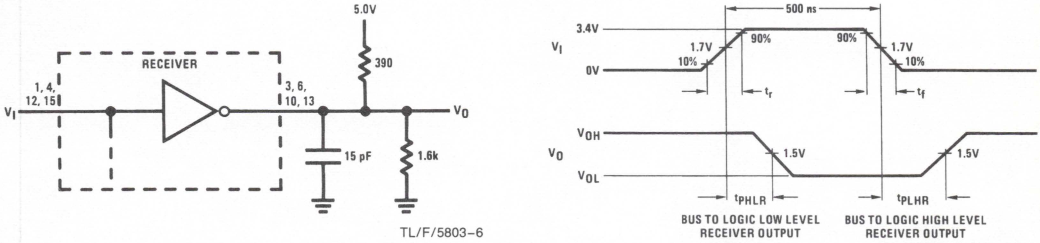

5.0V
91
7, 9
V_I
2, 5,
11, 14
1, 4,
12, 15
V_O
15 pF
200
500 ns
3.0V
0V
1.5V
10%
90%
t_r
t_f
V_OH
V_OL
1.7V
t_fB
t_rB
t_PHLB
t_PLHB
DRIVER INPUT TO BUS (LOW LEVEL)
DRIVER INPUT TO BUS (HIGH LEVEL)

TL/F/5803-4

TL/F/5803-5

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 2. Driver Propagation Delays

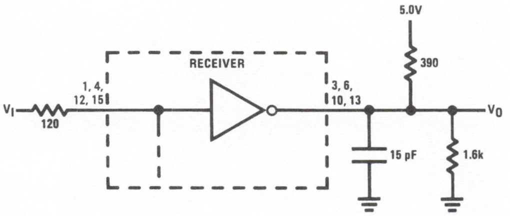

5.0V
390
RECEIVER
1, 4,
12, 15
V_I
3, 6,
10, 13
V_O
15 pF
1.6k
500 ns
3.4V
0V
1.7V
10%
90%
t_r
t_f
V_OH
V_OL
1.5V
t_PHLR
t_PLHR
BUS TO LOGIC LOW LEVEL RECEIVER OUTPUT
BUS TO LOGIC HIGH LEVEL RECEIVER OUTPUT

TL/F/5803-6

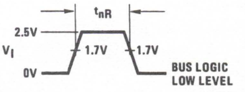
TL/F/5803-7

Note: $t_r = t_f = 15$ ns. Pulse width = 500 ns measured between 1.7V levels. f = 1 MHz.

FIGURE 3. Receiver Propagation Delays


5.0V
390
RECEIVER
V_I
120
1, 4,
12, 15
3, 6,
10, 13
V_O
15 pF
1.6k

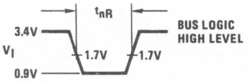
TL/F/5803-8


t_nR
2.5V
V_I
0V
1.7V
1.7V
BUS LOGIC LOW LEVEL

TL/F/5803-9

$t_r = t_f = 2.5$ ns

(a) Receiver Output (V_O) to Remain Greater than 2.2V


t_nR
3.4V
V_I
0.9V
1.7V
1.7V
BUS LOGIC HIGH LEVEL

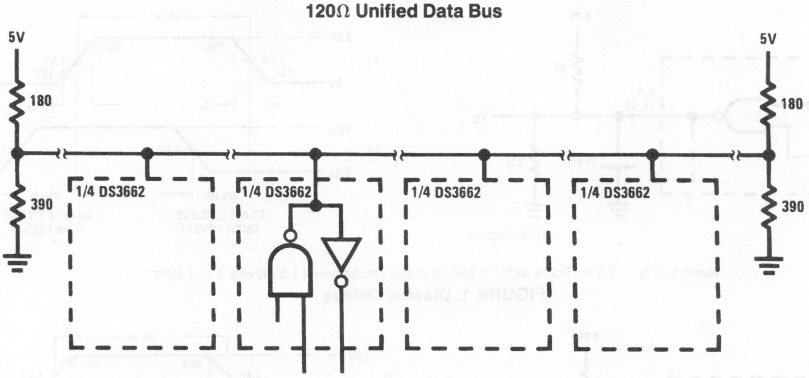
TL/F/5803-10

$t_r = t_f = 2.5$ ns

(b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms

Typical Application


120Ω Unified Data Bus
5V
180
390
1/4 DS3662
1/4 DS3662
1/4 DS3662
1/4 DS3662
5V
180
390

TL/F/5803-11

DS3662—The Bus Optimizer

National Semiconductor
Application Note 259
R. V. Balakrishnan

I. INTRODUCTION

A single ended Bus is an unbalanced Data Transmission medium, which is timeshared by several system elements. Like any unbalanced system, it is highly susceptible to common-mode noise, such as ground noise and crosstalk. In general, the latter determines the maximum physical length of the Bus that can be incorporated with acceptable reliability. Crosstalk is a major problem in high speed computer Buses which employ Schottky Transceivers for increased data rate capability. It is therefore highly desirable to minimize crosstalk noise in Bus circuits to allow for longer Buses and to provide higher system reliability.

This article describes the operation of the DS3662 Quad High Speed Trapezoidal Bus Transceiver, which has been specially designed to minimize crosstalk problems. The Driver generates precise Trapezoidal waveforms that reduce noise coupling to adjacent Bus channels. The Receiver uses a low pass filter, whose time constant is matched to the Driver slew rate to provide maximum noise rejection with acceptable signal delay characteristics. Precision high speed circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky Transceivers.

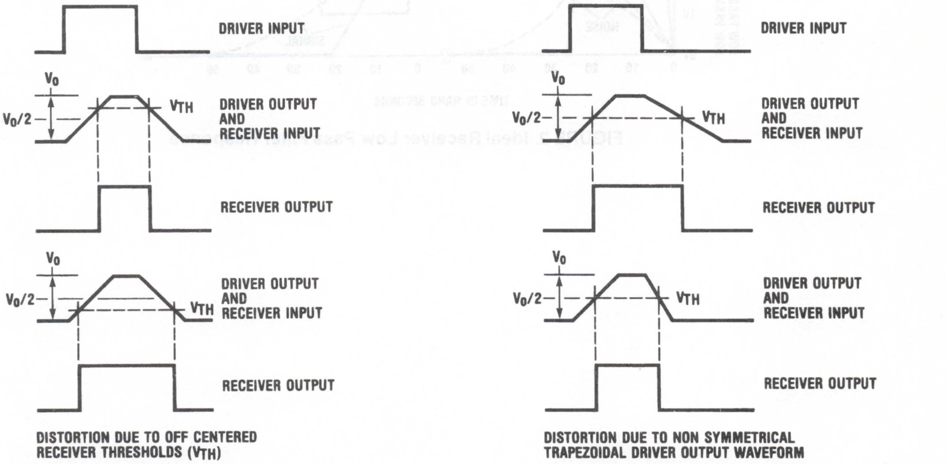
II. THE PROBLEM

Conventional Bus Drivers are designed to provide high output currents for charging and discharging relatively large Bus capacitances quickly. These high speed transitions are characterized by peak slew rates of up to 5V/ns around the mid-region of the transition. This can cause considerable noise coupling to adjacent lines, commonly referred to as crosstalk. Crosstalk also includes noise induced by sources external to the Bus. Additional noise may be generated due to reflections at imperfect terminations.

Bus Receviers are designed to respond to high speed transitions and to provide low propagation delays. Unfortunately, their fast response results in high noise sensitivity. The combined effect of the noise on the Bus and the sensitivity of the Receiver to the noise severely limits the Bus performance.

III. THE SOLUTION

The above situation can be considerably improved by employing noise reduction techniques in both the Driver and the Receiver circuits. Slew rate control can be used in the Driver to reduce crosstalk, and Receiver noise sensitivity can be reduced by using a low pass filter at its input. These techniques are commonly used in line transmission circuits where the associated data rates in general are considerably lower. However, these techniques do present some difficulties in high speed Bus circuits. Increased rise and fall times, resulting from slew rate control, can affect data rates unless care is taken to limit the maximum rise and fall times to minimum pulse width requirements. With any appreciable slew rate control, the rise and fall times of the resulting Driver output waveform will be comparable to the pulse widths at maximum data rates. This condition dictates high fidelity of the transmitted waveform and precise Receiver thresholds at the middle of the Bus voltage swing in order to minimize pulse width distortion. *Figure 1* illustrates the different sources of pulse width distortion due to the trapezoidal nature of the signal.



DISTORTION DUE TO OFF CENTERED RECEIVER THRESHOLDS (V_{TH})

DISTORTION DUE TO NON SYMMETRICAL TRAPEZOIDAL DRIVER OUTPUT WAVEFORM

TL/F/5857-1

TL/F/5857-2

FIGURE 1. Pulse Width Distortion

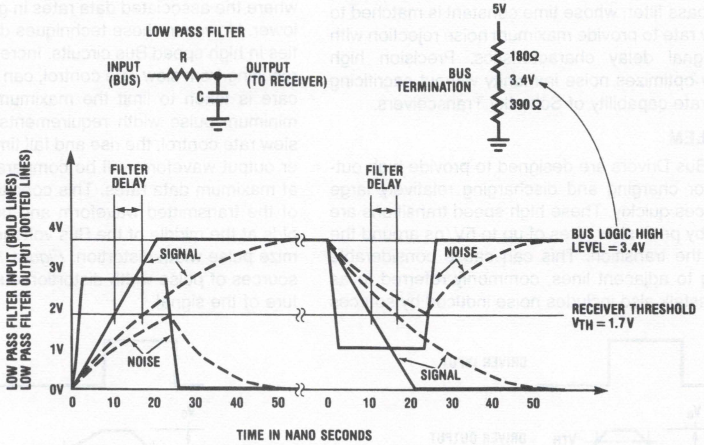
The low pass filter in the Receiver should provide optimum noise rejection without introducing excessive delay in passing the signal waveform. In addition, the Receiver should have a symmetrical response to positive and negative going transitions in order to maintain a low level of pulse width distortion, as well as equal noise rejection to positive and negative going noise pulses. The response of an ideal low pass filter to signal and noise pulses is shown in *Figure 2.*

The DS3662 overcomes these and other problems by using high speed linear circuitry with on-chip capacitors for controlling slew rate and low pass filtering. The Driver is of open collector type intended for use with terminated 120Ω Buses. The external termination consists of a 180Ω resistor from the Bus to +5V logic supply with a 390Ω resistor from the Bus to ground. Such a termination results in a Bus logic high level of 3.4V with V_{CC} at 5V (See *Figure 2*). The Bus can be terminated at one or both ends as shown in *Figure 3.*

IV. THE DRIVER

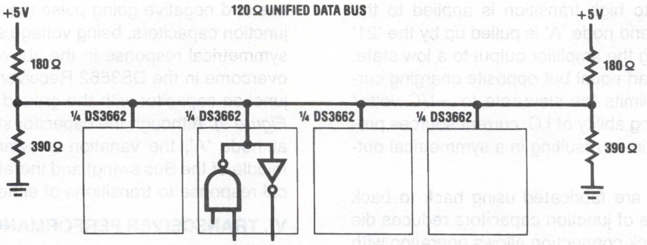
Using a Miller integrator circuit, the Driver generates a linearly rising and falling waveform with a constant slew rate of 0.2V/ns (typical) during the entire period of transition. This corresponds to typical rise and fall times of 15 ns. *Figure 4* compares the output waveform of a typical Schottky Driver and the DS3662 under different capacitive loads. It should be noted that even under heavy loading, the regular Drivers have peak slew rates that are considerably higher than the average. In contrast, the trapezoidal waveform provides considerably lower slew rate with slightly higher rise and fall times. Such an increase in rise and fall time has very little effect on data rates. In fact, the high fidelity of the transmitted waveform allows pulse widths as low as 20 ns to be transmitted on the Bus, as shown in *Figure 5.*

The block diagram of the Driver is shown in *Figure 6* and *7.* When a high to low transition is applied to the input, switch 'S' opens and node 'A' is pulled low by the current source 'I'. This switches the amplifier output to a high state. The slew rate of the output transition is limited by the charging current through the capacitor, a constant value equal to I/C volts/sec.



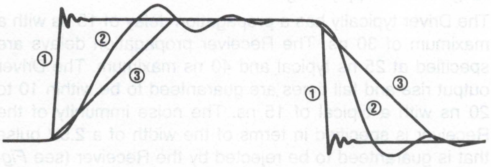
TL/F/5857-3

FIGURE 2. Ideal Receiver Low Pass Filter Response


+5V
120 Ω UNIFIED DATA BUS
+5V
180 Ω
390 Ω
¼ DS3662
¼ DS3662
¼ DS3662
¼ DS3662
180 Ω
390 Ω

TL/F/5857-4

FIGURE 3. Bus Termination



TL/F/5857-5

①—Typical High Speed Driver Output Unloaded

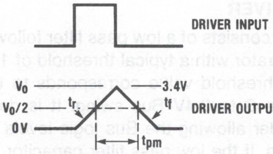
②—Typical High Speed Driver Output Loaded

③—Typical Output of Controlled Slew Rate Driver Which is Load Independent

① $t_r = t_f \sim 3$ ns
② $t_r = t_f \sim 10$ ns
③ $t_r = t_f \sim 15$ ns

Note: The word "loading" here refers to capacitive loading only.

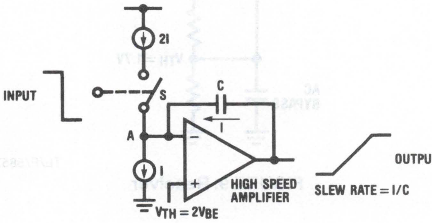
FIGURE 4. Waveform Comparison


DRIVER INPUT
V_0
3.4V
$V_0/2$
t_r
t_f
DRIVER OUTPUT
0V
t_{pm}

TL/F/5857-6

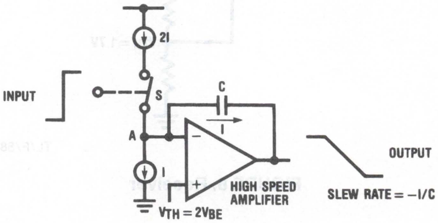
$t_{pm} \approx 20$ ns $t_r \approx t_f \approx 15$ ns (10% to 90%)

FIGURE 5. Minimum Pulse Width Driver Output


2I
INPUT
S
C
I
A
I
–
+
HIGH SPEED AMPLIFIER
OUTPUT
SLEW RATE = I/C
$V_{TH} = 2V_{BE}$

TL/F/5857-7

FIGURE 6. Driver


2I
INPUT
S
C
I
A
I
–
+
HIGH SPEED AMPLIFIER
OUTPUT
SLEW RATE = –I/C
$V_{TH} = 2V_{BE}$

TL/F/5857-8

FIGURE 7. Driver

Likewise, when a low to high transition is applied to the input, switch 'S' closes and node 'A' is pulled up by the '21' current source, switching the amplifier output to a low state. The capacitor now has an equal but opposite charging current which once again limits the slew rate to −I/C volts/sec. The inherent tracking ability of I.C. current sources provide equal rise and fall times resulting in a symmetrical output waveform.

The on-chip capacitors are fabricated using back to back junction diodes. The use of junction capacitors reduces die area and the back to back connection allows operation with either polarity. The capacitor terminal, connected to the amplifier input, remains at $V_{th} \cong 1.6V$ during the output transition. This voltage, being close to the middle of the output swing, reduces the effect of the capacitor voltage sensitivity on the output waveshape.

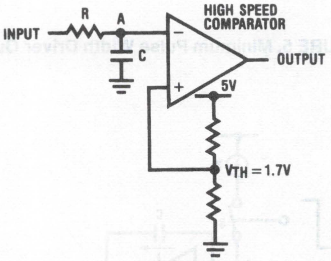
V. THE RECEIVER

The Receiver consists of a low pass filter followed by a high speed comparator with a typical threshold of 1.7V (see *Figure 8*). This threshold value corresponds to the mid-point voltage of the 0 to 3.4V Bus swing. It is derived from a potential divider allowing the Bus logic levels to track with V_{CC} variations. If the low pass filter capacitor is voltage insensitive, this circuit will provide equal propagation delay for positive and negative going signal transitions on the Bus. In addition, it will also provide equal noise rejection to a positive and negative going pulse (see *Figure 2*). However, the junction capacitors, being voltage sensitive, will exhibit nonsymmetrical response in the above circuit. This problem is overcome in the DS3662 Receiver by using a back to back junction capacitor with the ground end biased at 1.7V (see *Figure 9*). Although the capacitor still varies with the voltage at node 'A', the variation is symmetrical about 1.7V (the middle of the Bus swing) and therefore will provide an identical response to transitions of either polarity.

VI. TRANSCEIVER PERFORMANCE

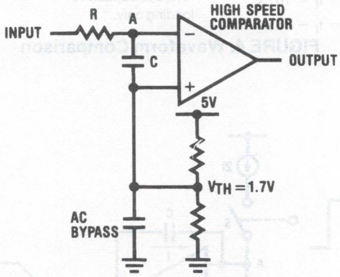
The characteristics of the trapezoidal Transceiver are fully detailed in the device data sheet. Some of the more important specifications are discussed below. Both AC and DC specifications are guaranteed over a 0–70°C temperature range and a supply range of 4.75–5.25V.

The Driver typically has a propagation delay of 15 ns with a maximum of 30 ns. The Receiver propagation delays are specified at 25 ns typical and 40 ns maximum. The Driver output rise and fall times are guaranteed to be within 10 to 20 ns with a typical of 15 ns. The noise immunity of the Receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the Receiver (see *Figure 10*). The Receiver typically rejects a 20 ns pulse going positive from ground level or going negative from a 3.4V logic 1 level. Worst case rejection is specified at 10 ns.



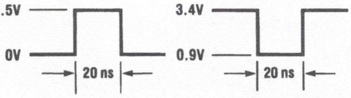
TL/F/5857-9

FIGURE 8. Receiver



TL/F/5857-10

FIGURE 9. Receiver



TL/F/5857-11

Rejects positive or negative going noise pulses of pulse widths up to 20 ns typical.
Detects and propagates trapezoidal signal pulses in 20 ns typical.

FIGURE 10. Receiver Noise Immunity

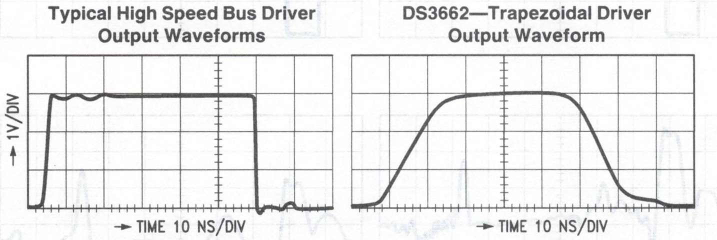
The AC response of the DS3662 Driver and Receiver are depicted in *Figures 11* and *12* respectively. *Figure 11* shows the typical Driver output waveform as compared to a standard high speed Transceiver output. Oscillograms in *Figure 12* demonstrate the ability of the Receiver to distinguish the trapezoidal signal from the noise. Here the Receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (= 16 ns) of the same amplitude (The signal is triangular since the pulse width is smaller than the rise and fall time of the Trapezoidal Driver output).

The performance of the Transceiver under actual operating condition is demonstrated in *Figures 13* through *15*. Oscillograms in *Figure 13* clearly show the capability of the DS3662 in real life situations. Here it is compared with the DS8834 under identical conditions. The Transceivers drive a minicomputer Bus (flat ribbon cable) 100 feet long, terminated at the far end with taps at various lengths for connecting to the Receiver input. The cable is randomly folded to generate crosstalk between the various parts. In addition a noise pulse is induced on the signal line by driving an adjacent line with a pulse generator. This corresponds to the second dominant pulse in the Bus waveforms at approximately 600 ns from the main signal pulse. As can be seen, the DS8834 with fast rise and fall times on the Driver output generates more crosstalk and its Receiver easily responds to this crosstalk and to the externally induced noise (even though it has hysteresis!), limiting the useful Bus length to less than 10 feet. In contrast, the DS3662's Driver generates much less crosstalk and its Receiver is immune to the induced noise even when the noise amplitude exceeds the signal amplitude as seen in the oscillogram at 50 feet. When the same experiment was repeated with the DS8641, it responded to the noise even at 10 feet as shown in *Figure 14*.

Figure 15 shows the plots of maximum data rate versus line length for the three Transceivers discussed above under two different conditions. The graph in *Figure 15a* is obtained with no consideration to the pulse width distortion whereas the one in *Figure 15b* is obtained for a maximum allowable pulse width distortion of ±10%. A square waveform is used so that the pulse width distortion criteria will apply to both positive and negative going pulses. These graphs clearly show that the DS3662 can be used at considerably higher data rates with lower distortion for longer distances than the other two Transceivers *(Figure 15b)* although the others have a slightly higher data rate capability at short distances with high timing distortion *(Figure 15a)*.

VII. CONCLUSION

The DS3662, with its combination of a trapezoidal Driver and a noise rejecting Receiver utilizing on chip capacitors, represents a significant improvement in high speed Bus circuits and a solution to Bus noise problems commonly encountered in Mini and Microcomputer systems.



Typical High Speed Bus Driver Output Waveforms

DS3662—Trapezoidal Driver Output Waveform

FIGURE 11

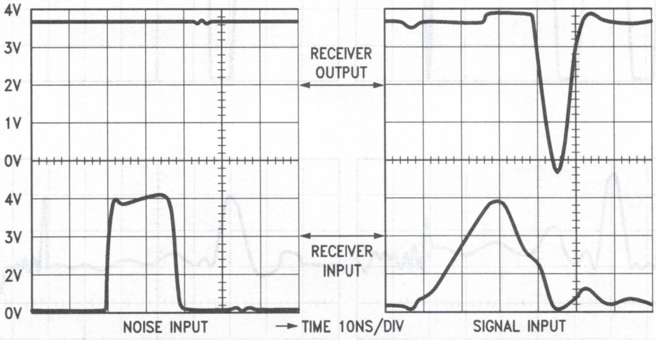
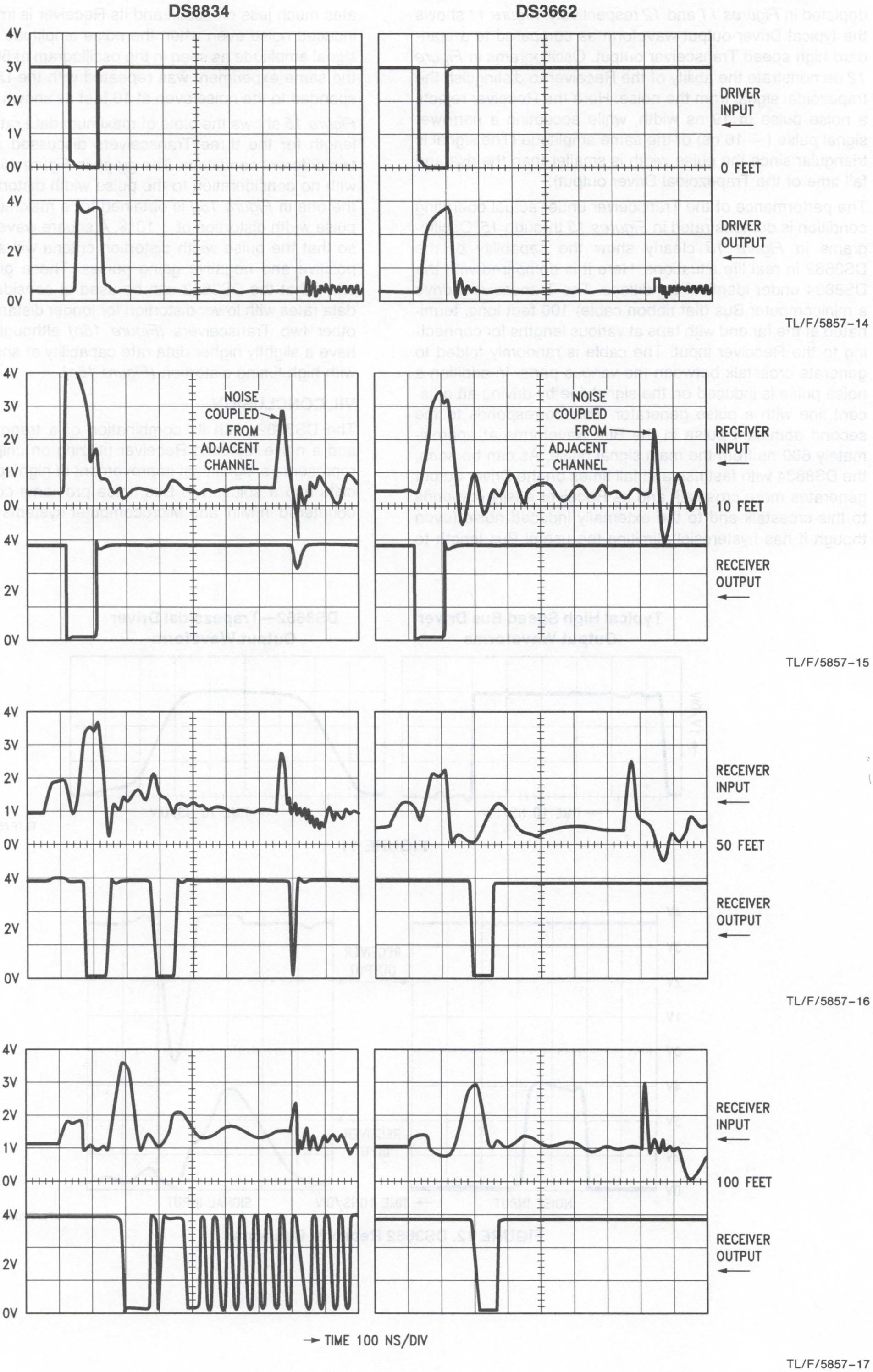


FIGURE 12. DS3662 Receiver Response



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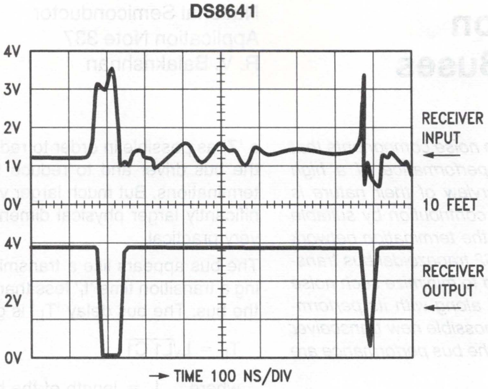
TL/F/5857-15

TL/F/5857-16

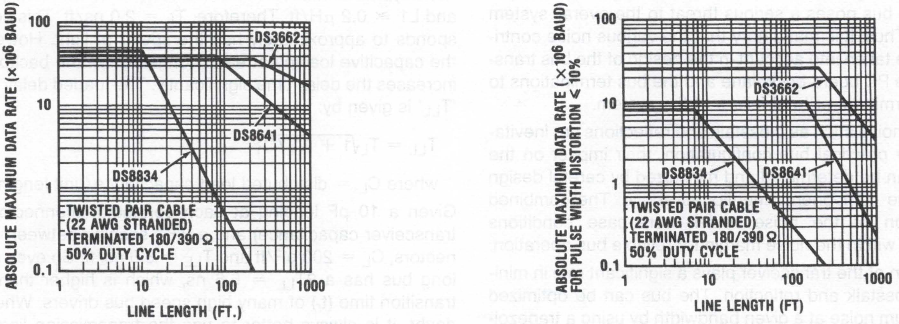
TL/F/5857-17

FIGURE 13



TL/F/5857-18

FIGURE 14



TL/F/5857-19

TL/F/5857-20

FIGURE 15. Data Rate vs. Line Length

Reducing Noise on Microcomputer Buses

National Semiconductor
Application Note 337
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Abstract: *This paper focuses on the noise components that have a significant impact on the performance of a high speed microcomputer bus. An overview of their nature is followed by ways to minimize their contribution by suitable design of the PC board backplane, the termination network and the bus transceiver. The DS3662 trapezoidal bus transceiver, which is specifically designed to minimize such noise on high speed buses, is presented along with its performance data. And to conclude, some possible new transceiver designs for further improvement of the bus performance are explored.*

INTRODUCTION

As the microcomputer bus bandwidth is extended to handle ever increasing clock rates, the noise susceptibility of a single-ended bus poses a serious threat to the overall system integrity. Thus, it is mandatory that the various noise contributions be taken into account in the design of the bus transceiver, the PC board backplane and the bus terminations to avoid intermittent or total failure of the system.

Although noise such as crosstalk and reflections are inevitable in any practical bus configuration, their impact on the system can be determined and minimized by careful design of all three components mentioned above. The combined contribution of the noise under worst-case conditions should be within the noise margin for reliable bus operation.

The design of the transceiver plays a significant role in minimizing crosstalk and reflection. The bus can be optimized for minimum noise at a given bandwidth by using a trapezoidal driver having suitable rise and fall times along with a matched low pass filtered receiver which provides a symmetrical noise margin. The DS3662 is one such transceiver, the first member in the family of trapezoidal bus transceviers available from National Semiconductor Corporation. This device represents a significant improvement in high speed bus circuit design and provides a solution to commonly encountered bus noise problems.

THE MICROCOMPUTER BUS

A typical microcomputer bus usually consists of a printed circuit board backplane with signal and ground traces on one side and a ground plane on the other. The length ranges from a few inches to several feet with as many as 32 closely spaced (0.6″ typical) card edge connectors. Each signal line interacts with the ground plane to form a transmission line with characteristic impedance 'Z' in the range of 90Ω–120Ω typical. It is desirable to have as large a 'Z' as possible in order to reduce the drive requirement of the bus driver and to reduce the power dissipated at the terminations. But much larger values of 'Z" translate to significantly larger physical dimensions and therefore are not very practical.

The bus appears like a transmission line to any signal having a transition time 't_r' less than the round trip delay '$2T_L$' of the bus. The bus delay 'T_L' is given by:

$$T_L = L\sqrt{L1\,C1} \qquad (1)$$

where L = length of the bus
$L1$ = distributed inductance per unit length
$C1$ = distributed capacitance per unit length

For a typical unloaded 100Ω microstrip line, $C1 \cong 20$ pF/ft and $L1 \cong 0.2$ μH/ft. Therefore, $T_L = 2.0$ ns/ft. This corresponds to approximately half the speed of light. However, the capacitive loading at each connector on the backplane increases the delay time significantly. The loaded delay time 'T_{LL}' is given by:

$$T_{LL} = T_L\sqrt{1 + (C_L/C_1} \qquad (2)$$

where C_L = distributed load capacitance/unit length

Given a 10 pF loading at each connector (connector + transceiver capacitance) and a 0.6″ spacing between connectors, C_L = 200 pF/ft and T_{LL} = 6.6 ns/ft. So even a 6″ long bus has a $2T_{LL}$ = 6.6 ns, which is higher than the transition time (t_r) of many high speed bus drivers. When in doubt, it is always better to use the transmission line approach than the lumped circuit approach as the latter is an approximation of the former. Also, the transmission line analysis gives more pessimistic (worst-case) values of crosstalk and reflection and is, hence, safer.

CROSSTALK REDUCTION

The crosstalk is due to the distributed capacitive coupling C_C and the distributed inductive coupling L_C between two lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 1.* Their respective peak amplitudes are:

$$V_{NE} = K_{NE}(2T_L)(V_I/t_r) \quad \text{for } t_r > 2\,T_L \qquad (3)$$

$$V_{NE} = K_{NE}(V_I) \quad \text{for } t_r < 2\,T_L \qquad (4)$$

$$V_{FE} = K_{FE}(L)(V_I/t_r) \qquad (5)$$

where V_I = signal swing on the drive line.

The coupling constants are given by the expressions:

$$K_{NE} = \frac{L(C_C Z + L_C/Z)}{4T_L} \qquad (6)$$

$$K_{FE} = \frac{C_C Z - L_C/Z}{2} \text{ ns/ft} \qquad (7)$$

The near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of near and far end crosstalk waveforms shown.

It should be noted from expressions 6 and 7 that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it. In microstrip backplanes the far end crosstalk pulse is usually the opposite polarity of the original signal.

Although the real world bus is far from the ideal situation depicted in *Figure 1,* several useful observations that apply to a general case can be made:

1. The crosstalk always scales with the signal amplitude.
2. Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
3. Far end crosstalk width is always t_r.
4. For $t_r < 2T_L$, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is a function of physical layout only.
5. The higher the value of 't_r' the lower the percentage of crosstalk (relative to signal amplitude).

The corresponding design implications are:

1. The noise margin expressed as a percentage of the signal swing is what's important, not the absolute noise margin. Therefore, to improve noise immunity, the percentage noise margin has to be maximized. This is achieved by reducing the receiver threshold uncertainty region and by centering the threshold between the high and low levels.
2. Smaller signal amplitude with the same transition time reduces bus drive requirements without reducing noise immunity.
3. Far end crosstalk is eliminated if the receiver is designed to reject pulses having pulse widths less than or equal to t_r.
4. When $t_r < 2T_L$, the near end crosstalk immunity for a given percentage noise margin has to be built into the backplane PC layout. Since $(V_{NE}/V_I) = K_{NE}$ for this case, K_{NE} should be kept lower than the available worst-case noise margin. K_{NE} may be reduced by either increasing the spacing between lines or by introducing a ground line in between. The ground line, in addition to increasing the spacing between the signal lines, forces the electric field lines to converge on it, significantly reducing crosstalk.
5. For minimum crosstalk the rise and fall times of the signal waveform should be as large as possible consistent with the minimum pulse width requirements of the bus. A driver that automatically limits the slew rate of the transition can go a long way in reducing crosstalk.

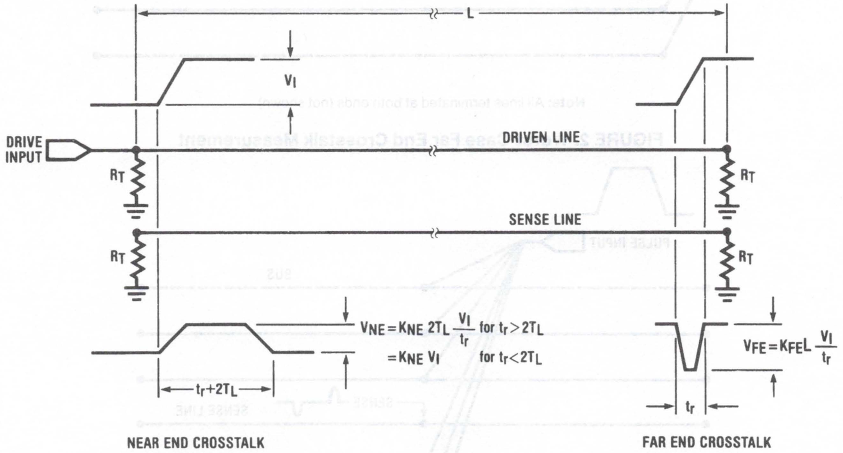
L
V_I
DRIVE INPUT
DRIVEN LINE
R_T
R_T
SENSE LINE
R_T
R_T
$V_{NE} = K_{NE}\, 2T_L \frac{V_I}{t_r}$ for $t_r > 2T_L$
$= K_{NE} V_I$ for $t_r < 2T_L$
$t_r + 2T_L$
$V_{FE} = K_{FE} L \frac{V_I}{t_r}$
t_r
NEAR END CROSSTALK
FAR END CROSSTALK

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FIGURE 1. Crosstalk under Ideal Conditions

CROSSTALK MEASUREMENT

When multiple lines on either side of the sense lines switch simultaneously the crosstalk is considerably larger, typically 3.5 times the single line switching case for microstrip backplanes. Also, the location of the drivers on the driven lines and the receiver on the sense line for worst-case crosstalk differs for the near end and far end cases as shown in *Figure 2* and *3* for a uniformly loaded bus. But if the far end crosstalk is not of the opposite polarity, then the combined effect of far end and near end crosstalk could have a larger amplitude and pulse width at a point near the middle of the sense line in *Figure 2.* So in a general case, or in the case of a non-uniformly loaded bus, it is advisable to check the sense line at several locations along the length of the bus to determine the worst-case crosstalk. The measurement should be made for both the positive and the negative transition of the drive signal.

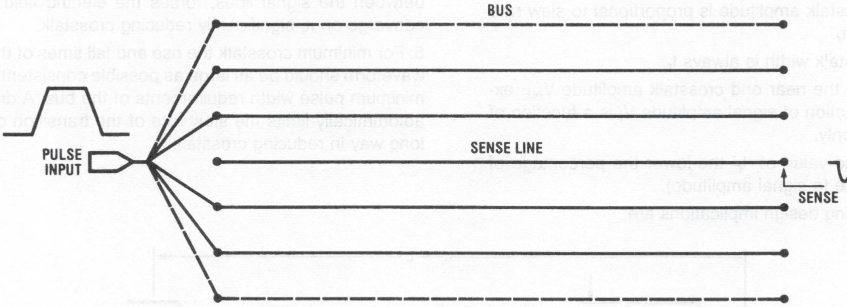
THE TERMINATION

A properly terminated transmission line has no reflections. But a practical microcomputer bus is neither a perfect transmission line nor is it properly terminated under all conditions. The capacitive loading at discrete locations, such as a used card slot, act as sources of reflection. However, in the limiting case when the bus is uniformly populated with a large number of modules, the bus behaves like a lower impedance transmission line. The loaded impedance 'Z_L' of the bus is given by the expression:

$$Z_L = \frac{Z}{\sqrt{1 + C_L/C_1}} \qquad (8)$$

where Z = unloaded line impedance

Unfortunately, uniform loading of the bus is not guaranteed at all times and even if it were (by dummy loading of



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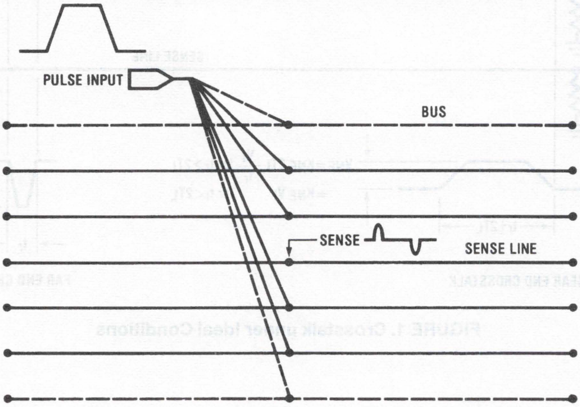
Note: All lines terminated at both ends (not shown)

FIGURE 2. Worst-Case Far End Crosstalk Measurement



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Note: All lines terminated at both ends (not shown)

FIGURE 3. Worst-Case Near End Crosstalk Measurement

the unused slots) Z_L is usually too low for proper termination of the bus. For example, a 10 pF per module loading of the 100Ω microstrip bus at 0.6″ spacing results in a $Z_L = 30\Omega$. One such termination at each end will require a 200 mA drive capacity on the bus driver for a nominal 3V swing. Such large drive currents and low value terminations increase the power dissipation of the system significantly in addition to causing other problems such as increased ground drop, inductive drops in traces due to large current being switched, etc. As a compromise the bus is usually terminated at an impedance higher than Z_L but less than or equal to Z. Consequently, there is always some amount of reflection present. For a perfect transmission line the reflection coefficient 'Γ' is given by the well known expression:

$$\Gamma = \frac{Z - R_t}{Z + R_t} \qquad (9)$$

where Z = impedance of the bus

R_t = termination resistance

The net effect, in the general case of a nonuniformly loaded bus, is that it may take several round trip bus delays after a bus driver output transition, before the quiescent voltage level is established. However, this delay is avoided by using a bus driver that has sufficient drive to generate a large enough voltage step during the first transition to cross well beyond the receiver threshold region under the worst-case load conditions.

Figure 4 illustrates the driver output waveform under such a condition. Here the fully loaded bus (with $Z_L = 30\Omega$), of the previous example, is driven by the DS3662 bus transceiver at the mid point. The driver is actually driving two transmission lines of $Z_L = 30\Omega$ in either direction from the middle and hence the initial step is given by:

$$V1 = \left(\frac{Z_L}{2}\right) 2I_S \qquad (10)$$

where I_S = Standing current on the bus due to each termination

For the DS3662, the termination can be designed for $2I_S$ = 100 mA and therefore:

V1 = (30/2)100 = 1.5V

This value of the initial swing is large enough to cross the narrow threshold region of the receiver as shown and therefore no waiting period is required for the reflections to build up the output high level. On the negative transition the problem is less critical due to the much higher sink capability of the DS3662 during pull down.

Reflections can also be caused by resistive loading of the bus by the DC input current of the receiver. The resulting reflectoin coefficient (Γ) is given by the expression:

$$\Gamma = -\tfrac{1}{2}\left(\frac{I_R}{I_S}\right) \qquad (11)$$

where I_R = receiver input current

Having a receiver with a high input impedance not only makes this component of reflection insignificant but also reduces the DC load on the driver, allowing the use of lower value termination resistors. This is particularly true when a large number of modules are connected to the bus.

The design implications of the above discussion may be summarized as follows:

1. If the driver has adequate drive to produce the necessary voltage swing under the worst-case loading ($Z_L/2$), reflections do not restrict the bus performance. This translates to a 100 mA minimum drive requirement for a typical microstrip bus.

2. If the drive is insufficient, time should be allowed for the reflections to build up the voltage level before the data is sampled.

3. For signals such as clock, strobe, etc., wherein the edge is used for triggering events, it is mandatory that the driver meet the above drive requirements if delayed or multiple triggering is to be avoided.

4. An ideal TTL bus transceiver should have at least a 100 mA drive, a high input impedance receiver with a narrow threshold uncertainty region.

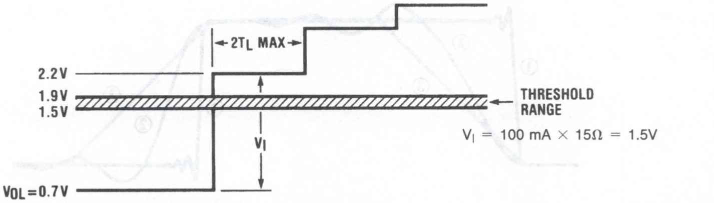


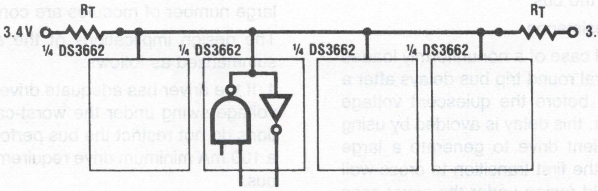
FIGURE 4. Worst-Case DS3662 Output Transition for $Z_L = 15\Omega$ and $R_T = 50\Omega$

THE DS3662 TRANSCEIVER

The DS3662 quad trapezoidal bus transceiver has been designed specifically to minimize the noise problems discussed previously. The driver generates precise trapezoidal waveforms that reduce crosstalk and the receiver uses a low pass filter to reject noise pulses having pulse widths up to the maximum driver output transition times. Precision output circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky transceivers.

Figure 5 shows the recommended configuration for microcomputer buses. The use of a 3.4V source with a single termination resistor at each end reduces the average power dissipation of the bus. However, a two resistor termination connected between the line and the power rails, having the same Thevenin's equivalent, can be substituted for lower cost.

Using a Miller integrator circuit, the driver generates a linearly rising and falling waveform with a constant slew rate of 0.2 V/ns *(Figure 6)*. This corresponds to a nominal transition time of 15 ns. *Figure 7* compares the output waveform of a typical high speed driver to that of DS3662 under different load conditions. It should be noted that even under heavy loading, the regular drivers have peak slew rates that are much higher than the average. On the other hand, the trapezoidal waveform has a much lower slew rate with only a slight increase in the transition time. Such an increase in the transition time has little or no effect on the data rates. In fact, the high fidelity of the DS3662 driver output waveform allows pulse widths as low as 20 ns to be transmitted on the bus.



R_T = 50Ω to 90Ω

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FIGURE 5. Recommended Bus Termination for Heavily Loaded Microstrip Backplanes

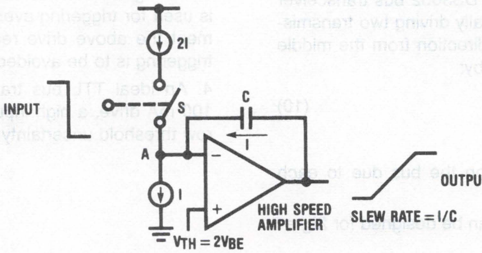

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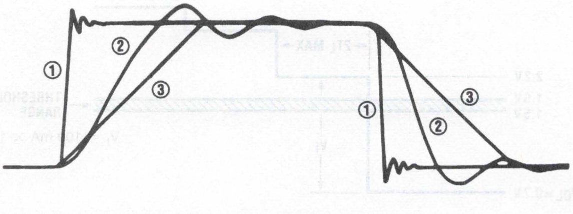
FIGURE 6. DS3662 Driver



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Note 1: Typical high speed driver output unloaded; $t_r = t_f \approx 3$ ns

Note 2: Typical high speed driver output loaded; $t_r = t_f \approx 10$ ns

Note 3: Typical output of controlled slew rate driver which is load independent; $t_r = t_f \approx 15$ ns

FIGURE 7. Waveform Comparison

The receiver consists of a low pass filter followed by a high speed comparator, with a typical threshold of 1.7V *(Figure 8)*. The noise immunity of the receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the receiver. The receiver typically rejects a 20 ns pulse going positive from the ground level or going negative from the 3.4V logic 1 level. The receiver threshold lies within a specified 400 mV region over the supply and temperature range and is centered between the low and high levels of the bus for a symmetrical noise margin.

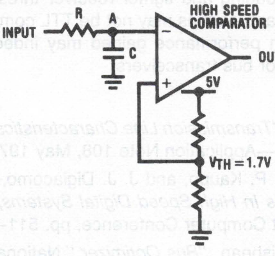

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FIGURE 8. DS3662 Receiver

Other features of the device include a 100 μA maximum DC bus loading specification under power ON or OFF condition and a glitch-free power up/down protection on the bus output.

Waveforms in *Figure 9* demonstrate the ability of the receiver to distinguish the trapezoidal signal from noise. Here the receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (16 ns) of the same peak amplitude (the signal is triangular because of the pulse width which is smaller than the transition time).

The real-world performance of the DS3662 transceiver shows an order of magnitude improvement in noise immunity over conventional transceivers under actual operating conditions (Reference #3). The controlled rise and fall times on the driver output significantly reduces both near end and the far end crosstalk. As expected, the pulse discrimination at the receiver input virtually eliminates the far end crosstalk, even on extremely long buses (over 100 feet). The near end crosstalk, which is particularly severe on the state of the art backplanes due to the tight spacing between the signal lines, is easily accommodated by the large percentage noise margin (>75%) provided by the receiver. Field reports indicate that the DS3662 not only solves those mysterious intermittent failure problems in mini and microcomputer systems, but also helps them meet the new FCC emission requirements due to the reduced RF radiation from the bus.

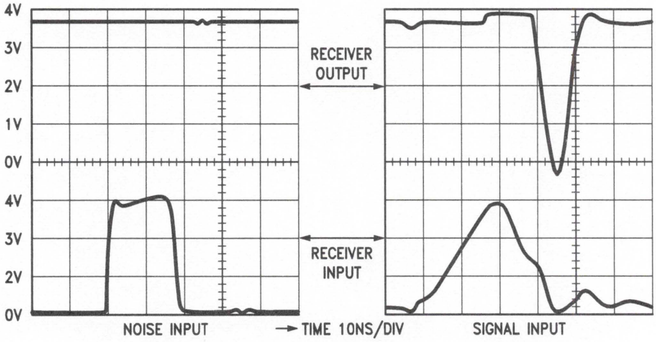

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FIGURE 9. DS3662 Receiver Response

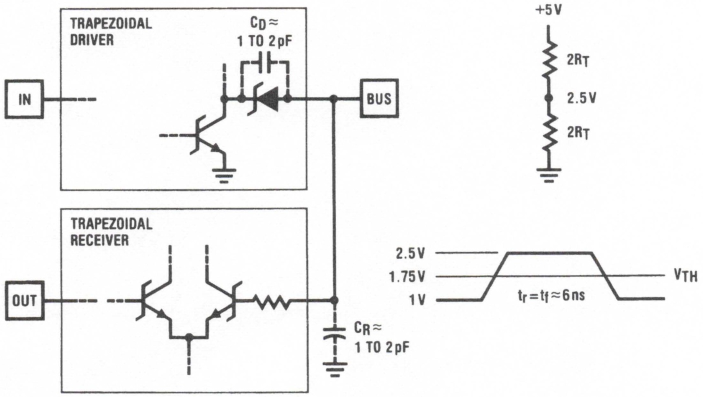

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FIGURE 10. High Speed Bus Transceiver with Low Output Loading for MicroComputer Backplanes

WHAT NEXT?

Since crosstalk scales with the signal amplitude, reducing the signal swing has not effect on the noise immunity as long as the percentage noise margin remains the same. On the other hand, there are several advantages in having lower signal swing. It reduces the drive current requirement of the driver thus reducing its output capacitance. Lower capacitive loading on the bus decreases its impedance reducing the drvie requirement even further. Having a lower current drive not only reduces the power dissipated at the terminations but also allows better matching of the termination due to the increased line impedance. In the ideal limiting case the driver has negligible loading effect on the bus and thus allows perfect termination under all load conditions.

In practice however, there are some obvious limitations. The receiver thresholds have to be maintained within tighter limits at lower signal swings to maintain the same percentage noise margin. Also, the capacitive loading is difficult to reduce beyond a certain point, due to the diminishing return in the way of lower current rating, as the loaded bus impedance approaches the unloaded impedance. However, the capacitance of an open collector driver output can be reduced significantly by using a Schottky diode as shown in *Figure 10.* The diode isolates the driver capacitance when the output is disabled. Using reduced signal swings and precise receiver thresholds, such a transceiver can provide significant improvements in microcomputer bus performance. The transceiver design presented in *Figure 10* is being considered for incorporation into the Futurebus standard by the IEEE.

CONCLUSION

A well designed bus transceiver goes a long way in improving the noise immunity of a single-ended TTL bus. Further improvements in bus performance may come from the use of reduced voltage swings and better transceiver designs for lower bus loading and tighter receiver threshold limits. Although such approaches may not be TTL compatible, the improvement in performance gained may indeed justify a new standard for bus transceivers.

REFERENCES

1) Bill Fowler, *"Transmission Line Characteristics,"* National Semiconductor—Application Note 108, May 1974.

2) A. Feller, H. P. Kaupp, and J. J. Digiacomo, *"Crosstalk And Reflections In High Speed Digital Systems,"* proceedings—Fall Joint Computer Conference, pp. 511–525, 1965

3) R. V. Balakrishnan, *"Bus Optimizer,"* National Semiconductor—Application Note 259, April 1981

4) David Montgomery, *"Borrowing RF Techniques For Digital Design,"* Computer Design, pp. 207–217, May 1982

5) R. V. Balakrishnan, *"Eliminating Crosstalk Over Long Distance Busing,"* Computer Design, pp. 155–162, March 1982

National Semiconductor

DS3667 TRI-STATE® Bidirectional Transceiver

General Description

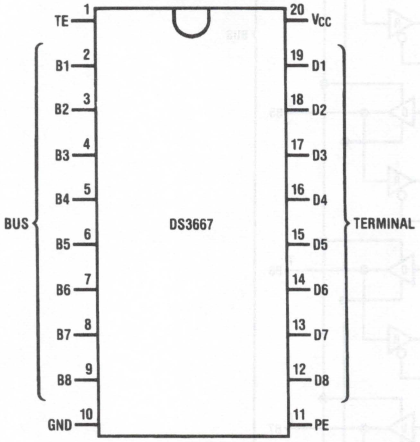
The DS3667 is a high-speed Schottky 8-channel bidirectional transceiver designed for digital information and communication systems. Pin selectable totem-pole/open collector outputs are provided at all driver outputs. This feature, together with the Dumb Mode which puts both driver and receiver outputs in TRI-STATE at the same time, means higher flexibility of system design. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. A power up/down protection circuit is included at all outputs to provide glitch-free operation during V_{CC} power up or down.

Features

- 8-channel bidirectional non-inverting transceivers
- Bidirectional control implemented with TRI-STATE output design
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- Pin selectable totem-pole/open collector outputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- Power up/down protection (glitch-free)
- Dumb Mode capability

Connection Diagram

Dual-In-Line Package



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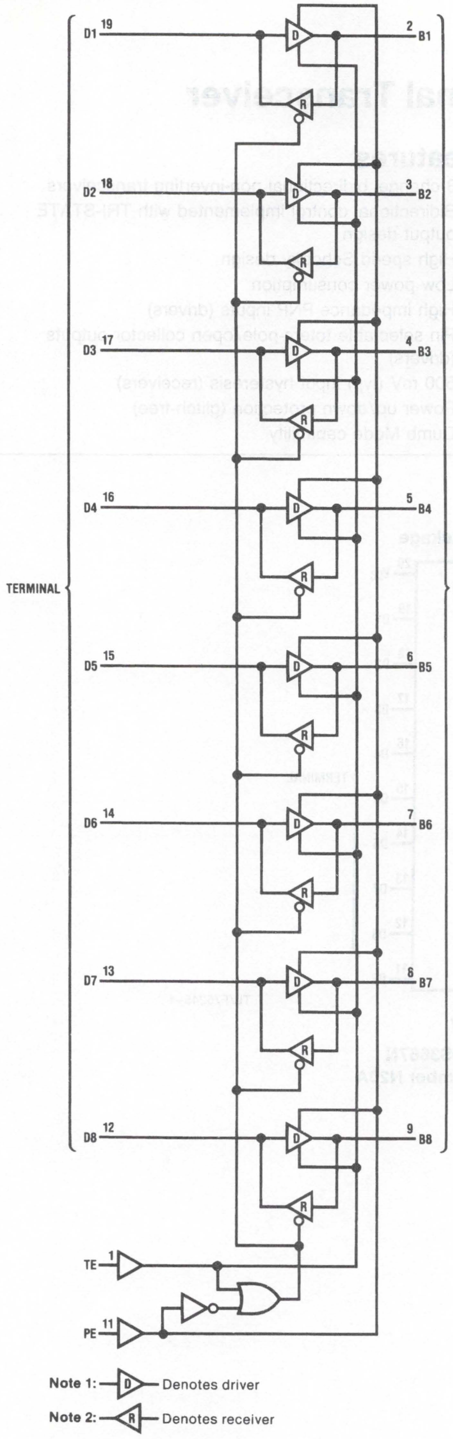
Top View

Order Number DS3667N
See NS Package Number N20A

Logic Diagram


D1 19
2 B1
D2 18
3 B2
D3 17
4 B3
D4 16
5 B4
D5 15
6 B5
D6 14
7 B6
D7 13
8 B7
D8 12
9 B8
TERMINAL
BUS
D
R
TE 1
PE 11
Note 1:
Denotes driver
Note 2:
Denotes receiver

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Functional Truth Table

Control Input Level		Data Transceivers		
TE	**PE**	**Mode**	**Bus Port**	**Terminal Port**
H	H	T	Totem-Pole Output	Input
H	L	T	Open Collector Output	Input
L	H	R	Input	Output
L	L	D	TRI-STATE	TRI-STATE

H: High Level Input
L: Low Level Input
T: Transmitting Mode
R: Receiving Mode
D: Dumb Mode

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1832 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA		−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus		400	500		mV
V_{OH}	High Level Output Voltage	Terminal	$I_{OH} = -800$ µA	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA	2.5	3.4		
V_{OL}	Low Level Output Voltage	Terminal	$I_{OL} = 16$ mA		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA		0.4	0.5	
I_{IH}	High Level Input Current	TE, PE	$V_I = 5.5V$		0.2	100	µA
			$V_I = 2.7V$		0.1	20	
		Terminal and Bus	$V_I = 4V$			200	
I_{IL}	Low Level Input Current	Terminal and TE, PE	$V_I = 0.5V$		−10	−100	µA
		Bus			−0.4	−1.0	mA
I_{OS}	Short Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)	−15	−35	−75	mA
		Bus		−50	−120	−200	
I_{CC}	Supply Current		Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$		75	100	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$		65	90	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 0V$, $V_I = 0V$, f = 10 kHz (Note 5)		20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This parameter is guaranteed by design. It is not a tested parameter.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $+70°C$ (Note 1)

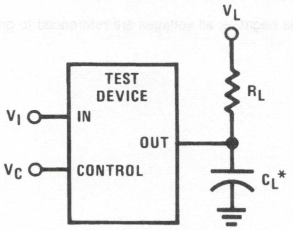
Symbol	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	$V_L = 2.3V$ $R_L = 38.3\Omega$ $C_L = 30\ pF$ *(Figure 1)*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	$V_L = 5.0V$ $R_L = 240\Omega$ $C_L = 30\ pF$ *(Figure 2)*		15	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	ns
t_{PZH}	Output Enable Time to High Level	TE (Notes 2 and 3)	Bus	$V_I = 3.0V$ $V_L = 0V$ $R_L = 480\Omega$ $C_L = 15\ pF$ *(Figure 1)*		19	30	ns
t_{PHZ}	Output Disable Time to High Level					15	20	ns
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$ $V_L = 2.3V$ $R_L = 38.3\Omega$ $C_L = 15\ pF$ *(Figure 1)*		24	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Enable Time to High Level	TE, PE (Notes 2 and 3)	Terminal	$V_I = 3.0V$ $V_L = 0V$ $R_L = 3\ k\Omega$ $C_L = 15\ pF$ *(Figure 1)*		19	35	ns
t_{PHZ}	Output Disable Time to High Level					17	25	ns
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$ $V_L = 5V$ $R_L = 280\Omega$ $C_L = 15\ pF$ *(Figure 1)*		27	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Pull-Up Enable Time	PE (Notes 2 and 3)	Bus	$V_I = 3V$ $V_L = 0V$ $R_L = 480\Omega$ $C_L = 15\ pF$ *(Figure 1)*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	ns

Note 1: All typical values are for $T_A = 25°C$, $V_{CC} = 5V$.

Note 2: Refer to Functional Truth Table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations

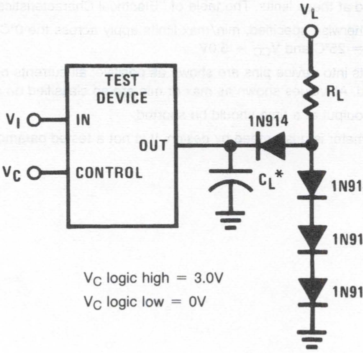


TL/F/5245-3

V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V
V_C logic low = 0V

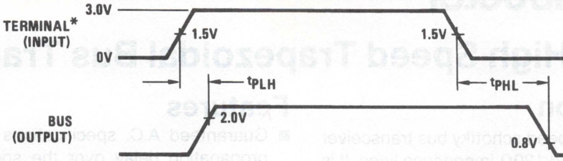
TL/F/5245-4

*C_L includes jig and probe capacitance

FIGURE 2

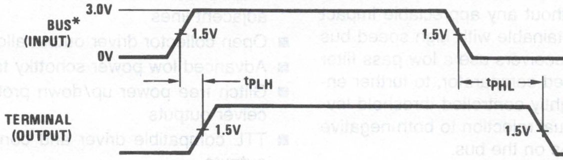
Switching Waveforms

Transmit Propagation Delays


3.0V
TERMINAL*
(INPUT)
0V
1.5V
1.5V
tPLH
tPHL
BUS
(OUTPUT)
2.0V
0.8V

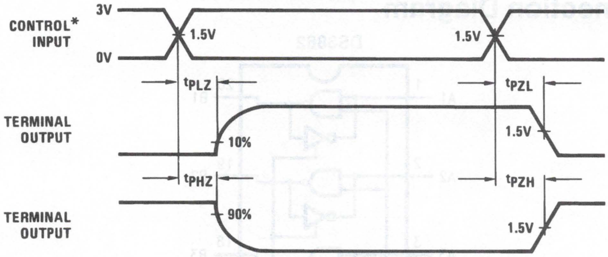
TL/F/5245–5

Receive Propagation Delays


3.0V
BUS*
(INPUT)
0V
1.5V
1.5V
tPLH
tPHL
TERMINAL
(OUTPUT)
1.5V
1.5V

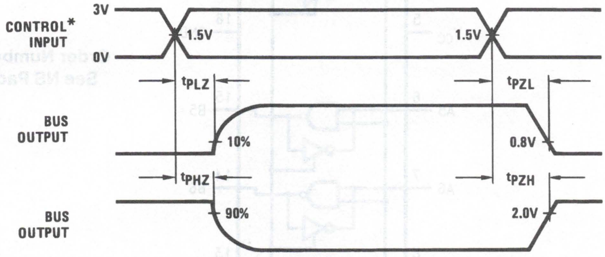
TL/F/5245–6

Terminal Enable/Disable Times


3V
CONTROL*
INPUT
0V
1.5V
1.5V
tPLZ
tPZL
TERMINAL
OUTPUT
10%
1.5V
tPHZ
tPZH
TERMINAL
OUTPUT
90%
1.5V

TL/F/5245–7

Bus Enable/Disable Times


3V
CONTROL*
INPUT
0V
1.5V
1.5V
tPLZ
tPZL
BUS
OUTPUT
10%
0.8V
tPHZ
tPZH
BUS
OUTPUT
90%
2.0V

TL/F/5245–8

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

National Semiconductor

PRELIMINARY

DS3862 Octal High Speed Trapezoidal Bus Transceiver

General Description

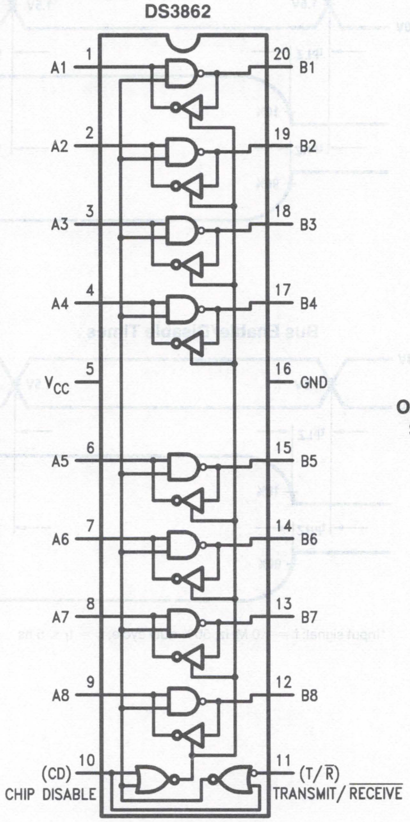
The DS3862 is an octal high speed schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 9 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends.

Features

- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level and respond symmetrically to positive and negative going pulses
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs, and receiver outputs
- Control logic is the same as the DS3896

Logic and Connection Diagram



Order Number DS3862J or DS3862N
See NS Package Number J20A or N20A

TL/F/8539-1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	5.5V
Power Dissipation	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs:						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	$An = V_{CC}$			1	mA
I_{IH}	Logical "1" Input Current	An = 2.4V			40	μA
I_{IL}	Logical "0" Input Current	An = 0.4V		−1	−1.6	mA
I_{IL}	CD & $T/\overline{R}$ Logical "0" Input Current	$CD = T/\overline{R} = 0.4V$		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input						
V_{OLB}	Low Level Bus Voltage	$An = T/\overline{R} = 2V$, Ibus = 100 mA		0.6	0.9	V
I_{IHB}	Logical "1" Bus Current	An = 0.8V, Bn = 4V, V_{CC} = 5.25V and 0V		10	100	μA
I_{ILB}	Logical "0" Bus Current	An = 0.8V, Bn = 0V, V_{CC} = 5.25V and 0V			100	μA
V_{TH}	Input Threshold	V_{CC} = 5V	1.5	1.7	1.9	V
Receiver Output						
V_{OH}	Logical "1" Output Voltage	Bn = 0.9V, I_{oh} = − 400μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	Bn = 4V, I_{ol} = 16 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 0.9V	−40	−70	−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V		90	135	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

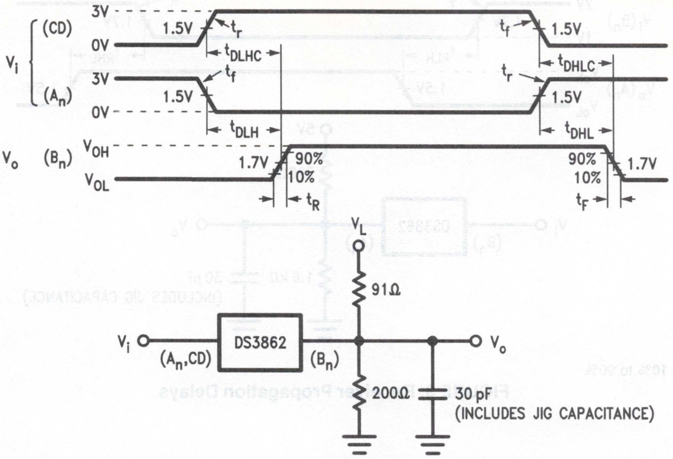
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Switching Characteristics $0^\circ C \le T_A \le 70^\circ C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, $T/\overline{R}$ = 2.0V, VL = 5V (*Figure 1*)		12	20	ns
t_{DHL}				12	20	ns
t_{DLHC}	CD to Bn	An = $T/\overline{R}$ = 2.0V, VL = 5V, (*Figure 1*)		12	20	ns
t_{DHLC}				15	25	ns
t_{DLHT}	$T/\overline{R}$ to Bn	VCI = An, VC = 5V, CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 91Ω, RL2 = 200Ω, VL = 5V (*Figure 2*)		20	30	ns
t_{DHLT}				25	40	ns
t_R	Driver Output Rise Time	CD = 0.8V, $T/\overline{R}$ = 2V, VL = 5V (*Figure 1*)	4	9	20	ns
t_F	Driver Output Fall Time		4	9	20	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, $T/\overline{R}$ = 0.8V (*Figure 3*)		15	25	ns
t_{RHL}				15	25	ns
t_{RLZC}	CD to An	Bn = 2.0V, $T/\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V (*Figure 4*)		15	25	ns
t_{RZLC}		Bn = 2.0V, $T/\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6K, VL = 5V (*Figure 4*)		10	20	ns
t_{RHZC}		Bn = 0.8V, $T/\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*)		5	10	ns
t_{RZHC}		Bn = 0.8V, $T/\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6K, CL = 30 pF (*Figure 4*)		8	15	ns
t_{RLZT}	$T/\overline{R}$ to An	VCI = Bn, VC = 3.4V, RC = 39Ω CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		20	30	ns
t_{RZLT}		VCI = Bn, VC = 3.4V, RC = 39Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6K, CL = 30 pF (*Figure 2*)		30	45	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 39Ω CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		5	10	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 39Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6K, CL = 30 pF (*Figure 2*)		10	20	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 5*)	9	12		ns

Note: NC means open

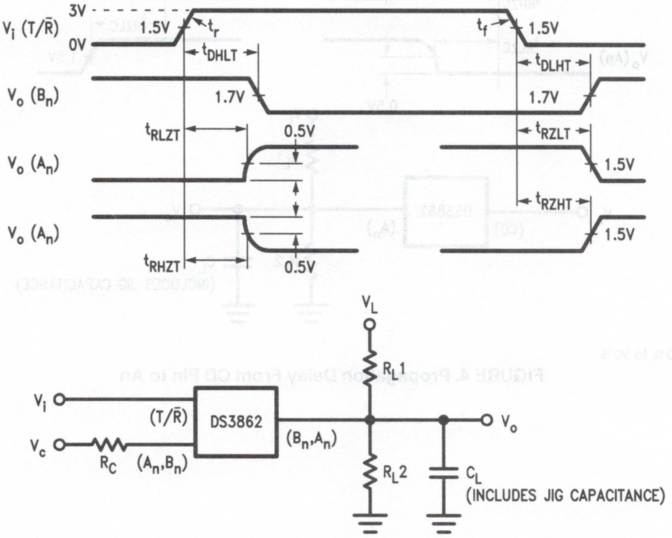
Switching Waveforms


3V
V_i (CD)
0V
3V
(A_n)
0V
1.5V
t_r
t_DLHC
t_f
1.5V
t_DLH
t_f
1.5V
t_DHLC
t_r
1.5V
t_DHL
V_o (B_n)
V_OH
V_OL
1.7V
90%
10%
t_R
90%
10%
1.7V
t_F
V_L
91Ω
V_i
(A_n,CD)
DS3862
(B_n)
V_o
200Ω
30 pF
(INCLUDES JIG CAPACITANCE)

TL/F/8539-2

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 1. Driver Propagation Delays

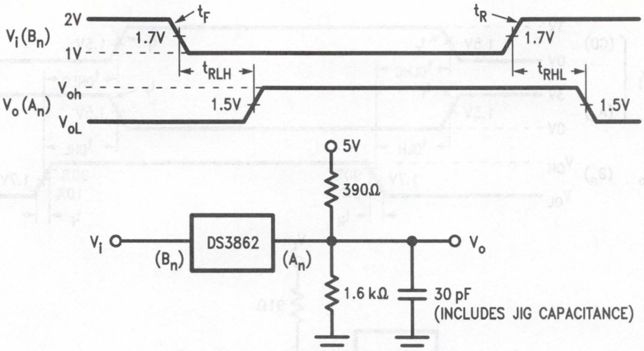

3V
V_i (T/R̄)
0V
1.5V
t_r
t_f
1.5V
t_DHLT
t_DLHT
V_o (B_n)
1.7V
1.7V
t_RLZT
0.5V
t_RZLT
V_o (A_n)
1.5V
t_RZHT
V_o (A_n)
1.5V
t_RHZT
0.5V
V_L
R_L1
V_i
(T/R̄)
DS3862
V_c
R_C
(A_n,B_n)
(B_n,A_n)
V_o
R_L2
C_L
(INCLUDES JIG CAPACITANCE)

TL/F/8539-3

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. Propagation Delay From T/R̄ Pin to An or Bn.

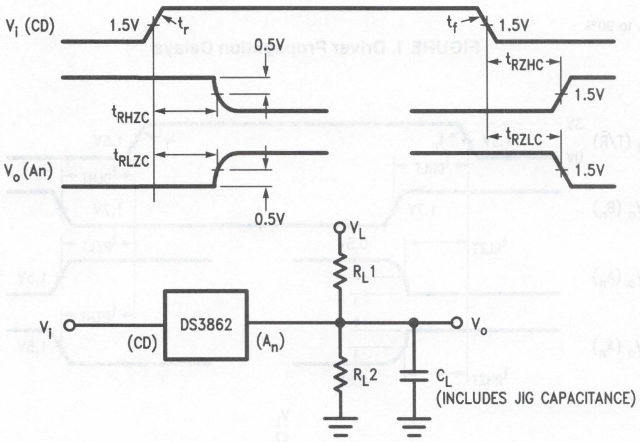
Switching Waveforms (Continued)


2V
t_F
$V_i(B_n)$
1.7V
1V
t_{RLH}
V_{oh}
$V_o(A_n)$
1.5V
V_{oL}
t_R
1.7V
t_{RHL}
1.5V
5V
390Ω
V_i
DS3862
(B_n)
(A_n)
V_o
1.6 kΩ
30 pF
(INCLUDES JIG CAPACITANCE)

TL/F/8539-4

Note: $t_R = t_F \leq 10$ ns from 10% to 90%

FIGURE 3. Receiver Propagation Delays

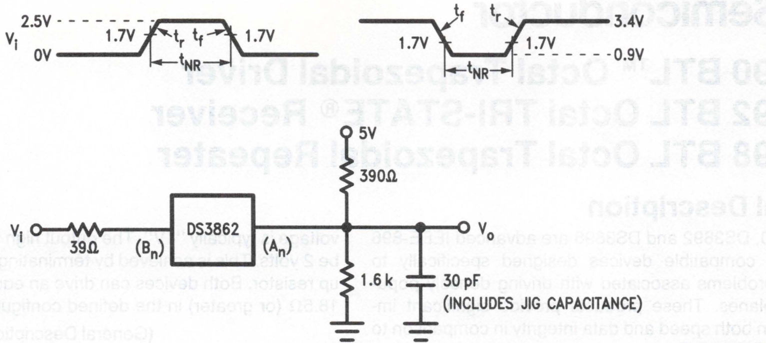

V_i (CD)
1.5V
t_r
0.5V
t_{RHZC}
t_{RLZC}
V_o (An)
0.5V
t_f
1.5V
t_{RZHC}
1.5V
t_{RZLC}
1.5V
V_L
R_L1
V_i
DS3862
(CD)
(A_n)
V_o
R_L2
C_L
(INCLUDES JIG CAPACITANCE)

TL/F/8539-5

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. Propagation Delay From CD Pin to An

Switching Waveforms (Continued)

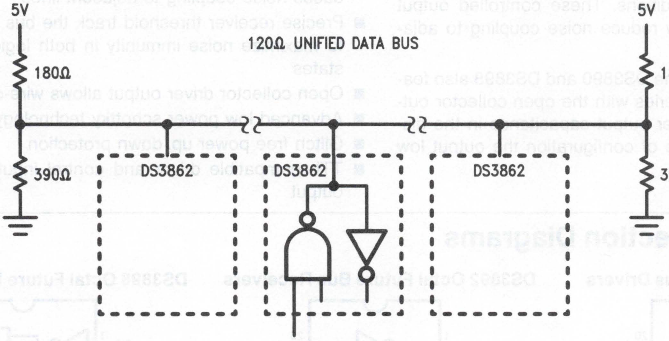

2.5V
V_i
0V
1.7V
t_r
t_f
1.7V
t_{NR}
t_f
t_r
3.4V
1.7V
1.7V
0.9V
t_{NR}
5V
390Ω
V_i
39Ω
DS3862
(B_n)
(A_n)
V_o
1.6 k
30 pF
(INCLUDES JIG CAPACITANCE)

TL/F/8539–6

Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 5. Receiver Noise Immunity: No Response at Output Input Waveform.

Typical Application


5V
180Ω
390Ω
120Ω UNIFIED DATA BUS
DS3862
DS3862
DS3862
5V
180Ω
390Ω

TL/F/8539–7

National Semiconductor

PRELIMINARY

DS3890 BTL™ Octal Trapezoidal Driver
DS3892 BTL Octal TRI-STATE® Receiver
DS3898 BTL Octal Trapezoidal Repeater

General Description

The DS3890, DS3892 and DS3898 are advanced IEEE-896 Future Bus compatible devices designed specifically to overcome problems associated with driving densely populated backplanes. These products provide significant improvement in both speed and data integrity in comparison to conventional bus drivers and receivers. Their low output capacitance, low voltage swing and noise immunity features make them ideal for driving low impedance busses with minimum power dissipation.

The DS3890 and DS3898 feature open collector outputs that generate precise trapezoidal waveforms with typical rise and fall times of 6 ns which are relatively independent of capacitive loading conditions. These controlled output characteristics significantly reduce noise coupling to adjacent lines.

To minimize bus loading, the DS3890 and DS3898 also feature a schottky diode in series with the open collector outputs that isolates the driver output capacitance in the disabled state. With this type of configuration the output low voltage is typically "1V". The output high level is intended to be 2 volts. This is achieved by terminating the bus with a pull up resistor. Both devices can drive an equivalent DC load of 18.5Ω (or greater) in the defined configuration.

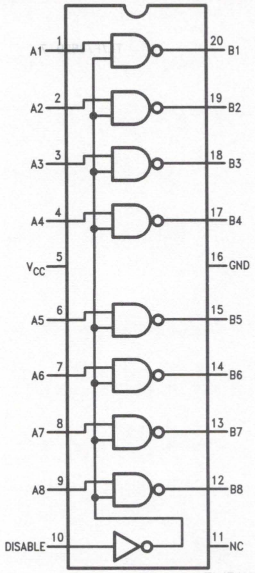
(General Description to be continued)

Features

- Meets IEEE 896 Future Bus Specification
- Driver output capacitance less than 5 pF
- 1 volt bus signal reduces power consumption
- Trapezoidal driver waveforms (t_r, t_f, typically 6 ns) reduces noise coupling to adjacent lines
- Precise receiver threshold track the bus logic high level to maximize noise immunity in both logic high ahd low states
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection
- TTL compatible driver and control inputs and receiver output

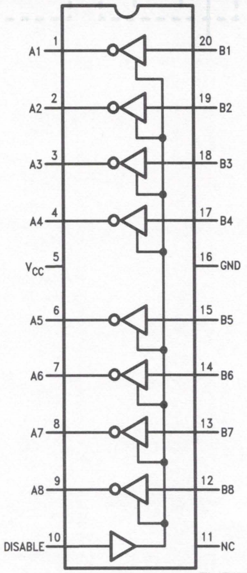
Logic and Connection Diagrams

DS3890 Octal Future Bus Drivers


A1 1
A2 2
A3 3
A4 4
VCC 5
A5 6
A6 7
A7 8
A8 9
DISABLE 10
20 B1
19 B2
18 B3
17 B4
16 GND
15 B5
14 B6
13 B7
12 B8
11 NC

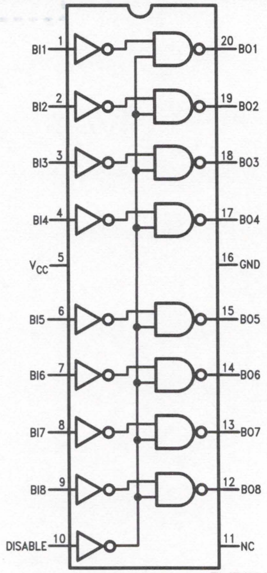
TL/F/8700–1

DS3892 Octal Future Bus Receivers


A1 1
A2 2
A3 3
A4 4
VCC 5
A5 6
A6 7
A7 8
A8 9
DISABLE 10
20 B1
19 B2
18 B3
17 B4
16 GND
15 B5
14 B6
13 B7
12 B8
11 NC

TL/F/8700–2

DS3898 Octal Future Bus Repeaters


BI1 1
BI2 2
BI3 3
BI4 4
VCC 5
BI5 6
BI6 7
BI7 8
BI8 9
DISABLE 10
20 BO1
19 BO2
18 BO3
17 BO4
16 GND
15 BO5
14 BO6
13 BO7
12 BO8
11 NC

TL/F/8700–3

Order Numbers DS3890J, N, DS3892J, N or DS3898J, N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Temperature (T_A)	0	70	°C

DS3890 Electrical Characteristics (Notes 2 and 3)

DRIVER AND CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL} An	V_{CC} = Max V_{IN} = 0.4V		−1	−1.6	mA
I_{IL} Dis	V_{CC} = Max V_{IN} = 0.4V		−180	−400	µA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	µA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
DRIVER OUTPUT					
V_{OL}	V_{CC} = Min R_L = 18.5Ω	0.75	1.0	1.2	V
I_{OH}	V_{CC} = Max V_{OUT} = 2V	−20	10	100	µA
I_O	V_{CC} = 0V V_{OUT} = 2V			100	µA
I_{IL}	V_{CC} = Max V_{OUT} = 0.75V		−100	−250	µA
I_{CC} Low	V_{CC} = Max		50	80	mA
I_{CC} High				TBD	mA

DS3892 Electrical Characteristics (Notes 2 and 3)

CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = Max V_{IN} = 0.4V		−180	−400	µA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	µA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
RECEIVER					
V_{OL}	V_{CC} = Min I_{OL} = 16 mA		0.35	0.5	V
V_{OH}	V_{CC} = Min I_{OH} = −400 µA	2.4	3.2		V
I_{OS}	V_{CC} = Max V_{OUT} = 0V	−40	−70	−100	mA
V_{TH} Rec	V_{CC} = 5V	1.5	1.55	1.6	V
I_{IH} Rec	V_{CC} = Max V_{IN} = 2V		10	100	µA
I_I Rec	V_{CC} = 0V V_{IN} = 2V			100	µA
I_{IL} Rec	V_{CC} = Max V_{IN} = 0.75V			TBD	µA
I_{CC} Low	V_{CC} = Max			80	mA
I_{CC} High				TBD	mA

DS3898 Electrical Characteristics (Notes 2 and 3)

Symbol	Conditions	Min	Typ	Max	Units
CONTROL INPUTS					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	$V_{CC}=\text{Max}$ $V_{IN}=0.4V$		−180	−400	μA
I_{IH}	$V_{CC}=\text{Max}$ $V_{IN}=2.4V$			40	μA
I_I	$V_{CC}=\text{Max}$ $V_{IN}=5.25V$			1	mA
V_{CL}	$V_{CC}=\text{Min}$ $I_{IN}=-12$ mA		−0.9	−1.5	V
RECEIVER INPUT					
V_{TH} Rec	$V_{CC}=5V$	1.5	1.55	1.6	V
I_{IH} Rec	$V_{CC}=\text{Max}$ $V_{IN}=2V$		10	100	μA
I_I Rec	$V_{CC}=0V$ $V_{IN}=2V$			100	μA
I_{IL} Rec	$V_{CC}=\text{Max}$ $V_{IN}=0.75V$			TBD	μA
DRIVER OUTPUT					
V_{OL}	$V_{CC}=\text{Min}$ $R_L=18.5\Omega$	0.75	1.0	1.2	V
I_{OH}	$V_{CC}=\text{Max}$ $V_{OUT}=2V$	−20	10	100	μA
I_O	$V_{CC}=0V$ $V_{OUT}=2V$			100	μA
I_{IL}	$V_{CC}=\text{Max}$ $V_{OUT}=0.75V$		−100	−250	mA
I_{CC} Low	$V_{CC}=\text{Max}$		90	135	mA
I_{CC} High				TBD	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis and apply to the full operating temperature and V_{CC} range.

Note 3: All typical values are $V_{CC}=5V$, $T_A=25°C$.

DS3890 Switching Characteristics *(Figure 1)*

($0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	An to Bn		9	15	ns
T_{dHL}			9	15	ns
T_{dLH}	Dis to Bn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns

DS3892 Switching Characteristics *(Figures 2, 3 and 4)*

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bn to An		12	18	ns
T_{pHL}			10	18	ns
T_{dLZ}	Dis to An		10	18	ns
T_{dZL}			8	15	ns
T_{dHZ}			4	8	ns
T_{dZH}			7	12	ns
TNR	Receiver noise rejection	3	6		ns

DS3898 Switching Characteristics (*Figures 4* and *5*)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bi to BOn		20	30	ns
T_{dHL}			20	30	ns
T_{dLH}	Dis to BOn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns
TNR	Receiver noise rejection	3	6		ns

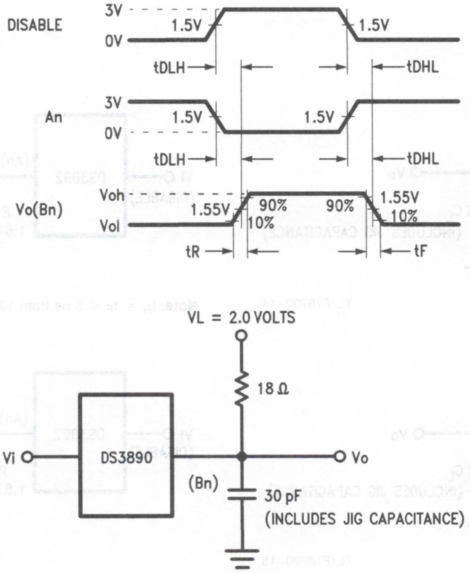
General Descriptions (Continued)

The DS8982 and DS3898 receiver inputs incorporate a low pass filter in conjunction with high speed comparator to further enhance the noise immunity. Both devices provide equal rejection to both positive and negative noise pulses (typically 6 ns) on the bus.

The DS3890 features TTL compatible inputs while both the DS3892 and DS3898 inputs are BTL compatible. The control inputs on all devices are TTL compatible.

BTL "Backplane Transceiver Logic" is a new logic signaling method developed by IEEE P896 Future Bus Standards Committee. This standard was adopted to enhance the performance of Backplane Busses. BTL compatible bus interface circuits feature low capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard overcomes some of the fundamental limitations of TTL bus transceivers in heavily loaded backplane bus applications. Devices designed to this standard provide significant improvements in switching speed and data integrity.

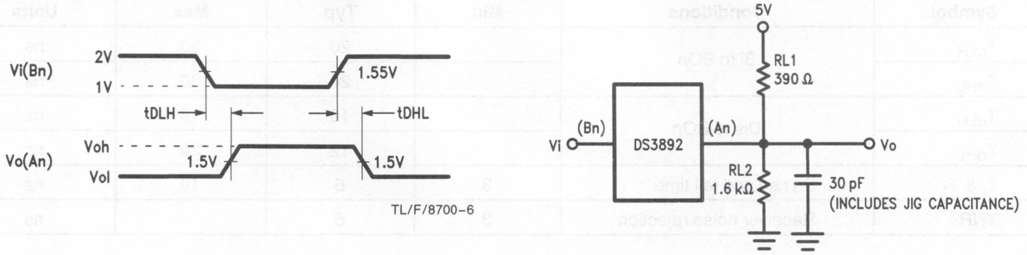
AC Switching Waveforms


DISABLE
3V
0V
1.5V
1.5V
tDLH
tDHL
An
3V
0V
1.5V
1.5V
tDLH
tDHL
Vo(Bn)
Voh
Vol
1.55V
1.55V
90%
10%
90%
10%
tR
tF
TL/F/8700-4
VL = 2.0 VOLTS
18 Ω
Vi
DS3890
Vo
(Bn)
30 pF
(INCLUDES JIG CAPACITANCE)
TL/F/8700-5

Note: $t_R = t_F < 10$ ns from 10% to 90%

FIGURE 1
Driver Propagation Delays

AC Switching Waveforms (Continued)

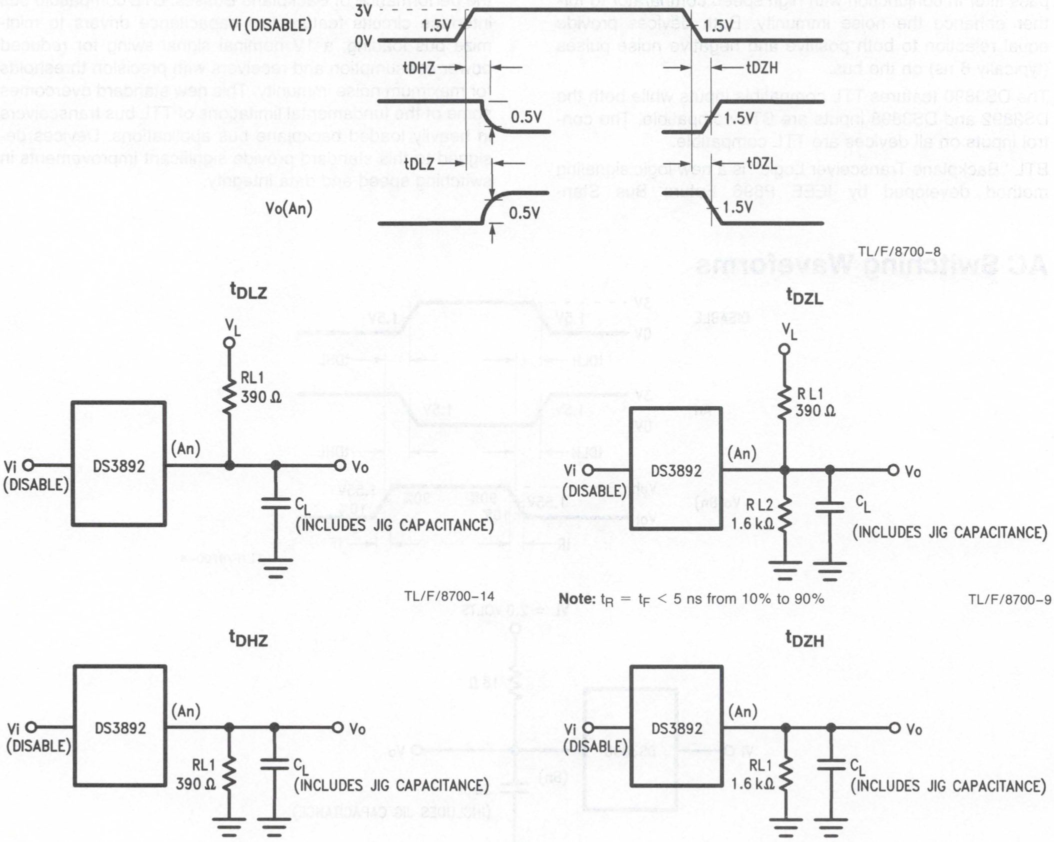

Vi(Bn)
2V
1V
1.55V
tDLH
tDHL
Voh
Vo(An)
Vol
1.5V
1.5V
5V
RL1
390 Ω
(Bn)
Vi
DS3892
(An)
Vo
RL2
1.6 kΩ
30 pF
(INCLUDES JIG CAPACITANCE)

TL/F/8700-6

Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700-7

FIGURE 2. Receiver Propagation Delays


Vi (DISABLE)
3V
0V
1.5V
1.5V
tDHZ
tDZH
0.5V
1.5V
tDLZ
tDZL
Vo(An)
0.5V
1.5V
tDLZ
VL
RL1
390 Ω
Vi
(DISABLE)
DS3892
(An)
Vo
CL
(INCLUDES JIG CAPACITANCE)
tDZL
VL
RL1
390 Ω
Vi
(DISABLE)
DS3892
(An)
Vo
RL2
1.6 kΩ
CL
(INCLUDES JIG CAPACITANCE)
tDHZ
Vi
(DISABLE)
DS3892
(An)
Vo
RL1
390 Ω
CL
(INCLUDES JIG CAPACITANCE)
tDZH
Vi
(DISABLE)
DS3892
(An)
Vo
RL1
1.6 kΩ
CL
(INCLUDES JIG CAPACITANCE)

TL/F/8700-8

TL/F/8700-14

Note: $t_R = t_F < 5$ ns from 10% to 90%

TL/F/8700-9

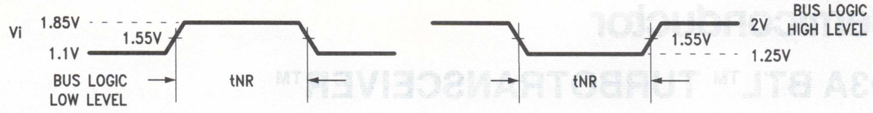
TL/F/8700-15

TL/F/8700-16

Note: $t_R = t_F < 5$ ns from 10% to 90%

FIGURE 3. Propagation Delay from Disable Pin to An

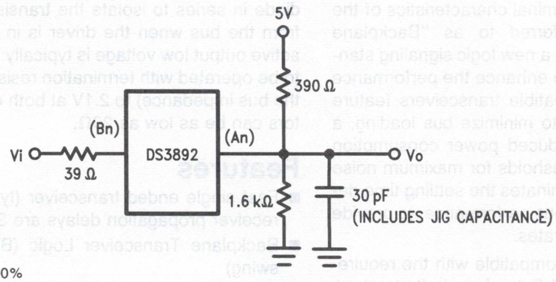
AC Switching Waveforms (Continued)


Vi
1.85V
1.55V
1.1V
BUS LOGIC LOW LEVEL
tNR
tNR
1.55V
2V
BUS LOGIC HIGH LEVEL
1.25V

High

Low

TL/F/8700-10

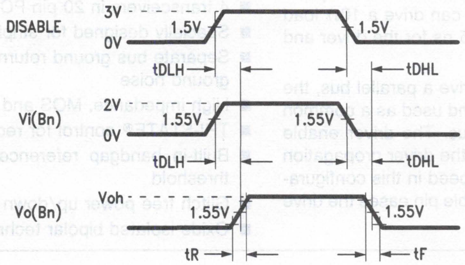

5V
390 Ω
(Bn)
(An)
Vi
DS3892
Vo
39 Ω
1.6 kΩ
30 pF
(INCLUDES JIG CAPACITANCE)

Note: $t_R = t_F < 2$ ns from 10% to 90%

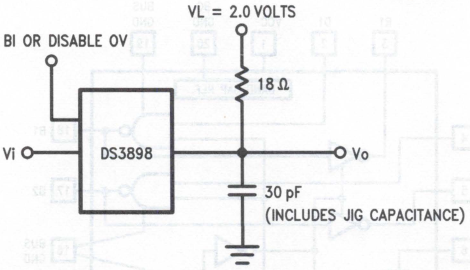
TL/F/8700-11

FIGURE 4

Receiver Noise Immunity: "No Response at Output" Input Waveforms


DISABLE
3V
0V
1.5V
1.5V
tDLH
tDHL
2V
Vi(Bn)
0V
1.55V
1.55V
tDLH
tDHL
Voh
Vo(Bn)
1.55V
1.55V
tR
tF

TL/F/8700-12


VL = 2.0 VOLTS
BI OR DISABLE OV
18 Ω
Vi
DS3898
Vo
30 pF
(INCLUDES JIG CAPACITANCE)

Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700-13

FIGURE 5

Repeater Propagation Delays

National Semiconductor

PRELIMINARY

DS3893A BTL™ TURBOTRANSCEIVER™

General Description

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The bus terminal characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the proposed IEEE 896 Futurebus draft standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL Transceivers but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and 5 ns for the receiver.

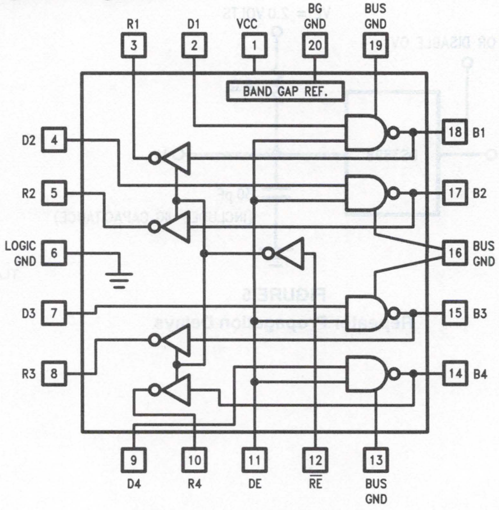
When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2.1V at both ends. Each of the resistors can be as low as 20Ω.

Features

- Fast single ended transceiver (typical driver enable and receiver propagation delays are 3.5 ns and 5 ns)
- Backplane Transceiver Logic (BTL™) levels (1V logic swing)
- Less than 5 pF bus-port capacitance
- Drives densely loaded backplanes with equivalent load impedances down to 10Ω
- Complies with IEEE 896 Futurebus standard
- 4 transceivers in 20 pin PCC package
- Specially designed for stripline backplanes
- Separate bus ground returns for each driver to minimize ground noise
- High impedance, MOS and TTL compatible inputs
- TRI-STATE® control for receiver outputs
- Built-in bandgap reference provides accurate receiver threshold
- Glitch free power up/down protection on all outputs
- Oxide isolated bipolar technology

Connection and Logic Diagram



TL/F/8698-1

Order Number DS3893AV
See NS Package Number V20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.5V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Driver Output Receiver Input Clamp Current	±15 mA
Power Dissipation at 70°C	900 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.0	2.2	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics (Notes 2, 3 and 4) $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (DE, $\overline{RE}$, Dn)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_I	Input Leakage Current	DE = $\overline{RE}$ = Dn = V_{CC}			100	μA
I_{IH}	Input High Current	DE = $\overline{RE}$ = Dn = 2.5V			20	μA
I_{IL}	Dn Input Low Current	Dn = 0.5V, DE = V_{CC} = Max			−200	μA
	DE Input Low Current	DE = 0.5V, Dn = V_{CC} = Max			−700	μA
	$\overline{RE}$ Input Low Current	$\overline{RE}$ = 0.5V, V_{CC} = Max			−100	μA
V_{CL}	Input Diode Clamp Voltage	$I_{clamp} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage	Dn = DE = V_{IH} *(Figure 2)* $R_T = 10\Omega$, $V_T = 2.2V$	0.75	1.0	1.2	V
		Dn = DE = V_{IH} *(Figure 2)* $R_T = 18.5\Omega$, $V_T = 2.14$	0.75	1.0	1.1	V
I_{ILB}	Output Bus Current (Power On)	Dn = DE = 0.8V, V_{CC} = Max Bn = 0.75V	−250		100	μA
I_{IHB}	Output Bus Current (Power Off)	Dn = DE = 0.8V, V_{CC} = 0V Bn = 1.2V			100	μA
V_{OCB}	Driver Output Positive Clamp	V_{CC} = Max or 0V, Bn = 1 mA	1.9		2.9	V
		V_{CC} = Max or 0V, Bn = 10 mA	2.3		3.2	V
V_{OHB}	Output High Bus Voltage	V_{CC} = Max, Dn = 0.8V *(Figure 2)* $V_T = 2.0V$, $R_T = 10\Omega$	1.90			V
V_{TH}	Receiver Input Threshold		1.475	1.55	1.625	V
RECEIVER OUTPUT: (Rn)						
V_{OH}	Voltage Output High	Bn = 1.2V, $I_{oh} = -3$ mA, $\overline{RE}$ = 0.8V	2.5V			V
V_{OL}	Voltage Output Low	Bn = 2V, $I_{ol} = 6$ mA, $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OZ}	TRI-STATE Leakage	$V_o = 2.5V$, $\overline{RE}$ = 2V			20	μA
		$V_o = 0.5V$, $\overline{RE}$ = 2V			−20	μA
I_{OS}	Output Short Circuit Current (Note 5)	Bn = 1.2V, $V_o = 0V$ $\overline{RE}$ = 0.8V, V_{CC} = Max	−80	−120	−200	mA
I_{CC}	Supply Current	Dn = DE = $\overline{RE}$ = V_{IH}, V_{CC} = Max		70	95	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

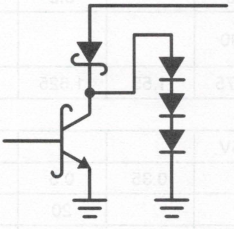
Note 4: Unused inputs should not be left floating. Tie unused inputs to either V_{CC} or GND thru a resistor.

Note 5: Only one output at a time should be shorted.

Switching Characteristics $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

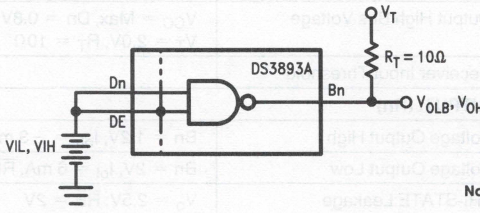
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER: (*Figures 3* and *6*)						
t_{PHL}	Driver Input to Output	$V_T = 2V$ $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1	3.5	7	ns
t_{PLH}	Driver Input to Output	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1	3.5	7	ns
t_r	Output Rise time	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1	2	5	ns
t_f	Output Fall Time	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1	2	5	ns
t_{skew}	Skew Between Drivers in Same Package	(Note 1)		1		ns
DRIVER ENABLE: (*Figures 3* and *6*)						
t_{PHL}	Enable Delay	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, Dn = 3V	1	3.5	7	ns
t_{PLH}	Disable Delay	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, Dn = 3V	1	3.5	7	ns
RECEIVER: (*Figures 4* and *7*)						
t_{PHL}	Receiver Input to Output	$C_L = 50$ pF, $\overline{RE}$ = DE = 0.3V, S3 Closed	2	5	8	ns
t_{PLH}	Receiver Input to Output	$C_L = 50$ pF, $\overline{RE}$ = DE = 0.3V, S3 Open	2	5	8	ns
t_{skew}	Skew Between Receivers in Same Package	(Note 1)		1		ns
RECEIVER ENABLE: (*Figures 5* and *8*)						
t_{ZL}	Receiver Enable to Output Low	$C_L = 50$ pF, $R_L = 500$, DE = 0.3V S2 Open Bn = 2V	2	6	12	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 50$ pF, $R_L = 500$, DE = 0.3V S1 Open Bn = 1V	2	5	12	ns
t_{LZ}	Receiver Disable From Output Low	$C_L = 50$ pF, $R_L = 500$, DE = 0.3V S2 Open Bn = 2V	1	5	8	ns
t_{HZ}	Receiver Disable From Output High	$C_L = 50$ pF, $R_L = 500$, DE = 0.3V S1 Open Bn = 1V	1	4	8	ns

Note 1: t_D and t_R skew is an absolute value, defined as differences seen in propagation delays between each of the drivers or receivers in the same package of the same delay, V_{CC}, temperature and load conditions.



TL/F/8698-12

FIGURE 1. Equivalent Bus Output

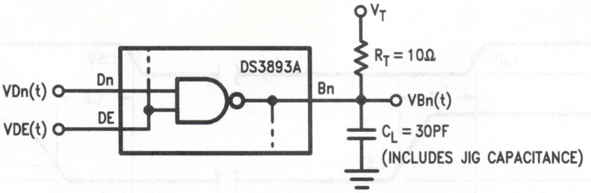


Note: n = 1, 2, 3, 4

TL/F/8698-2

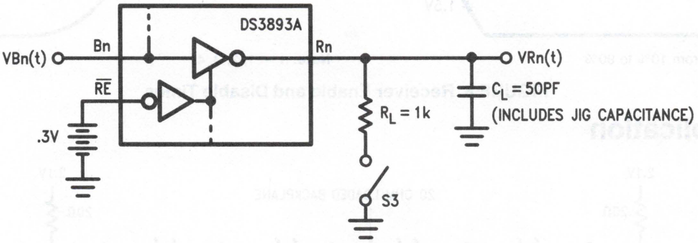
FIGURE 2. Driver Output Voltage

AC Test Circuits


VT
RT = 10Ω
DS3893A
VDn(t)
Dn
Bn
VBn(t)
VDE(t)
DE
CL = 30PF
(INCLUDES JIG CAPACITANCE)

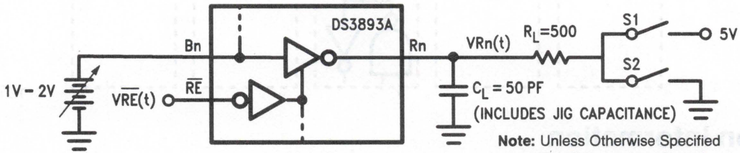
TL/F/8698-3

FIGURE 3


DS3893A
VBn(t)
Bn
Rn
VRn(t)
RE
CL = 50PF
(INCLUDES JIG CAPACITANCE)
RL = 1k
.3V
S3

TL/F/8698-4

FIGURE 4

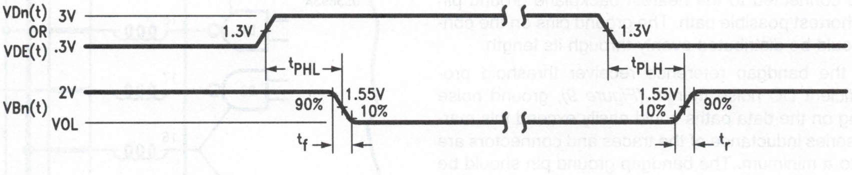

DS3893A
Bn
Rn
VRn(t)
RL=500
S1
5V
S2
1V - 2V
RE
VRE(t)
CL = 50 PF
(INCLUDES JIG CAPACITANCE)

Note: Unless Otherwise Specified
The Switches are Closed

TL/F/8698-5

FIGURE 5

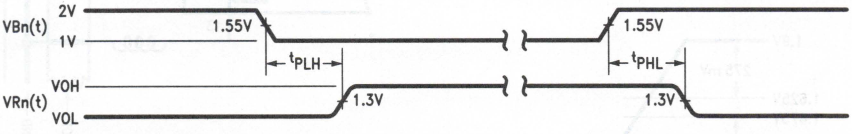
Switching Time Waveforms


VDn(t)
OR
VDE(t)
3V
.3V
1.3V
1.3V
tPHL
tPLH
2V
VBn(t)
VOL
90%
1.55V
10%
1.55V
10%
90%
tf
tr

$t_R = t_F \leq 4ns$ FROM 10% TO 90%

TL/F/8698-6

FIGURE 6. Driver Propagation Delay

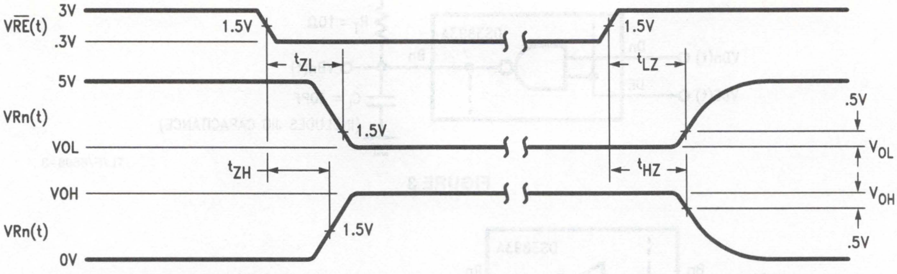

2V
VBn(t)
1V
1.55V
1.55V
tPLH
tPHL
VOH
VRn(t)
VOL
1.3V
1.3V

$t_R = t_F \leq 4ns$ FROM 10% TO 90%

TL/F/8698-7

FIGURE 7. Receiver Propagation Delay

Switching Time Waveforms (Continued)


VRE(t)
3V
.3V
1.5V
1.5V
tZL
tLZ
5V
VRn(t)
1.5V
VOL
.5V
VOL
tZH
tHZ
VOH
VOH
VRn(t)
1.5V
0V
.5V

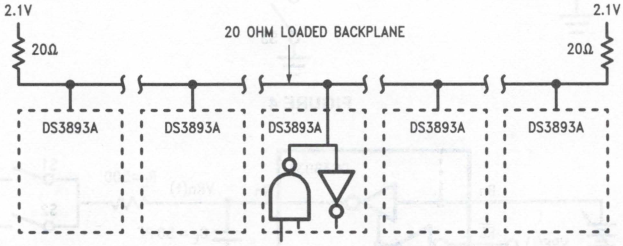
Note: $t_R = t_F \leq 4$ ns From 10% to 90%

Note: n = 1, 2, 3, 4

TL/F/8698-8

FIGURE 8. Receiver Enable and Disable Times

Typical Application


2.1V
20Ω
20 OHM LOADED BACKPLANE
2.1V
20Ω
DS3893A
DS3893A
DS3893A
DS3893A
DS3893A

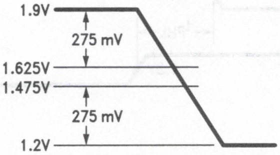
TL/F/8698-9

Application Information

Due to the high current and very high speed capability of the TURBOTRANSCEIVER's driver output stage, circuit board layout and bus grounding are critical factors that affect the system performance.

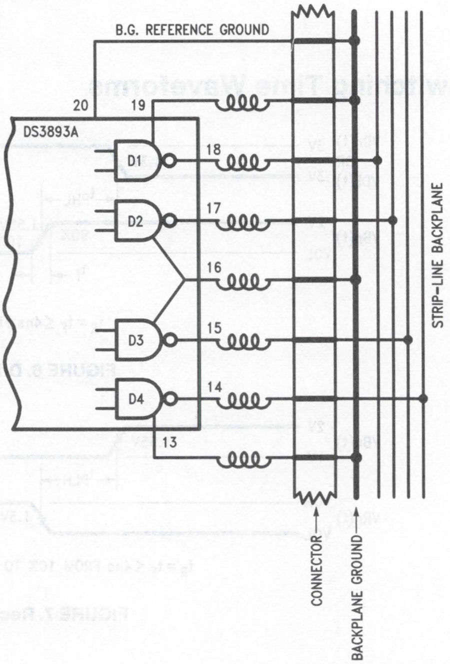
Each of the TURBOTRANSCEIVER's bus ground pins should be connected to the nearest backplane ground pin with the shortest possible path. The ground pins on the connector should be distributed evenly through its length.

Although the bandgap reference receiver threshold provides sufficient DC noise margin *(Figure 9)*, ground noise and ringing on the data paths could easily exceed this margin if the series inductance of the traces and connectors are not kept to a minimum. The bandgap ground pin should be returned to the connector through a separate trace that does not carry transient switching currents. The transceivers should be mounted as close as possible to the connector. It should be noted that even one inch of trace can add a significant amount of ringing to the bus signal.


1.9V
275 mV
1.625V
1.475V
275 mV
1.2V

TL/F/8698-10

FIGURE 9. Noise Margin


B.G. REFERENCE GROUND
20
19
DS3893A
D1
18
D2
17
16
D3
15
D4
14
13
STRIP-LINE BACKPLANE
CONNECTOR
BACKPLANE GROUND

TL/F/8698-11

FIGURE 10

National Semiconductor

DS3896/DS3897 Futurebus Trapezoidal™ Transceivers

General Description

These advanced IEEE-896 Futurebus compatible transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

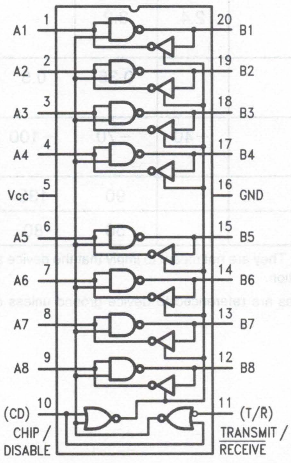
These signalling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL™).

Features

- 8 bit DS3896 transceiver provides high package density
- 4 bit DS3897 transceiver provides separate driver input and receiver output pins
- Meets IEEE 896 Futurebus specification
- BTL compatible
- Less than 5 pF output capacitance for minimal bus loading
- 1 Volt bus signal swing reduces power consumption
- Trapezoidal driver waveforms (t_r, t_f ≅ 6 ns typical) reduce noise coupling to adjacent lines
- Temperature insensitive receiver thresholds track the bus logic high level to maximize noise immunity in both high and low states
- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs and receiver outputs

Logic and Connection Diagrams

DS3896N, J



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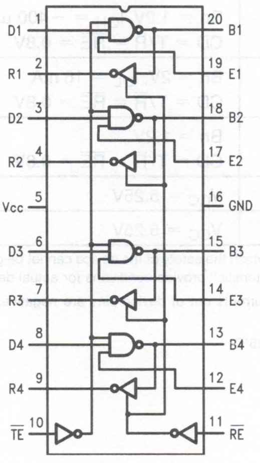
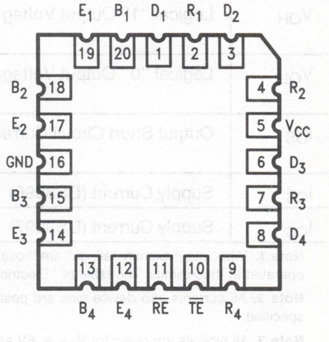
DS3897N, J



TL/F/8510-2

DS3897V



TL/F/8510-11

Order Number DS3896J, N, DS3897J, N or DS3897V
See NS Package Number J20A, N20A or V20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Power Dissipation at 70°C N Package	1480 mW
J Package	1250 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Termination Voltage	1.90	2.10	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics: (Note 2 and 3) ($0°C \leq T_A \leq 70°C$, $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs: (An, Dn, En, CD, $T/\overline{R}$, $\overline{RE}$, $\overline{TE}$)						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	$An = Dn = En = V_{CC}$			1	mA
I_{IH}	Logical "1" Input Current	$An = Dn = En = 2.4V$			40	μA
I_{IL}	Logical "0" Input Current	$An = Dn = En = 0.4V$		−1	−1.6	mA
I_{ILC}	Logical "0" Input Current	$CD = T/\overline{R} = \overline{RE} = \overline{TE} = 0.4V$		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input: (Bn)						
V_{OLB}	Low Level Bus Voltage	$An = Dn = En = T/\overline{R} = 2V$, $VL = 2V$ $RL = 18.5\Omega$, $CD = \overline{TE} = 0.8V$ (*Figure 1*)	0.75	1.0	1.2	V
I_{IHB}	Maximum Bus Current (Power On)	$An = Dn = En = 0.8V$, $V_{CC} = 5.25V$ $Bn = 2V$		10	100	μA
I_{ILB}	Maximum Bus Current (Power Off)	$An = Dn = En = 0.8V$, $V_{CC} = 0V$ $Bn = 2V$			100	μA
V_{TH}	Receiver Input Threshold	$V_{CC} = 5V$	1.5	1.55	1.60	V
Receiver Output: (An, Rn)						
V_{OH}	Logical "1" Output Voltage	$Bn = 1.2V$, $I_{OH} = -400\ \mu A$ $CD = T/\overline{R} = \overline{RE} = 0.8V$	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	$Bn = 2V$, $I_{OL} = 16\ mA$ $CD = T/\overline{R} = \overline{RE} = 0.8V$		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$Bn = 1.2V$ $CD = T/\overline{R} = \overline{RE} = 0.8V$	−40	−70	−100	mA
I_{CC}	Supply Current (DS3896)	$V_{CC} = 5.25V$		90	135	mA
I_{CC}	Supply Current (DS3897)	$V_{CC} = 5.25V$		50	80	mA

Note 1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristic" provide conditions for actual device operation.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. All typicals are given for $V_{CC} = 5V$ and $T_a = 25°C$.

DS3896 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, $T/\overline{R}$ = 2.0V, VL = 2V (*Figure 2*)	5	9	15	ns
t_{DHL}			5	9	15	ns
t_{DLHC}	CD to Bn	An = $T/\overline{R}$ = 2.0V, VL = 2V (*Figure 2*)	5	10	18	ns
t_{DHLC}			5	12	20	ns
t_{DLHT}	$T/\overline{R}$ to Bn	VCI = An, VC = 5V, (*Figure 5*) CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 18Ω, RL2 = NC, VL = 2V	5	15	25	ns
t_{DHLT}			5	22	35	ns
t_R	Driver Output Rise Time	CD = 0.8V, $T/\overline{R}$ = 2V, VL = 2V (*Figure 2*)	3	6	10	ns
t_F	Driver Output Fall Time		3	6	10	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, $T/\overline{R}$ = 0.8V (*Figure 3*)	5	12	18	ns
t_{RHL}			5	10	18	ns
t_{RLZC}	CD to An	Bn = 2.0V, $T/\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V (*Figure 4*)	5	10	18	ns
t_{RZLC}		Bn = 2.0V, $T/\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k, VL = 5V (*Figure 4*)	5	8	15	ns
t_{RHZC}		Bn = 0.8V, $T/\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*)	2	4	8	ns
t_{RZHC}		Bn = 0.8V, $T/\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF (*Figure 4*)	3	7	12	ns
t_{RLZT}	$T/\overline{R}$ to An	VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 5*)	8	14	20	ns
t_{RZLT}		VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6k, CL = 30 pF (*Figure 5*)	14	24	40	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 5*)	2	4	8	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6k, CL = 30 pF (*Figure 5*)	2	8	15	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 6*)	3	6		ns

Note: NC means open

DS3897 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified**)**

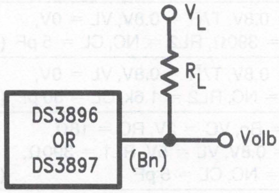
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	Dn, En to Bn	$\overline{TE}$ = 0.8V, $\overline{RE}$ = 2.0V, VL = 2V (*Figure 2*)	5	9	15	ns
t_{DHL}			5	9	15	ns
t_{DLHT}	$\overline{TE}$ to Bn	An = $\overline{RE}$ = 2.0V, VL = 2V, (*Figure 2*) RL1 = 18Ω, RL2 = NC, VL = 2V (*Figure 5*)	5	10	18	ns
t_{DHLT}			5	12	20	ns
t_R	Driver Output Rise Time	CD = 0.8V, $T/\overline{R}$ = 2V, VL = 2V (*Figure 2*)	3	6	10	ns
tF	Driver Output Fall Time		3	6	10	ns

DS3897 Switching Characteristics (Continued)

($0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Receiver:						
t_{RLH}	Bn to Rn	$\overline{TE}$ = 2.0V, $\overline{RE}$ = 0.8V (*Figure 3*)	5	10	18	ns
t_{RHL}			5	12	18	ns
t_{RLZR}	$\overline{RE}$ to Rn	Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 5 pF RL1 = 390Ω, RL2 = NC (*Figure 4*)	5	10	18	ns
t_{RZLR}		Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k (*Figure 4*)	5	8	15	ns
t_{RHZR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF(*Figure 4*)	2	4	8	ns
t_{RZHR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF(*Figure 4*)	3	7	12	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 6*)	3	6		ns
Driver plus Receiver:						
t_{DRLH}	Dn to Rn	$\overline{TE}$ = $\overline{RE}$ = 0.8V (*Figure 7*)	10	20	30	ns
t_{DRHL}			10	20	30	ns

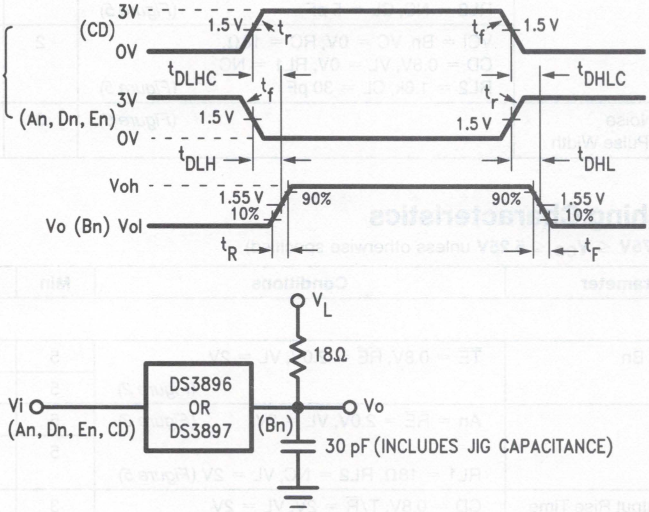
Note: NC means open



V_L
R_L
DS3896
OR
DS3897
(Bn)
Volb

TL/F/8510-3

FIGURE 1. Driver Output Low Voltage Test

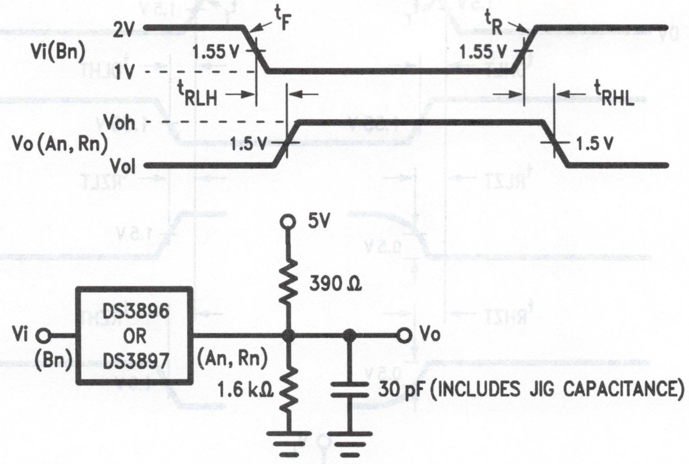


3V
(CD)
0V
Vi
3V
(An, Dn, En)
0V
1.5 V
t_r
t_f
1.5 V
t_{DLHC}
t_f
t_r
t_{DHLC}
1.5 V
1.5 V
t_{DLH}
t_{DHL}
Voh
1.55 V
10%
90%
90%
1.55 V
10%
Vo (Bn) Vol
t_R
t_F
V_L
18Ω
Vi
(An, Dn, En, CD)
DS3896
OR
DS3897
(Bn)
Vo
30 pF (INCLUDES JIG CAPACITANCE)

TL/F/8510-4

Note: $t_r = t_f \le 5$ ns from 10% to 90%

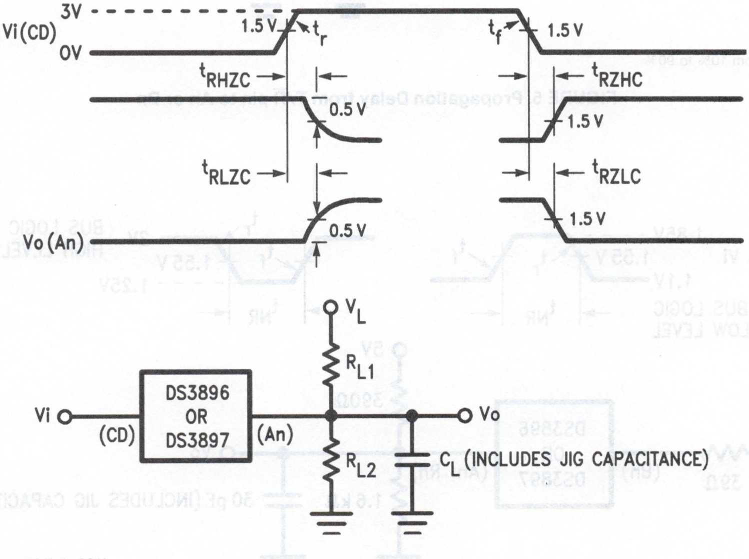
FIGURE 2. Driver Propagation Delays


2V
Vi(Bn)
1.55 V
1V
t_F
t_R
1.55 V
t_RLH
t_RHL
Voh
Vo (An, Rn)
1.5 V
Vol
1.5 V
5V
390 Ω
DS3896
OR
DS3897
Vi
(Bn)
(An, Rn)
Vo
1.6 kΩ
30 pF (INCLUDES JIG CAPACITANCE)

TL/F/8510–5

Note: $t_R = t_F \le 10$ ns from 10% to 90%

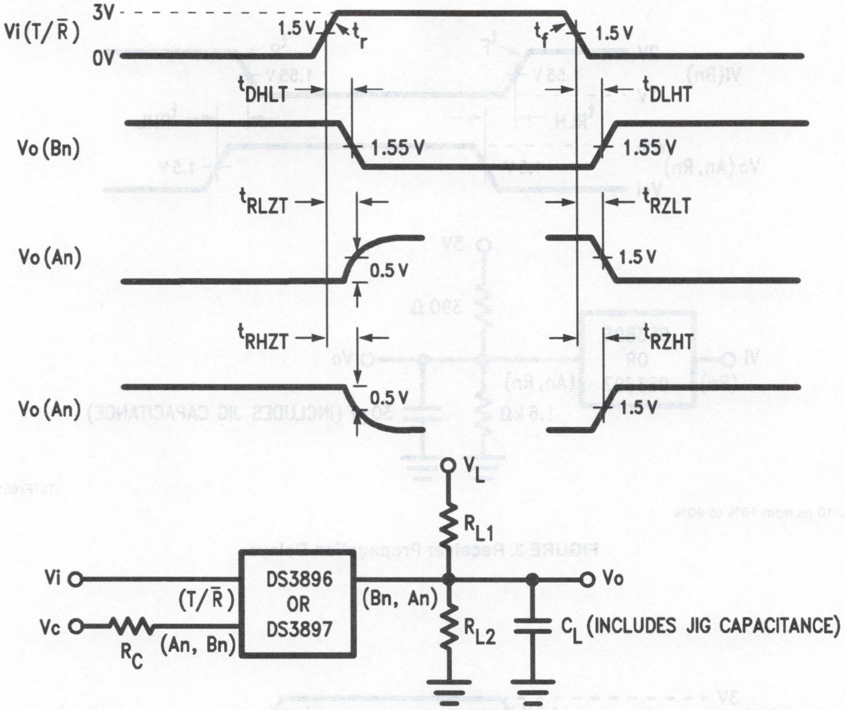
FIGURE 3. Receiver Propagation Delays


3V
Vi(CD)
0V
1.5 V
t_r
t_f
1.5 V
t_RHZC
t_RZHC
0.5 V
1.5 V
t_RLZC
t_RZLC
1.5 V
0.5 V
Vo (An)
V_L
R_L1
DS3896
OR
DS3897
Vi
(CD)
(An)
Vo
R_L2
C_L (INCLUDES JIG CAPACITANCE)

TL/F/8510–6

Note: $t_r = t_f \le 5$ ns from 10% to 90%

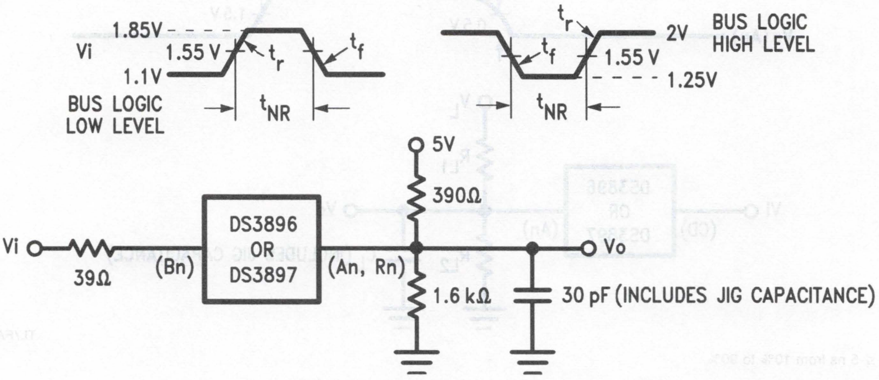
FIGURE 4. Propagation Delay from CD pin to An


3V
Vi (T/R̄)
0V
1.5 V
t_r
t_f
1.5 V
t_{DHLT}
t_{DLHT}
Vo (Bn)
1.55 V
1.55 V
t_{RLZT}
t_{RZLT}
Vo (An)
0.5 V
1.5 V
t_{RHZT}
t_{RZHT}
Vo (An)
0.5 V
1.5 V
V_L
R_{L1}
Vi
Vo
(T/R̄)
DS3896
OR
DS3897
(Bn, An)
Vc
R_C
(An, Bn)
R_{L2}
C_L (INCLUDES JIG CAPACITANCE)

TL/F/8510-7

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

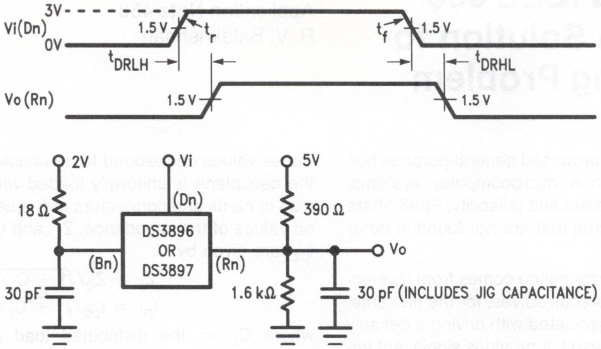
FIGURE 5. Propagation Delay from T/R̄ pin to An or Bn


1.85V
Vi
1.55 V
t_r
t_f
1.1V
BUS LOGIC
LOW LEVEL
t_{NR}
t_r
t_f
2V
BUS LOGIC
HIGH LEVEL
1.55 V
1.25V
t_{NR}
5V
390Ω
Vi
39Ω
(Bn)
DS3896
OR
DS3897
(An, Rn)
Vo
1.6 kΩ
30 pF (INCLUDES JIG CAPACITANCE)

TL/F/8510-8

Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 6. Receiver Noise Immunity: "No Response at Output" Input Waveforms

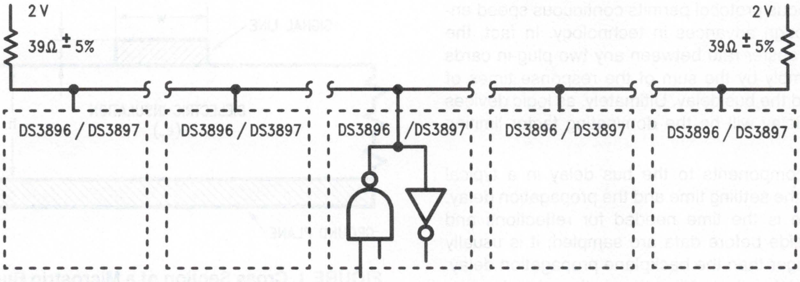

3V
Vi(Dn)
0V
1.5 V
t_r
t_f
1.5 V
t_{DRLH}
t_{DRHL}
Vo (Rn)
1.5 V
1.5 V
2V
Vi
5V
18 Ω
(Dn)
390 Ω
DS3896
OR
DS3897
(Bn)
(Rn)
Vo
30 pF
1.6 kΩ
30 pF (INCLUDES JIG CAPACITANCE)

TL/F/8510–9

Note: $t_r = t_f \leq 5\ \mu s$ from 10% to 90%

FIGURE 7. Driver Plus Receiver Delays

Typical Application


2 V
39Ω ± 5%
2 V
39Ω ± 5%
DS3896 / DS3897
DS3896 / DS3897
DS3896 / DS3897
DS3896 / DS3897
DS3896 / DS3897

TL/F/8510–10

The Proposed IEEE 896 Futurebus—A Solution to the Bus Driving Problem

National Semiconductor
Application Note 458
R. V. Balakrishnan

The IEEE 896 Futurebus is a proposed general-purpose bus standard for high-performance microcomputer systems. With a strong emphasis on speed and reliability, P896 offers a number of innovative features that are not found in other backplane buses.

A major contribution to its performance comes from its electrical specifications. The Futurebus solves, for the first time, the fundamental problems associated with driving a densely populated backplane—as a result, it provides significant improvements in both speed and data integrity. Two years of effort by the P896 committee have culminated in a deeper understanding of the physics of the backplane bus, leading to an ingenious solution to the bus problem.

Speed is probably the most important feature of any bus standard. This is especially true for the Futurebus, since its totally asynchronous protocol permits continuous speed enhancements through advances in technology. In fact, the maximum data transfer rate between any two plug-in cards is determined simply by the sum of the response times of the two cards and the bus delay. Ultimately, as logic devices get faster, bus delay will be the dominating factor limiting bus speed.

There are two components to the bus delay in a typical system, namely, the settling time and the propagation delay. The settling time is the time needed for reflections and crosstalk to subside before data are sampled; it is usually several times longer than the backplane propagation delay. As will be shown later, the settling time is the price the user pays for not driving the bus properly.

By using a special transceiver, the Futurebus not only eliminates the settling time delay but also reduces the propagation delay of the loaded backplane to provide maximum possible bus throughput.

THE PHYSICS OF THE BACKPLANE BUS

For high-speed signals the bus acts like a transmission line with an associated characteristic impedance and propagation delay whose unloaded values, Z_o and t_{po}, are given by

$$Z_o = \sqrt{L/C}$$

$$t_{po} = \ell \sqrt{L/C}$$

ℓ = length of the bus, L = distributed inductance per unit length, and C = distributed capacitance per unit length.(1)

These values can be calculated for a typical microstrip backplane *(Figure 1)* by means of the following equations:

$$Z_o = (87/\sqrt{\epsilon_r + 1.41}) \bullet \ln [5.98h/(0.8w + t)]\Omega$$

$$t_{po} = 1.017 \sqrt{0.475\, \epsilon_r + 0.67} \text{ ns/ft}$$

where ϵ_r = relative dielectric constant of the board material (typically $\epsilon_r = 4.7$ for fiberglass and w,h,t = the dimensions indicated in *Figure 1*. For a typical P896 backplane, t = 1.4 mils, w = 25 mils, h = ¹⁄₁₆ inch, and $\epsilon_r = 4.7$. By substituting these values we get $Z_o = 100\Omega$ and t_{po} = 1.7 ns/ft.

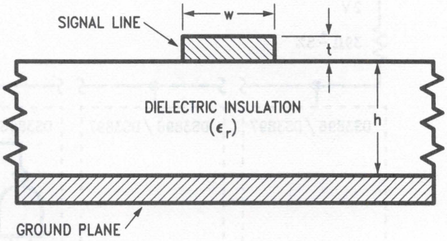
These values correspond to an *unloaded* backplane. When the backplane is uniformly loaded with the capacitance of plug-in cards and connectors at frequent intervals, the loaded values of the impedance, Z_L, and the propagation delay, t_{pL}, are given by

$$Z_L = Z_o/\sqrt{1 + C_L/C)}$$

$$t_{pL} = t_{po}/\sqrt{1 + C_L/C)}$$

where C_L = the distributed load capacitance per unit length.(1)

The distributed capacitance, C of the unloaded backplane can be measured in the lab. For our microstrip, it is 20 pF/ft. This does not include, however, the capacitance of the connectors mounted on the backplane and the associated plated-through holes, which can amount to 5 pF per card slot.



TL/F/8842-1

FIGURE 1. Cross Section of a Microstrip Bus Line

The loading capacitance of the plug-in card, however, is dominated by the loading capacitance of the transceiver, which can be 12–20 pF for TTL devices. Allowing another 3–5 pF for printed-circuit traces and the connector, the total loading per card slot can add up to 30 pF. For a system such as P896, which has 15 slots per foot, C_L = 450 pF/ft. Therefore,

$$Z_L = 100/\sqrt{1 + (450/20)} = 20\Omega$$

$$t_{pL} = 1.7 \sqrt{1 + (450/20)} = 8.25 \text{ ns/ft}$$

As can be seen above, the capacitive loading drastically alters both the impedance and the propagation delay of the bus. This reduces the bus throughput in two ways. One obvious impact is the increased propagation delay. But the not so obvious and even more serious problem is the reduced bus impedance, which is much harder to drive.

For example, to drive the loaded bus properly with a TTL driver which has a 3V nominal swing, the required drive current, I_D, must be

$$I_D = 3V/(Z_L/2)$$

The impedance seen by the driver is half of Z_L, since from a given board two transmission lines are being driven, one towards each terminator *(Figure 2)*. Therefore,

$$I_D = 3/(20/2) = 300 \text{ mA}$$

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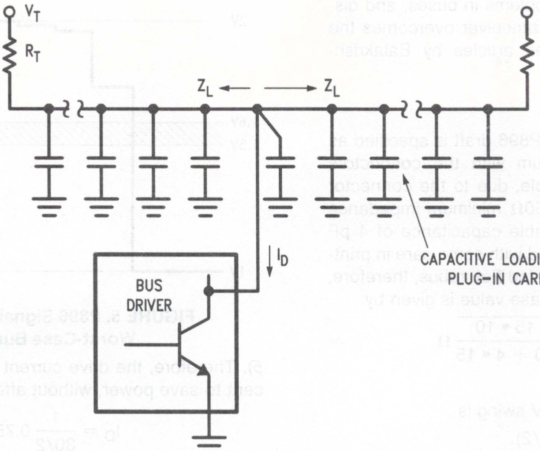

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FIGURE 2. The Loaded Bus—Each Driver Sees Two Loaded Line Impedances in Parallel ($Z_L \| Z_L = Z_{L/2}$).

This is much higher than the standard TTL's drive capability of 50 to 100 mA. *Figure 3* shows the effect of using a 50 mA driver, in this situation, on the bus waveform. The voltage swing on the bus has its first transition at 0.5V, the product of the drive current and $Z_L/2$. This value falls well below the upper threshold limit of the TTL receiver. Therefore, *several round-trip delays to the nearest termination are required for the waveform to cross the receiver threshold region.* In our example, one round-trip delay is $2t_{pL} = 16.5$ ns/ft. Therefore the settling times can exceed 100 ns even for relatively short buses. This long settling time drastically affects bus throughput at high speeds. Even worse, the voltage steps in the threshold region can cause multiple triggering in the cases of the clock and strobe signals.

One way to solve these problems is to use 100 mA drivers with precision receivers that have a narrow threshold region such that the first transition crosses well over the threshold. This technique is widely used for clock lines to avoid multiple triggering. Its use on data/address lines is limited because of the significantly higher power requirement arising from the large number of lines involved (32 address/data lines).

Even if power is not a limitation, switching to higher current drivers provides only a marginal improvement. The reason for this is quite simple. A higher current driver unfortunately has a higher output capacitance, which reduces the bus impedance further. This in turn requires an even higher current drive for proper operation.

The Futurebus Transceiver

A more elegant solution—one that is now a part of the P896 proposal—directly attacks the root of the problem, namely, the large output capacitance of the transceiver. By simply adding a Schottky diode in series with an open-collector driver output, the capacitance of the drive transistor is isolated by the small reverse-biased capacitance of the diode in the non-transmitting state *(Figure 4)*. The Schottky diode capacitance is typically less than 2 pF and is relatively independent of the drive current. Allowing for a receiver input capacitance of another 2 pF, the total loading of the Futurebus transceiver can be kept under 5 pF. The P896 draft specifies a maximum plug-in card capacitance of 10 pF to accommodate the 5 pF trace and connector capacitances.

In addition to reducing the loading on the bus, the Futurebus transceiver features several other enhancements over a conventional TTL transceiver that drastically reduce power consumption and improve system reliability.

A major portion of the power savings comes from a reduced voltage swing—1V—on the bus. Contrary to popular belief, the lower swing does not reduce crosstalk immunity (provided the receiver threshold is tightly controlled).(2) The induced crosstalk from other lines on the bus scales down with the amplitude of the signal transistion causing it. Consequently, if a line receiver has a precision threshold, the noise margin, expressed as a percentage of signal amplitude, remains the same, as does the crosstalk immunity. However, the absolute noise margin, with reference to a noise source external to the bus, does shrink linearly with amplitude. Fortunately, the low impedance and the relatively short length of the bus make this externally generated noise component insignificant in high-speed backplanes. Nevertheless, it is recommended that the backplane be shielded from strong noise sources external to the bus.

Noise Immunity and EMI

The Futurebus transceiver has a precision receiver threshold centered between the low and high bus levels of 1 and 2V, respectively *(Figure 5)*. Confined to a narrow region of ±3 percent ±50 mV), the threshold voltage tracks the bus high level to provide a maximum-percentage noise margin with respect to the low and high signal levels of the bus. In addition, to reduce crosstalk, which is proportional to di/dt, the driver features a trapezoidal output waveform with a 6 ns transition time. Moreover, the receiver incorporates a noise filter which selectively rejects crosstalk noise pulses of up to 8 ns in pulse width. These techniques, borrowed from the DS3662 trapezoidal bus transceiver from National Semiconductor, virtually eliminate crosstalk, thereby increasing system reliability by several orders of magnitude.

Detailed analyses of crosstalk problems in buses, and discussions of how the trapezoidal tranceiver overcomes the problems, can be found in three articles by Balakrishnan.(2–4)

DRIVE CURRENT

The backplane impedance in the P896 draft is specified as 50Ω minimum and 60Ω maximum with the connectors mounted. In our microstrip example, due to the connector and the plated-through holes, a 50Ω minimum impedance translates into a maximum allowable capacitance of 4 pF per slot. This can be easily attained with some care in printed-circuit board design. A fully loaded Futurebus, therefore, has an impedance whose worst-case value is given by

$$Z_{min} = 50/\sqrt{1 + \frac{15 \bullet 10}{20 + 4 \bullet 15}}\ \Omega$$

$$= 30\Omega$$

The drive current required for a 1V swing is

$$I_D = 1/(30/2)$$

However, with a precision receiver threshold it is possible for the driver to swing past the threshold with a comfortable margin even if the first step climbs to only 75 percent of the final amplitude under worst-case loading (see again *Figure 5*). Therefore, the drive current can be reduced by 25 percent to save power, without affecting performance:

$$I_D = \frac{1}{30/2}0.75 = 50\text{ mA}$$

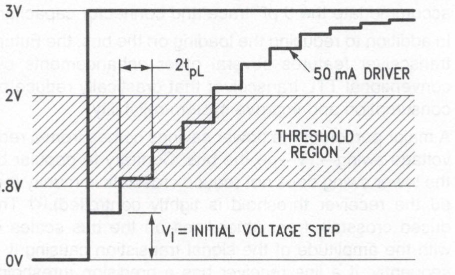

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FIGURE 3. TTL Bus Waveforms—50 mA Driver vs 300 mA Driver

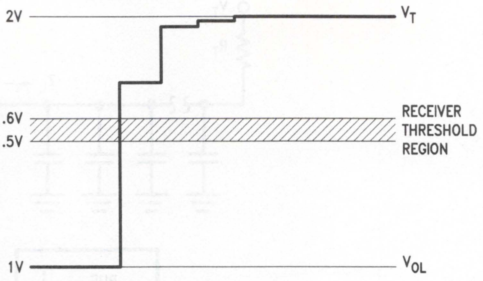

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FIGURE 5. P896 Signaling Levels and the Worst-Case Bus Waveform

At this current level, the power dissipated in the driver is low enough to allow eight to ten transceivers to be built into a single, narrow, dual-in-line plastic package.

National Semiconductor has two Futurebus transceivers, the DS3896 and the DS3897, that are now available in sample quantities. The DS3896 is an octal device with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. On the other hand, the DS3896 provides high package density for data/address lines.

Fabricated in an oxide-isolated bipolar process, these devices combine very high speed with large drive capability. The propagation delays are 8 ns typical for the driver and 10 ns typical for the receiver.

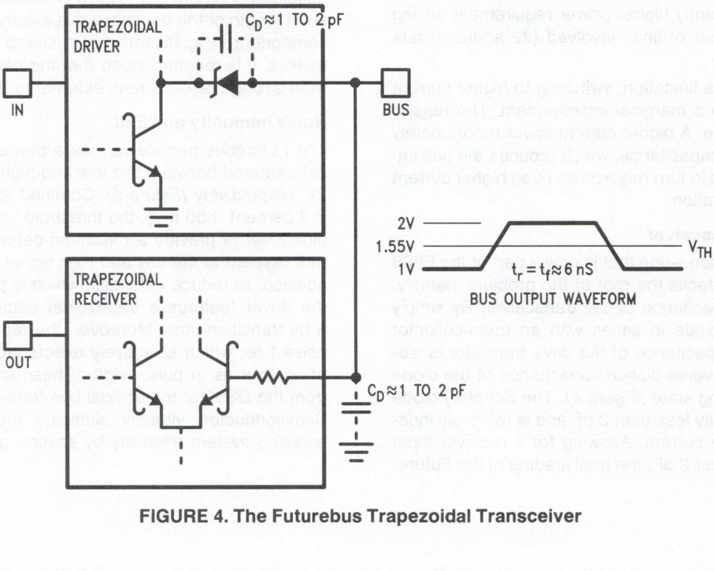

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FIGURE 4. The Futurebus Trapezoidal Transceiver

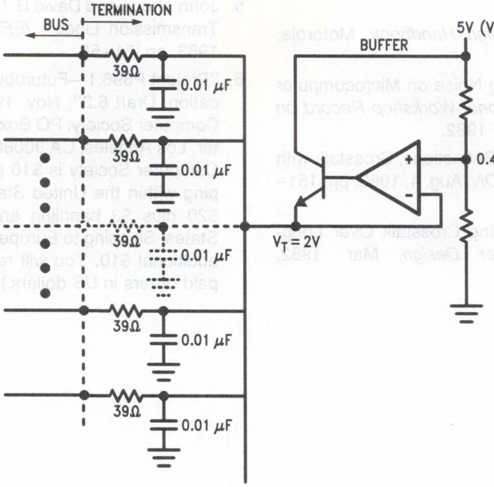

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FIGURE 6. The Futurebus Termination Circuit

OTHER HIGHLIGHTS

Bus Propagation Delay

There is an additional benefit resulting from reducing the capacitive loading on the bus. This benefit arises from the reduced propagation delay, which further improves the bus speed.

Recalculating the loaded propagation delay for the Futurebus transceiver yields

$$t_{PL} = t_{po}\sqrt{1 + (C_L/C)}$$
$$= 1.7\sqrt{1 + \frac{(10 + 4)15}{20}}$$
$$= 5.765 \text{ ns/ft}$$

This is a 30-percent improvement over the TTL example. It should be noted that this is the worst-case delay per foot and that the asynchronous nature of the Futurebus protocol will take full advantage of lower propagation delays in a typical system, either due to lower loading levels or due to the closer spacing of two plug-in boards that are in communication.

Termination

The drive current and the signal swing determine the termination resistors. If the drive current is derived properly, the termination will match the bus impedance under the given loading. For P896, the value of each of the two termination resistors, R_T, is

$$R_T = \left(\frac{1V}{50 \text{ mA}}\right) 2 = 40\Omega$$

This value is greater than the loaded impedance of the Futurebus, because the drive current is only 75 percent of that required for a full swing on the first transition. However, in a practical bus the impedance varies with various load conditions, and therefore the above termination value is a good compromise between the worst-case values of the bus impedances of 30 and 50Ω.

The P896 draft requires that the bus be terminated at both ends, with a single resistor of 39Ω connected to an active voltage source of 2V *(Figure 6)*. This arrangement has a significantly lower power dissipation than a "Thévenin-equivalent" two-resistor termination connected to ground and the 5V rail. The 2V source is derived from the 5V supply using a potential divider followed by a buffer; the source can be shared among all the bus lines as long as it is properly bypassed for alternating current close to each resistor. The termination voltage is deliberately made to follow the 5V supply variation in order to keep the receiver threshold at the center of the bus swing with supply variations.

Wire-OR Glitch

One of the advantages of an open-collector bus is a wire-OR capability. This feature is fully exploited in the P896 bus, particularly in its sophisticated arbitration protocol and broadcast mechanism. Unfortunately, due to the fundamental nature of transmission lines, wire-ORing on the bus can cause erroenous glitches having pulse widths of up to the round-trip delay of the bus. The analysis of the wire-OR glitch is covered well by Theus and Gustavson.(5)

To overcome the wire-OR glitch, the broadcast acknowledge lines (AI* and DI*) and the three arbitration control lines are required to have integrators at the output of the receiver capable of rejecting pulses having widths of up to the maximum round-trip delay of the bus.

And More

Geographic addressing and live insertion and withdrawal capability are some of the other highlights of the Futurebus.

The reader is encouraged to read the draft proposal,(6) and the article by Theus and Borrill in this issue, for more details.

The electrical specification of P896 is based on a thorough knowledge of backplane operation. A combination of theoretical analysis and bench measurements has been used to create an electrically clean bus environment. Significant improvements have been made in favor of higher performance—at the expense of only a slight increase in today's cost and complexity—to assure a long design lifetime for the standard. The result is a proposed standard that has the performance, in terms of both speed and reliability, to justify the name, "Futurebus".

ACKNOWLEDGEMENT

I would like to thank Paul Borrill for his help and encouragement in finding this solution to the bus driving problem.

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Timing Analysis of Synchronous and Asynchronous Busses

National Semiconductor
Application Note 514
David Hawley and R.V. Balakrishnan

ABSTRACT

This paper presents detailed examples of bus timing calculations for both synchronous and asynchronous busses, showing that bus throughput can be maximized by taking into account the characteristics and limitations of the transceiver technology being used. Based on these examples, a performance analysis of the currently available high speed bus interface technologies is made in terms of their maximum attainable transfer rate on both types of backplane busses. The results show that the use of a faster transceiver, as judged by its data sheet, doesn't necessarily result in a faster bus.

INTRODUCTION

In order to derive the highest possible throughput from a backplane bus, a careful analysis and optimization of timing parameters is essential. The maximum speed attainable at the physical level of the bus is a function of the transceiver technology, the electrical length of the bus, and the type of protocol, synchronous or asynchronous, being used. A clear understanding of the bus timing constraints lets the designer take best advantage of a given technology, such as TTL, ECL, or BTL (Backplane Transceiver Logic). Contrary to intuitive thinking, a faster transceiver will not always result in a faster bus. It can be shown through examples that greater bus transfer rates can be obtained by using specially designed bus transceivers, such as the BTL Trapezoidal, that at first glance may appear to be slower than the equivalent AS or FAST devices. These devices, in addition to improving bus bandwidth, also reduce crosstalk, ground noise, and system power requirements.

BUS PROPAGATION DELAY AND SETTLING TIME

Traditionally, system designers have used standard TTL devices to drive the backplane bus. Unfortunately, although TTL appears to provide fast rise and fall times, it cannot cleanly drive the capacitance of a loaded backplane or the resistance required for proper termination. BTL technology is a result of work that was done within the IEEE 896.1 Futurebus committee specifically to solve the problems of driving a backplane with transmission-line characteristics. By using a smaller voltage swing, lower capacitance drivers, and receivers with precision thresholds, BTL transceivers overcome the "bus driving problem."

Simply stated, the problem is one of driving a low impedance transmission line (*Figures 1* and *2)*. The capacitive loading of a bus due to TTL transceivers reduces its impedance from an unloaded value of 60–100Ω to a fully loaded impedance of less than 20Ω. A properly matched termination resistance would therefore require a current of over 300 mA in order to cleanly drive a 3V nominal TTL swing! Since most TTL drivers cannot supply this current, they must depend on reflections to build up the bus voltage to a DC level. This results in a settling-time penalty of one or more bus round-trip propagation delays on every signal transition, or 35 ns on a typical 20″ TTL bus.

The low output capacitance of BTL transceivers allows the total capacitive loading of a card in a backplane to be kept under 10 pF. This doubles the impedance of a loaded bus to almost 30Ω. BTL also specifies a reduced signal swing of 1V, which allows a properly terminated bus to be driven cleanly at under 75 mA. Consequently, there are no reflections, and the settling time is zero. A BTL driver can be guaranteed to cross the threshold of every receiver on the backplane with the incident edge of a signal wavefront.

The propagation delay of a bus is also a strong function of the capacitive loading. In the TTL case, the capacitive loading increases the signal propagation delay by a factor of 3 to 5 over an unloaded bus. In a 20″ bus, BTL can reduce this delay from a value of 13 ns in the TTL case to less than 9 ns, increasing the potential bus bandwidth significantly.

SYNCHRONOUS BUS TIMING

For our first example, let's consider burst data transfers on a synchronous bus. In many backplane systems, burst transfers provide the highest performance, because the overhead associated with the address cycle can be spread out over a number of data cycles. Although other types of transactions may be more complex and require more time (clock cycles), it is likely that many systems will be optimized for burst transfers.

In this example, we are making some simplifying assumptions which ignore some of the penalties associated with a general-purpose synchronous bus. One of these is that the entire interface is synchronized to the bus clock. In general, each card in a backplane will be running off of its own internal high-speed clock. This results in resynchronization metastability problems at both the master and slave interfaces, as well as a clock latency penalty of typically 50% of the clock period. We are also ignoring the return of status from the slave on each data transfer, by assuming all status can be generated before the data is clocked. This would not be true, for example, if parity had to be verified before the next data transfer could take place.

Clock Skew

In this example, the system clock is being distributed to each board through a clock line on the backplane. Since the clock line is being driven from a single point, the loaded capacitance on it is considerably less than on most other lines, and the settling time is typically zero, even in a TTL-based backplane. Due to the finite propagation delay across the bus, however, the clock edge still arrives at each board at different times, creating a relative edge inaccuracy commonly referred to as clock skew.

The worst-case skew can be cut in half by locating the clock source centrally on the backplane, rather than at one end. Additional clock skew will be introduced by the propagation delay differences in the receiver and logic gates that process the clock signal between boards. For a typical 20″

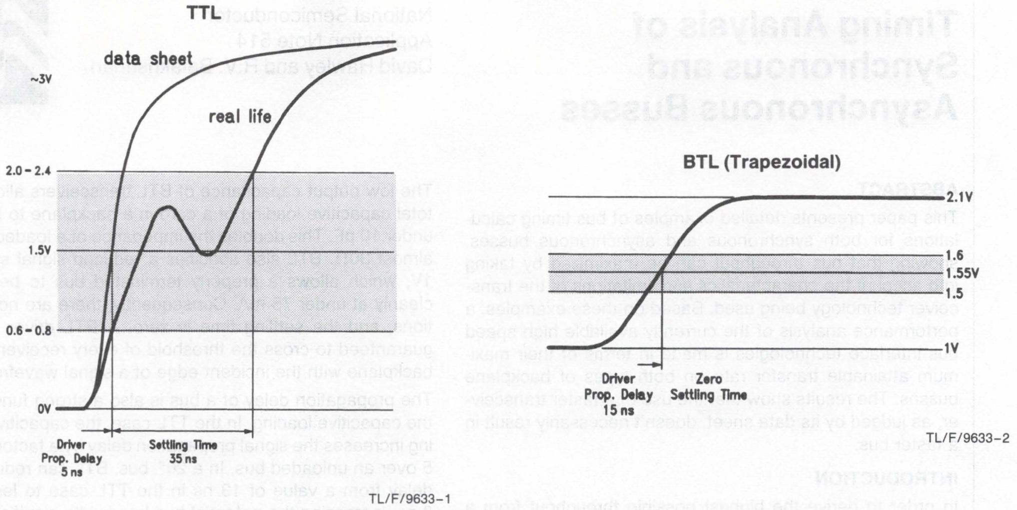


FIGURE 1. Settling Times

bus, with the clock driver located at the midpoint, total skew can easily exceed 10 ns; in our case, 5 ns for the bus, plus 7 ns for the receiver and a transparent latch used to implement bus wait states.

Synchronous Data Transfer Timing

In this example *(Figure 3)*, the worst case data propagation delay from the master to the slave is simply the sum of the delays of the individual components of the data path. This path travels through the master's edge-triggered flip-flop and bus driver, across the length of the bus, and then through the slave's bus receiver and flip-flop, where the incoming data is latched. However, because this is a synchronous system, the data can be "pipelined" to some extent within the intervening logic. This means that the minimum clock cycle possible under this configuration is the sum of the logic skews, plus the maximum bus propagation delay, the set-up and hold times of the receiver, and the clock skew *(Figure 4)*.

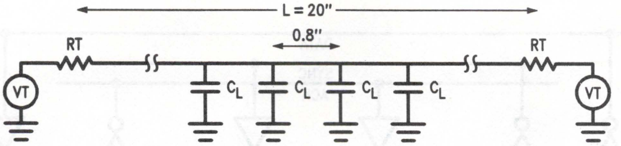
The advantage of a synchronous system is that the absolute timing requirements are set by the clock; the entire system can be optimized with this constraint in mind. This can become a disadvantage as technology advances beyond the point at which the synchronous bus was designed. A synchronous system must be continually redesigned for higher clock rates in order to take advantage of improvements in technology. Synchronous busses are therefore more suited to specific applications than to general-purpose, extended lifespan products.

Synchronous Timing Calculations

The first set of calculations assumes a TTL bus with AS transceivers and logic. As can be seen, the bus settling time overwhelms all the other skews and delays in the system. The upper limit of a discrete TTL synchronous bus implementation is roughly 15 MT (megatransfers/second). No particular advantage is gained by using FAST devices because, while the maximum propagation delays specified for that family are shorter than for AS, the maximum skews are generally greater. The effect of skew specifications is another subtlety of system performance analysis.

Two types of BTL transceivers are currently available, the BTL Trapezoidal and the BTL Turbo. The Trapezoidal transceivers have controlled rise and fall times on their drivers of 6 ns (nominal) to reduce crosstalk interference and switching noise within the backplane. In addition, the receivers incorporate crosstalk filters that practically eliminate far-end crosstalk problems on the bus. The Turbo transceivers eliminate these Trapezoidal features, but are much faster as a result. Switching noise problems are overcome by the use of individual ground return lines for each driver. Stripline backplane construction and careful layout techniques are required to minimize crosstalk.

Although the BTL Trapezoidal transceiver delays are much greater than those of the TTL devices, the absence of settling time results in a smaller overall clock cycle time. A maximum transfer rate of 18 MT becomes possible. When the Turbo devices are used, system throughput increases to 24 MT in this discrete implementation.


L = 20"
0.8"
RT
RT
VT
VT
C_L
C_L
C_L
C_L

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C_L (TTL) ≈ 25 pF/0.8" = 375 pF/ft.

C_L (BTL) ≈ 10 pF/0.8" = 150 pF/ft.

$Z_O \approx 75\Omega$	Unloaded Bus Impedance
$C_O \approx 20$ pF/ft.	Distributed Capacitance of Unloaded Bus
$T_O \approx 1.8$ ns/ft.	Unloaded Bus Propagation Delay

$Z_L = Z_O/\sqrt{1 + (C_L/C_O)}$	Loaded Bus Impedance
$T_L = L \times T_O \times \sqrt{1 + (C_L/C_O)}$	Loaded Propagation Delay

$\boxed{T_L \text{ (TTL)} \approx 13.3 \text{ ns}}$ $\boxed{\text{TL (BTL)} \approx 8.75 \text{ ns}}$

FIGURE 2. Effects of Capacitive Loading

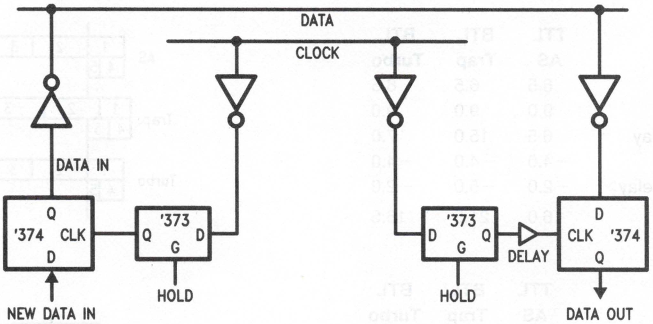
DATA
CLOCK
DATA IN
Q
'374
CLK
D
'373
Q
G
D
HOLD
NEW DATA IN
'373
D
G
Q
HOLD
DELAY
D
CLK
'374
Q
DATA OUT

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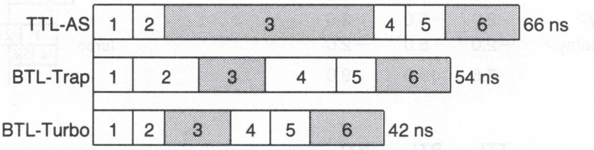
FIGURE 3. Synchronous Bus Logic for Burst Data Transfers



	TTL AS	BTL Trap	BTL Turbo
1) Max '374 Skew	5.0	5.0	5.0
2) Max Bus Driver Skew	4.5	10.0	5.0
3) Max Bus Delay	35.0	9.0	9.0
4) Max Bus Receiver Skew	4.5	13.0	6.0
5) Max '374 Setup and Hold	5.0	5.0	5.0
6) Max Clock Skew	12.0	12.0	12.0
TOTAL (ns)	66.0	54.0	42.0
MTransfers/second	18.5	18.5	23.8

FIGURE 4. Synchronous Burst Data Transfer Timing

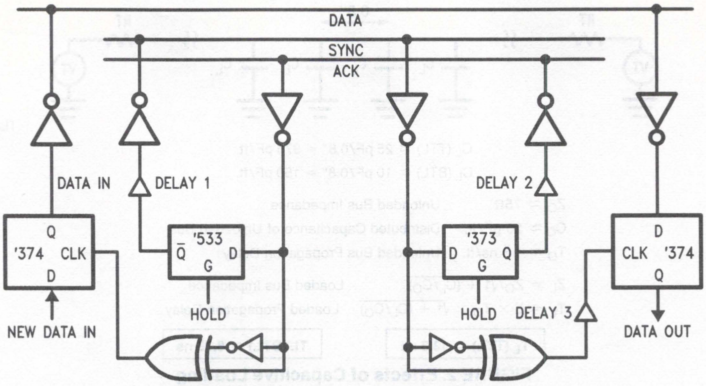

DATA
SYNC
ACK
DATA IN
DELAY 1
DELAY 2
'374
Q
CLK
D
NEW DATA IN
'533
Q̄
G
D
HOLD
'373
D
Q
G
HOLD
DELAY 3
D
CLK
'374
Q
DATA OUT

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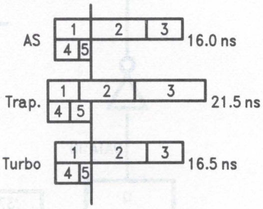
FIGURE 5. Asynchronous Bus Logic for Burst Data Transfers

DELAY 1	TTL AS	BTL Trap	BTL Turbo
1) Max XOR Delay	6.5	6.5	6.5
2) Max '374 Delay	9.0	9.0	9.0
3) Max Data Driver Delay	6.5	15.0	7.0
4) <Min '533 Delay>	−4.0	−4.0	−4.0
5) <Min Sync Driver Delay>	−2.0	−5.0	−2.0
TOTAL (ns)	16.0	21.5	16.5



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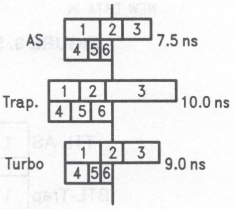
DELAY 2	TTL AS	BTL Trap	BTL Turbo
1) Max XOR Delay	6.5	6.5	6.5
2) Max '374 Hold Time	3.0	3.0	3.0
3) Delay 3	5.5	14.0	7.0
4) <Min '373 Delay>	−3.5	−3.5	−3.5
5) <Min Ack Driver Delay>	−2.0	−5.0	−2.0
5) <Min Data Receiver Delay>	−2.0	−5.0	−2.0
TOTAL (ns)	7.5	10.0	9.0



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DELAY 3	TTL AS	BTL Trap	BTL Turbo
1) Max Data Receiver Delay	6.5	18.0	8.0
2) Max '374 Setup Time	2.0	2.0	2.0
4) <Min Sync Receiver Delay>	−2.0	−5.0	−2.0
5) <Min XOR Delay>	−1.0	−1.0	−1.0
TOTAL (ns)	5.5	14.0	7.0

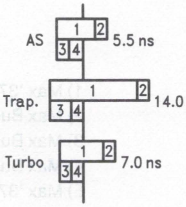

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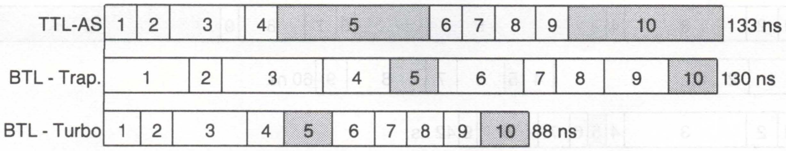
FIGURE 6. Asynchronous Bus Logic Delay Calculations



	TTL AS	BTL Trap	BTL Turbo
1) Max Ack Receiver Delay	6.5	18.0	8.0
2) Max '533 Delay	7.5	7.5	7.5
3) Delay 1	16.0	21.5	16.5
4) Max Sync Driver Delay	6.5	15.0	7.0
5) Max Bus Delay + Skew	35.0	10.0	10.0
6) Max Sync Receiver Delay	6.5	18.0	8.0
7) Max '373 Delay	6.0	6.0	6.0
8) Delay 2	7.5	10.0	9.0
9) Max Ack Driver Delay	6.5	15.0	7.0
10) Max Bus Delay	35.0	9.0	9.0
TOTAL (ns)	133.0	130.0	88.0
MTransfers/second	7.5	7.7	11.4

FIGURE 7. Asynchronous Burst Data Transfer Timing (Worst Case)

The largest cycle time delay in the final BTL Turbo example is clock skew. Bus skews can be reduced by distributing the clock to each board independently, using a dedicated trace on the backplane such that all lines are of equal length. This makes the clock propagation delay from the driver to each board the same, and thus practically eliminates the bus skew. In addition, better tolerances on driver, receiver, and logic propagation delays (smaller skews) will improve both the clock skew and the effect of transceiver delays on the cycle time.

ASYNCHRONOUS BUS TIMING

Our second example is also of a burst transfer, but this time using asynchronous bus timing. In this system, the master issues a strobe along with the data, and waits for an acknowledgement from the slave before removing the current data from the bus lines. All timing is controlled by the two participants in the data transfer. (Once again, we are assuming that new status does not have to be generated on each data transfer.)

The greatest advantage of an asynchronous bus protocol is its ability to adapt the speed of the bus to the speed of any two communicating boards. The most flexibility is achieved when no technology dependencies are introduced into the protocol. Unlike a synchronous system, where every board is designed with the same timing constraints in mind, a technology-independent module is designed with no assumptions about the timing of the rest of the system. Instead, each transmitting board simply guarantees that its data is valid on the bus at least zero nanoseconds before it issues its synchronization signal, and each receiving board is responsible for ensuring that its data has been successfully latched before issuing an acknowledge. The protocol itself imposes no artificial set-up or hold time limitations.

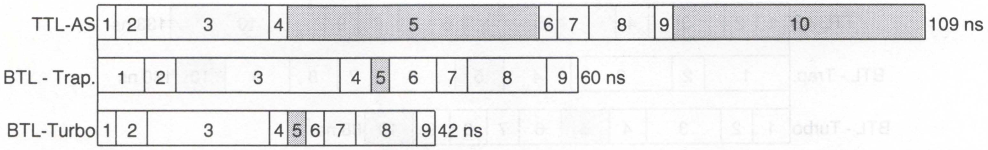
The result of this lack of timing constraints is that a board built today, using today's technology, is guaranteed to work in a system designed perhaps twenty years from now. That system will be forced to slow down whenever necessary to accommodate the greater internal delays and skews of the older module. However, if two future modules are communicating, they will transfer data at the maximum rate allowed by the future technology. The new IEEE Futurebus standard implements this type of protocol.

ASYNCHRONOUS DATA TRANSFER TIMING

The requirement that boards generate their own data synchronization and acknowledge signals, and the likelihood of zero set-up and hold times on the bus, make the timing of the asynchronous system more complicated than the previous example *(Figure 5).* Also, we are maximizing the performance of the sync/ack handshake by transferring data on each signal transition. This is known as a two-edge handshake.

On the master side, the board must guarantee that its data is valid on the bus before issuing the synchronization signal. This means that a delay must be inserted in the sync signal path (Delay 1) which includes the maximum propagation delays through the XOR clock generation circuit, edge-triggered flip-flop, and data bus driver. This is excessive, however, because the minimum delays through the sync latch and bus driver can be subtracted *(Figure 6).*

On the slave side, delays are required to guarantee that both the set-up and hold time specifications of the data latch are met. The set-up time delay (Delay 3) ensures that the sync signal, which may have minimum propagation delays through the sync bus receiver and XOR clock generator, arrives at the edge-triggered data flip-flop a set-up time after the data, which may have a maximum delay through



	TTL AS	BTL Trap	BTL Turbo
1) Min Ack Receiver Delay	2.0	5.0	2.0
2) Min '533 Delay	4.0	4.0	4.0
3) Delay 1	16.0	21.5	16.5
4) Min Sync Driver Delay	2.0	5.0	2.0
5) Min Bus Delay + Skew	35.0	1.0	1.0
6) Min Sync Receiver Delay	2.0	5.0	2.0
7) Min '373 Delay	3.5	3.5	3.5
8) Delay 2	7.5	10.0	9.0
9) Min Ack Driver Delay	2.0	5.0	2.0
10) Min Bus Delay	35.0	0.0	0.0
TOTAL (ns)	109.0	60.0	42.0
MTransfers/second	9.2	16.7	23.8

FIGURE 8. Asynchronous Burst Data Transfer Timing (Best Case)

the data bus receiver. The hold time delay (Delay 2) ensures that the data remains at the data flip-flop a hold time after the sync signal, which this time may have a maximum propagation delay through the XOR and the set-up time delay element just introduced. Since the removal of data is controlled by the ack signal, the hold time delay can be reduced by the minimum delays through the ack latch and bus driver, and the minimum propagation delay of the data bus receiver.

This is all very confusing at first, but these delay elements now in place in our circuit guarantee the receiver set-up and hold time requirements while maintaining the technology independence of the bus protocol. Now we can calculate the burst data transfer rate on this asynchronous bus.

The critical path is now the sync/ack handshake. The circuit delays are in place to make sure that data is transferred successfully. To calculate the transfer rate, simply add up all the propagation delays through the sync/ack loop *(Figures 7* and *8):* on the master, the ack receiver, the sync latch, Delay 1, and the sync driver; a bus propagation delay; on the slave, the sync receiver, the ack latch, Delay 2, and the ack driver; and another bus propagation delay.

Should you use worst-case values throughout your evaluation? The beauty of a technology-independent asynchronous protocol is that is will adapt to the speed of the individual logic elements in the sync/ack handshake path. If all the devices happen to have worst-case characteristics, then yes. If they are all fast parts, however, then data transfer will take place under best-case conditions. Both calculations are included, providing the expected operating range of the circuit.

ASYNCHRONOUS TIMING CALCULATIONS

Once again, the TTL design is overwhelmed by the settling time of the bus. Since the sync/ack signal pair are acting as clocks in this system, glitches that may occur during the signal settling time are intolerable. This means that the 35 ns bus settling time must be hard-wired into the receiver logic, and cannot be reduced under best-case conditions. The performance of an asynchronous TTL backplane, from 7.5 to 9.2 MT, cannot approach that of a similar synchronous backplane.

The BTL Trapezoidal system has very similar performance to a TTL backplane under worst-case conditions. However, because there is no settling time penalty associated with BTL signals, the effect of improvements in device operation have a far more pronounced effect. In the best case, the performance is close to that of the equivalent synchronous system. Also, since the bus signal propagation delay is a function only of the distance between the two boards, modules placed in adjacent slots will experience almost no backplane delays.

A BTL Turbo board benefits from the same clean electrical environment that a Trapezoidal one does, except with a 40–50% overall improvement in performance. In the best case, the performance is the same as that of the equivalent synchronous system. Of course, as device parameters improve, with lower propagation delays and skews, the performance of the asynchronous system will continue to improve. The largest reductions in the transfer cycle time will come as interfaces for asynchronous busses such as Futurebus are integrated onto a single piece of silicon, where skews and delays can be more tightly controlled.

CONCLUSION

The use of transceivers designed specifically for the transmission-line environment typical in today's high-speed backplanes provides advantages in both the performance and electrical integrity of a system. The advantages of BTL only become obvious after a careful analysis of data transfer timing considerations. The Trapezoidal and Turbo options provide a designer with the opportunity to make the appropriate application-dependent cost/performance tradeoffs. A sometimes controversial issue is the appropriateness of a synchronous versus an asynchronous design. The former will usually provide an immediate performance advantage in a fully synchronized environment, but a carefully-designed general-purpose asynchronous protocol will often have a longer useful product life.

REFERENCES

1. R.V. Balakrishnan, "The Proposed IEEE 896 Futurebus—A Solution to the Bus Driving Problem," *IEEE Micro,* August 1984.
2. R.V. Balakrishnan, "Physical Layer Timing Design Considerations for High Speed Backplane Busses," Buscon/87 West, January 1987.
3. D.B. Gustavson and J. Theus, "Wire-OR Logic on Transmission Lines," IEEE Micro, June 1983, pp. 51–55.
4. *Interface Databook,* National Semiconductor Corp., Santa Clara, CA, 1986.
5. *ALS/AS Logic Databook,* National Semiconductor Corp., Santa Clara, CA, 1987.
6. *IEEE P896 D7.5a,*"Futurebus: A Bus Standard for Multiprocessing Architectures", IEEE, June 1987.

TABLE I. Device Parameters

Device	Parameter (Transition)	Minimum Prop. Delay	Maximum Prop. Delay	Maximum Skew	Setup/Hold
DM74AS374	LH	3.0	8.0	5.0	**2.0/3.0**
Edge-Triggered Flip-Flop	HL	4.0	**9.0**	**5.0**	
DM74AS373	LH	**3.5**	**6.0**	**2.5**	2.0/3.0
Transparent Latch	HL	**3.5**	**6.0**	**2.5**	
DM74AS533	LH	**4.0**	**7.5**	**3.5**	2.0/3.0
Inverting Transparent Latch	HL	4.0	7.0	3.0	
DM74AS86	Other Input L	2.0	**6.5**	4.5	
2-Input XOR	Other Input H	**1.0**	6.0	5.0	
DM74AS240	LH	2.0	6.5	**4.5**	
Bus Driver/Receiver	HL	2.0	5.7	3.7	
DM74AS242	LH	**2.0**	**6.5**	**4.5**	
Bus Transceiver	HL	2.0	5.7	3.7	
DS3896	Rx	**5.0**	**18.0**	**13.0**	
BTL Trapezoidal Transceiver	Tx	**5.0**	**15.0**	**10.0**	
DS3893	Rx	**2.0**	**8.0**	**6.0**	
BTL Turbo Transceiver	Tx	**2.0**	**7.0**	**5.0**	

Note: Values in boldface are those used in the preceding calculations.

National Semiconductor

DS75160A/DS75161A/DS75162A
IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down.

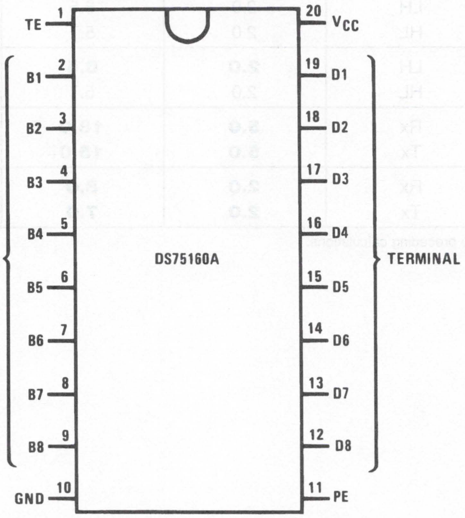
The General Purpose Interface Bus is comprised of 16 signal lines — 8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system, or with DS75162A in a multi-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

Connection Diagrams

Dual-In-Line Package



TL/F/5804-1

Top View

Order Number DS75160AN
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C Molded Package	1897 mW

*Derate molded package 15.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$		2.7	3.5		V
		Bus (Note 5)	$I_{OH} = -5.2$ mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OH} = 48$ mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and TE, PE, DC, SC Inputs	$V_I = 5.5V$			0.2	100	µA
			$V_I = 2.7V$			0.1	20	
I_{IL}	Low-Level Input Current		$V_I = 0.5V$			−10	−100	µA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)} = 0$ (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)} = -1.5V$ to 0.4V	−1.3			mA
				$V_{I(bus)} = 0.4V$ to 2.5V	0		−3.2	
				$V_{I(bus)} = 2.5V$ to 3.7V			2.5 −3.2	
				$V_{I(bus)} = 3.7V$ to 5V	0		2.5	
				$V_{I(bus)} = 5V$ to 5.5V	0.7		2.5	
			$V_{CC} = 0V$, $V_{I(bus)} = 0V$ to 2.5V				40	µA
I_{OS}	Short-Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current	DS75160A	Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$			85	125	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$			70	100	
		DS75161A	TE = 0.8V, DC = 0.8V, $V_I = 0.8V$			84	125	
		DS75162A	TE = 0.8V, DC = 0.8V, SC = 2V, $V_I = 0.8V$			85	125	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 5V$ or 0V, $V_I = 0V$ to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to outputs on DS75161A and DS75162A that are open collector.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%, T_A = 0°C$ to $70°C$ (Note 1)

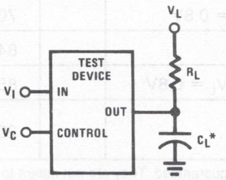
Symbol	Parameter	From	To	Conditions	DS75160A			DS75161A			DS75162A			Units
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	$V_L = 2.3V$ $R_L = 38.3\Omega$ $C_L = 30$ pF *Figure 1*		10	20		10	20		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20		14	20		14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	$V_L = 5.0V$ $R_L = 240\Omega$ $C_L = 30$ pF *Figure 2*		14	20		14	20		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20		10	20		10	20	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Bus	$V_I = 3.0V$ $V_L = 0V$ $R_L = 480\Omega$ $C_L = 15$ pF *Figure 1*		19	32		23	40		23	40	ns
t_{PHZ}	Output Disable Time From High Level					15	22		15	25		15	25	ns
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$ $V_L = 2.3V$ $R_L = 38.3\Omega$ $C_L = 15$ pF *Figure 1*		24	35		28	48		28	48	ns
t_{PLZ}	Output Disable Time From Low Level					17	25		17	27		17	27	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Terminal	$V_I = 3.0V$ $V_L = 0V$ $R_L = 3\ k\Omega$ $C_L = 15$ pF *Figure 1*		17	33		18	40		18	40	ns
t_{PHZ}	Output Disable Time From High Level					15	25		22	33		22	33	ns
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$ $V_L = 5V$ $R_L = 280\Omega$ $C_L = 15$ pF *Figure 1*		25	39		28	52		28	52	ns
t_{PLZ}	Output Disable Time From Low Level					15	27		20	35		20	35	ns
t_{PZH}	Output Pull-Up Enable Time (DS75160A Only)	PE (Note 2)	Bus	$V_I = 3V$ $V_L = 0V$ $R_L = 480\Omega$ $C_L = 15$ pF *Figure 1*		10	17		NA			NA		ns
t_{PHZ}	Output Pull-UP Disable Time (DS75160A Only)					10	15		NA			NA		ns

Note 1: Typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$ and are meant for reference only.

Note 2: Refer to Functional Truth Tables for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



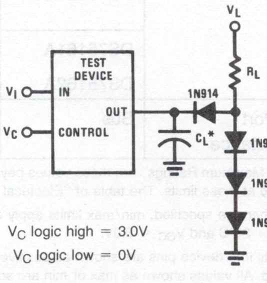
TL/F/5804-8

V_C logic high = 3.0V

V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V

V_C logic low = 0V

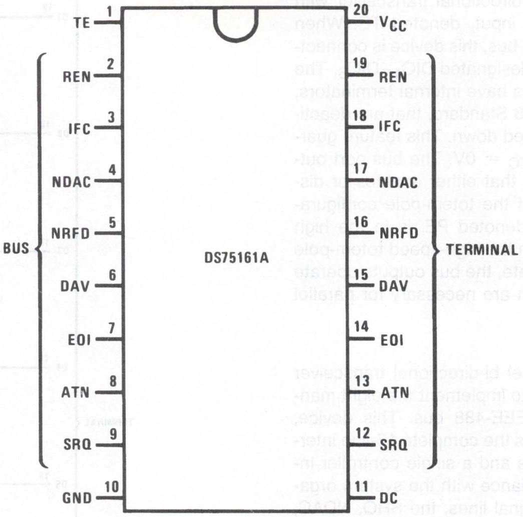
TL/F/5804-9

*C_L includes jig and probe capacitance

FIGURE 2

Connection Diagrams (Continued)

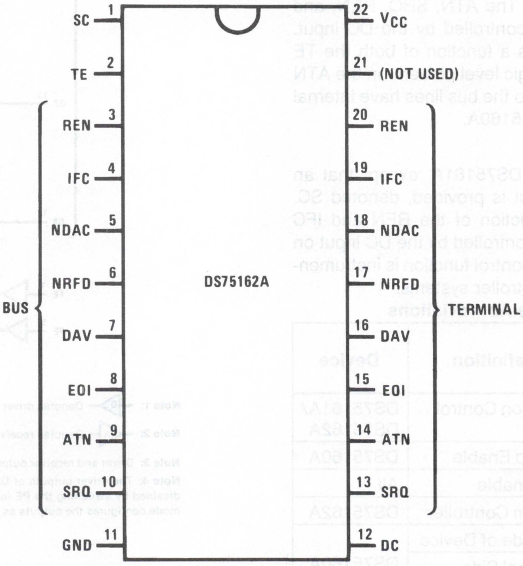
Dual-In-Line Package


TE 1
REN 2
IFC 3
NDAC 4
NRFD 5
DAV 6
EOI 7
ATN 8
SRQ 9
GND 10
BUS
DS75161A
20 VCC
19 REN
18 IFC
17 NDAC
16 NRFD
15 DAV
14 EOI
13 ATN
12 SRQ
11 DC
TERMINAL

TL/F/5804-2

Top View

Dual-In-Line Package


SC 1
TE 2
REN 3
IFC 4
NDAC 5
NRFD 6
DAV 7
EOI 8
ATN 9
SRQ 10
GND 11
BUS
DS75162A
22 VCC
21 (NOT USED)
20 REN
19 IFC
18 NDAC
17 NRFD
16 DAV
15 EOI
14 ATN
13 SRQ
12 DC
TERMINAL

TL/F/5804-3

Top View

Order Number DS75161AN or DS75162AN
See NS Package Number N20A or N22A

Functional Description

DS75160A

This device is an 8-channel bi-directional transceiver with one common direction control input, denoted TE. When used to implement the IEEE-488 bus, this device is connected to the eight data bus lines, designated DIO$_1$–DIO$_8$. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when V_{CC} = 0V. The bus port outputs also have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When this control input, denoted PE, is in the high state, the bus outputs operate in the high-speed totem-pole mode. When PE is in the low state, the bus outputs operate as open collector outputs which are necessary for parallel polling.

DS75161A

This device is also an 8-channel bi-directional transceiver which is specifically configured to implement the eight management signal lines of the IEEE-488 bus. This device, paired with the DS75160A, forms the complete 16-line interface between the IEEE-488 bus and a single controller instrumentation system. In compliance with the system organization of the management signal lines, the SRQ, NDAC, and NRFD bus port outputs are open collector. In contrast to the DS75160A, these open collector outputs are a fixed configuration. The direction control is divided into three groups. The DAV, NDAC, and NRFD transceiver directions are controlled by the TE input. The ATN, SRQ, REN, and IFC transceiver directions are controlled by the DC input. The EOI transceiver direction is a function of both the TE and DC inputs, as well as the logic level present on the ATN channel. The port connections to the bus lines have internal terminators identical to the DS75160A.

DS75162A

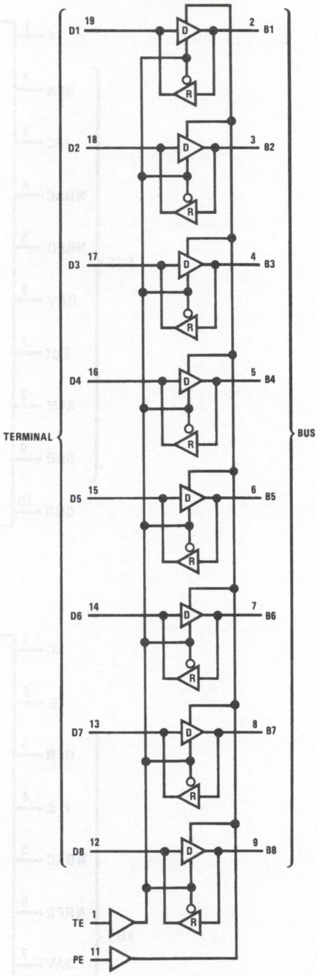
This device is identical to the DS75161A, except that an additional direction control input is provided, denoted SC. The SC input controls the direction of the REN and IFC transceivers that are normally controlled by the DC input on the DS75161A. This additional control function is instrumental in implementing multiple controller systems.

Table of Signal Line Abbreviations

Signal Line Classification	Mnemonic	Definition	Device
Control Signals	DC	Direction Control	DS75161A/ DS75162A
	PE	Pull-Up Enable	DS75160A
	TE	Talk Enable	All
	SC	System Controller	DS75162A
Data I/O Ports	B1–B8	Bus Side of Device	DS75160A
	D1–D8	Terminal Side of Device	
Management Signals	ATN	Attention	DS75161A/ DS75162A
	DAV	Data Valid	
	EOI	End or Identify	
	IFC	Interface Clear	
	NDAC	Not Data Accepted	
	NRFD	Not Ready for Data	
	REN	Remote Enable	
	SRQ	Service Request	

Logic Diagrams

DS75160A



Note 1: —▷— Denotes driver

Note 2: —◁— Denotes receiver

Note 3: Driver and receiver outputs are totem-pole configurations

Note 4: The driver outputs of DS75160A can have their active pull-ups disabled by switching the PE input (pin 11) to the logic low state. This mode configures the outputs as open collector.

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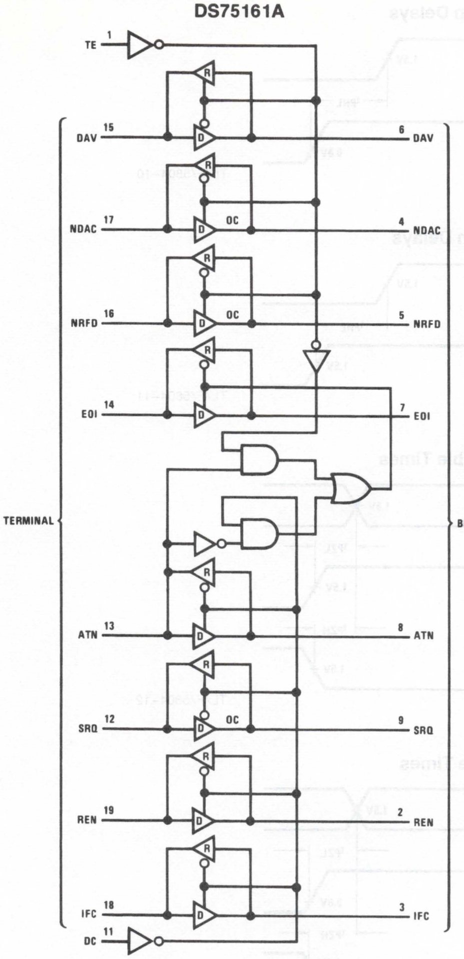
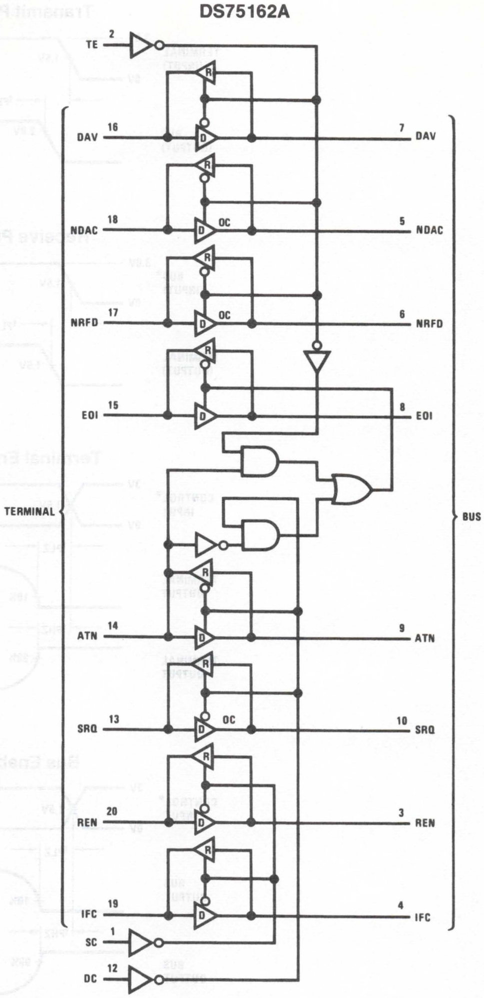
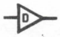
Logic Diagrams (Continued)

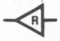

DS75161A
TE 1
R
D
DAV 15
6 DAV
NDAC 17
OC
4 NDAC
NRFD 16
OC
5 NRFD
EOI 14
7 EOI
TERMINAL
BUS
ATN 13
8 ATN
SRQ 12
OC
9 SRQ
REN 19
2 REN
IFC 18
3 IFC
DC 11

TL/F/5804-5


DS75162A
TE 2
R
D
DAV 16
7 DAV
NDAC 18
OC
5 NDAC
NRFD 17
OC
6 NRFD
EOI 15
8 EOI
TERMINAL
BUS
ATN 14
9 ATN
SRQ 13
OC
10 SRQ
REN 20
3 REN
IFC 19
4 IFC
SC 1
DC 12

TL/F/5804-6

Note 1:  Denotes driver

Note 2:  Denotes receiver

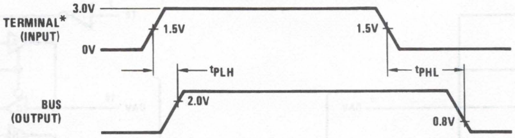
Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

TL/F/5804-7

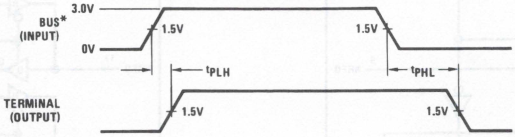
Switching Waveforms

Transmit Propagation Delays


3.0V
TERMINAL*
(INPUT)
0V
1.5V
1.5V
tPLH
tPHL
BUS
(OUTPUT)
2.0V
0.8V

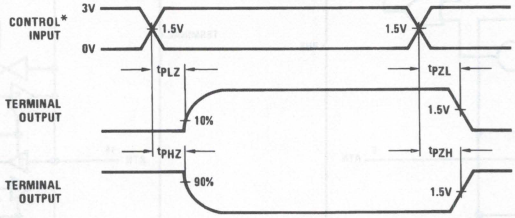
TL/F/5804-10

Receive Propagation Delays


3.0V
BUS*
(INPUT)
0V
1.5V
1.5V
tPLH
tPHL
TERMINAL
(OUTPUT)
1.5V
1.5V

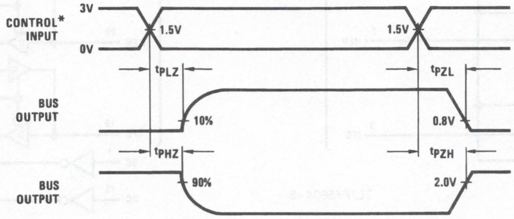
TL/F/5804-11

Terminal Enable/Disable Times


3V
CONTROL*
INPUT
0V
1.5V
1.5V
tPLZ
tPZL
TERMINAL
OUTPUT
10%
1.5V
tPHZ
tPZH
TERMINAL
OUTPUT
90%
1.5V

TL/F/5804-12

Bus Enable/Disable Times

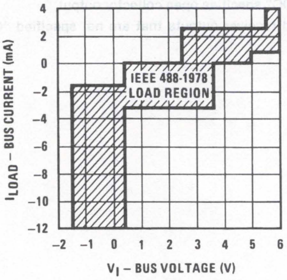

3V
CONTROL*
INPUT
0V
1.5V
1.5V
tPLZ
tPZL
BUS
OUTPUT
10%
0.8V
tPHZ
tPZH
BUS
OUTPUT
90%
2.0V

TL/F/5804-13

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristics



TL/F/5804-14

Refer to Electrical Characteristics table

Functional Truth Tables

DS75160A

Control Input Level		Data Transceivers	
TE	PE	Direction	Bus Port Configuration
H	H	T	Totem-Pole Output
H	L	T	Open Collector Output
L	X	R	Input

DS75161A

Control Input Level			Transceiver Signal Direction						
TE	DC	ATN*	EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H		R	R	R	T	R	R	T
H	L		T	T	T	R	R	R	T
L	H		R	R	R	T	T	T	R
L	L		T	T	T	R	T	T	R
H	X	H	T						
L	X	H	R						
X	H	L	R						
X	L	L	T						

DS75162A

Control Input Level				Transceiver Signal Direction						
SC	TE	DC	ATN*	EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H	H		R	T	T	T	R	R	T
H	H	L		T	T	T	R	R	R	T
H	L	H		R	T	T	T	T	T	R
H	L	L		T	T	T	R	T	T	R
L	H	H		R	R	R	T	R	R	T
L	H	L		T	R	R	R	R	R	T
L	L	H		R	R	R	T	T	T	R
L	L	L		T	R	R	R	T	T	R
X	H	X	H	T						
X	L	X	H	R						
X	X	H	L	R						
X	X	L	L	T						

H = High level input
L = Low level input
X = Don't care
T = Transmit, i.e., signal outputted to bus
R = Receive, i.e., signal outputted to terminal
*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic.

National Semiconductor

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

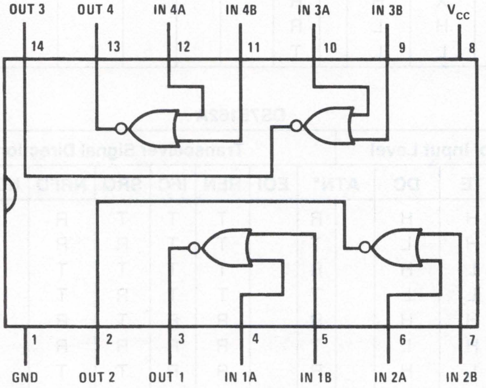
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (30 μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package


OUT 3
OUT 4
IN 4A
IN 4B
IN 3A
IN 3B
V_{CC}
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND
OUT 2
OUT 1
IN 1A
IN 1B
IN 2A
IN 2B

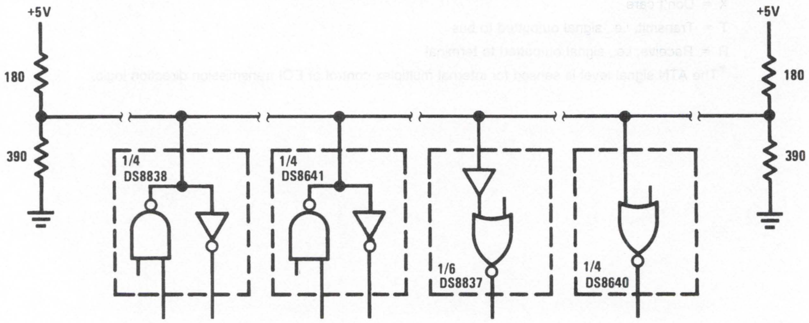
TL/F/5805-1

Top View

Order Number DS7640J, DS8640J or DS8640N
See NS Package Number J14A or N14A

Typical Application

120Ω Unified Data Bus


+5V
180
390
1/4
DS8838
1/4
DS8641
1/6
DS8837
1/4
DS8640
+5V
180
390

TL/F/5805-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	µA
			$V_{CC} = 0V$		1.0	50	µA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	µA
V_{OH}	Output Voltage	$I_{OH} = -400$ µA, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply to $V_{CC} = 5V$, $T_A = 25°C$.

National Semiconductor

DS7641/DS8641 Quad Unified Bus Transceiver

General Description

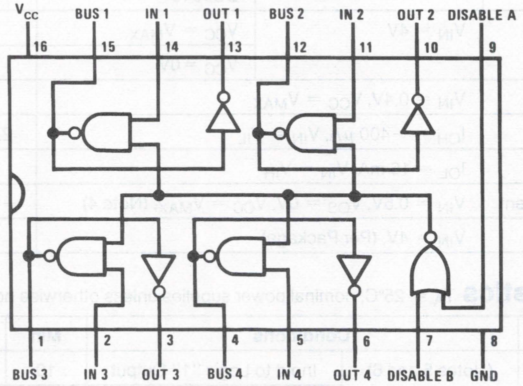
The DS7641 and DS8641 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when $V_{CC} = 0V$. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30 μA typical bus terminal current with normal V_{CC} or with $V_{CC} = 0V$
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Connection Diagram

Dual-In-Line Package


V_CC
BUS 1
IN 1
OUT 1
BUS 2
IN 2
OUT 2
DISABLE A
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
BUS 3
IN 3
OUT 3
BUS 4
IN 4
OUT 4
DISABLE B
GND

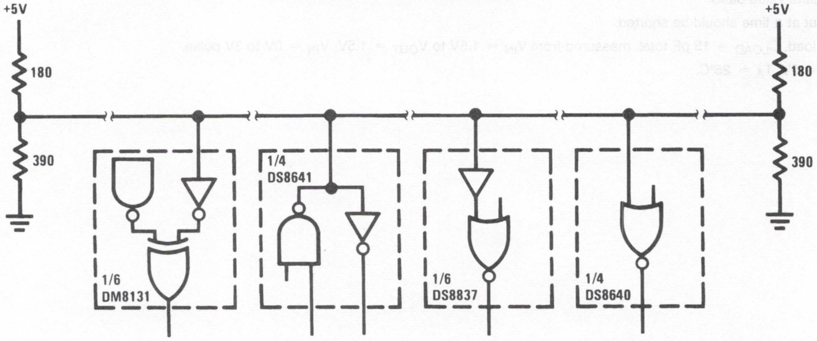
TL/F/5806–1

Top View

Order Number DS7641J, DS8641J or DS8641N
See NS Package Number J16A or N16A

Typical Application

120Ω Unified Data Bus


+5V
180
390
+5V
180
390
1/6 DM8131
1/4 DS8641
1/6 DS8837
1/4 DS8640

TL/F/5806–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS7641	4.5	5.5	V
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS7641	−55	+125	°C
DS8641	0	+70	°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$				1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$			30	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OL} = 16$ mA	DS7641	1.80	1.50		V
			DS8641	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA	DS7641		1.50	1.20	V
			DS8641		1.50	1.30	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (per Package)			50	70	mA

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delays (Note 7)	(Note 5)				
	Disable to Bus "1"			19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7641 and across the 0°C to +70°C range for the DS8641. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 7: The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified.

National Semiconductor

DS7833/DS8833/DS7835/DS8835 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when $V_{CC} = 0V$. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and common inverter receiver disable control.

The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

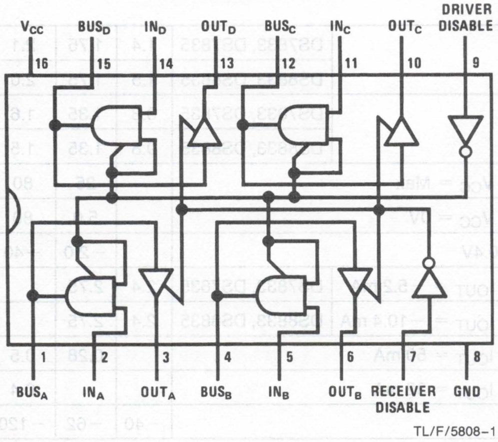
Features

■ Receiver hysteresis	400 mV typ
■ Receiver noise immunity	1.4V typ
■ Bus terminal current for normal V_{CC} or $V_{CC} = 0V$	80 μA max
■ Receivers	
Sink	16 mA at 0.4V max
Source	2.0 mA (Mil) at 2.4V min 5.2 mA (Com) at 2.4V min
■ Drivers	
Sink	50 mA at 0.5V max 32 mA at 0.4V max
Source	10.4 mA (Com) at 2.4V min 5.2 mA (Mil) at 2.4V min

- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC—terminated buses
- Compatible with Series 54/74

Connection Diagram

Dual-In-Line Package

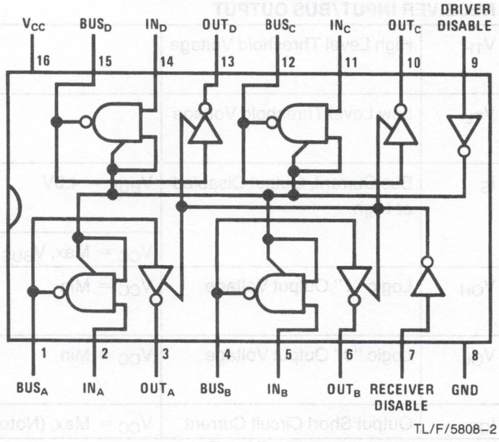

VCC
BUSD
IND
OUTD
BUSC
INC
OUTC
DRIVER DISABLE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
BUSA
INA
OUTA
BUSB
INB
OUTB
RECEIVER DISABLE
GND
TL/F/5808–1

Top View

Order Number DS7833J, DS8833J or DS8833N

See NS Package Number J16A or N16A

Dual-In-Line Package


VCC
BUSD
IND
OUTD
BUSC
INC
OUTC
DRIVER DISABLE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
BUSA
INA
OUTA
BUSB
INB
OUTB
RECEIVER DISABLE
GND
TL/F/5808–2

Top View

Order Number DS7835J, DS8835J or DS8835N

See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7833/DS7835	4.5	5.5	V
DS8833/DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833/DS7835	−55	+125	°C
DS8833/DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltages	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min	DS7833, DS8833, DS8835				0.8	V
			DS7835				0.7	
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_S	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable	V_{OUT} = 2.4V				40	μA
		Inputs = 2.0V	V_{OUT} = 0.4V				−40	μA

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)							
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)	DS7833, DS7835	28	−40	−70	mA
			DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max	DS7833, DS8833		84	116	mA
			DS7835, DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

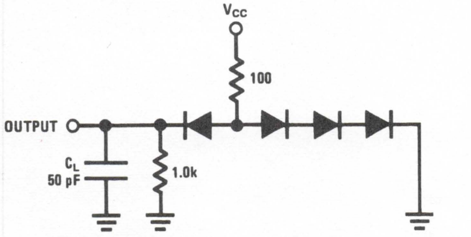
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

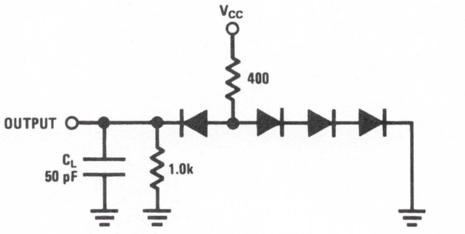
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Input	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Input	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		20	35	ns
			Receiver		13	25	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		24	40	ns
			Receiver		16	35	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		19	35	ns
			Receiver DS7833/DS8833		15	30	ns
			Receiver DS7835/DS8835		33	50	ns

AC Test Circuits



TL/F/5808-3

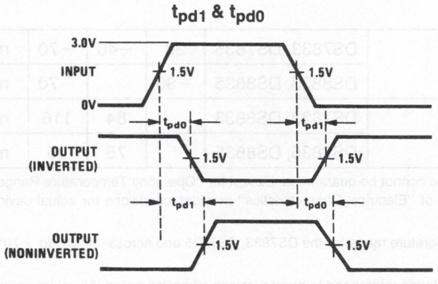
FIGURE 1. Driver Output Load



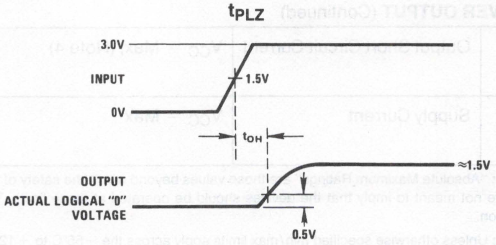
TL/F/5808-4

FIGURE 2. Receiver Output Load

Switching Time Waveforms


t_{pd1} & t_{pd0}
3.0V
INPUT
1.5V
0V
t_{pd0}
t_{pd1}
OUTPUT (INVERTED)
OUTPUT (NONINVERTED)

TL/F/5808-5

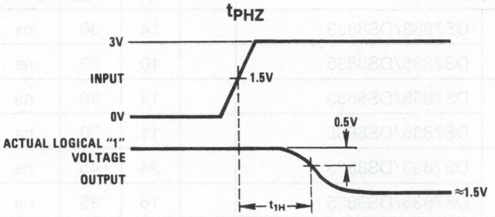

t_{PLZ}
3.0V
INPUT
1.5V
0V
t_{OH}
≈1.5V
OUTPUT
ACTUAL LOGICAL "0" VOLTAGE
0.5V

TL/F/5808-6

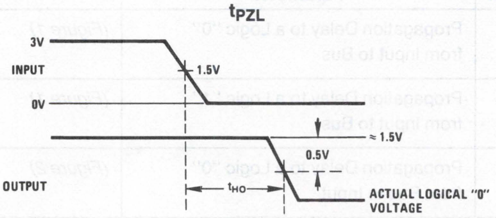
f = 1 MHz

$t_r = t_f \leq 10$ ns (10% to 90%)

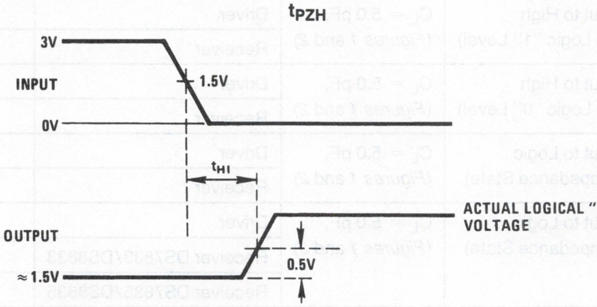
DUTY CYCLE = 50%


t_{PHZ}
3V
INPUT
1.5V
0V
0.5V
ACTUAL LOGICAL "1" VOLTAGE
OUTPUT
≈1.5V
t_{1H}

TL/F/5808-7


t_{PZL}
3V
INPUT
1.5V
0V
≈ 1.5V
0.5V
OUTPUT
t_{HO}
ACTUAL LOGICAL "0" VOLTAGE

TL/F/5808-8


t_{PZH}
3V
INPUT
1.5V
0V
t_{H1}
ACTUAL LOGICAL "1" VOLTAGE
OUTPUT
≈ 1.5V
0.5V

TL/F/5808-9

National Semiconductor

DS7834/DS8834/DS7839/DS8839 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 and DS7839/DS8839 employ TTL outputs on the receiver.

The DS7839/DS8839 are non-inverting quad tranceivers with two common inverter driver disable controls.

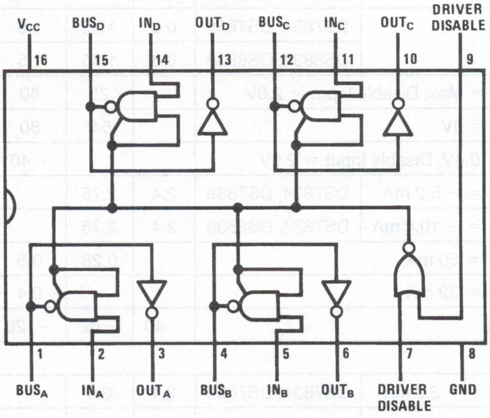
The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

Features

- Receiver hysteresis 400 mV typ
- Receiver noise immunity 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V 80 µA max
- Receivers
  - Sink 16 mA at 0.4V max
  - Source 2.0 mA (Mil) at 2.4V min
  - 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink 50 mA at 0.5V max
  - 32 mA at 0.4V max
  - Source 10.4 mA (Com) at 2.4V min
  - 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω DC-terminated Buses
- Compatible with Series 54/74

Connection Diagrams

Dual-In-Line Package



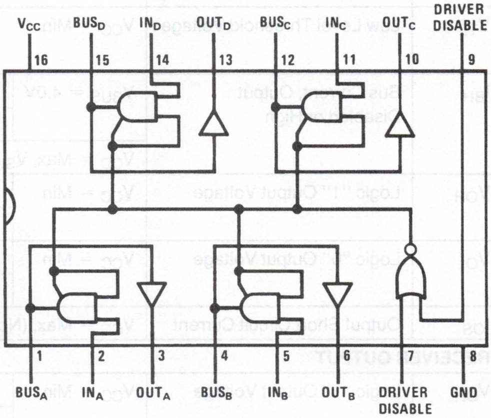
V_{CC}
BUS_D
IN_D
OUT_D
BUS_C
IN_C
OUT_C
DRIVER DISABLE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
BUS_A
IN_A
OUT_A
BUS_B
IN_B
OUT_B
DRIVER DISABLE
GND

TL/F/5809-1

Top View

Order Number DS7834J, DS8834J or DS8834N
See NS Package Number J16A or N16A

Dual-In-Line Package



V_{CC}
BUS_D
IN_D
OUT_D
BUS_C
IN_C
OUT_C
DRIVER DISABLE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
BUS_A
IN_A
OUT_A
BUS_B
IN_B
OUT_B
DRIVER DISABLE
GND

TL/F/5809-2

Top View

Order Number DS7839J, DS8839J or DS8839N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7834, DS7839	4.5	5.5	V
DS8834, DS8839	4.75	5.25	V
Temperature (T_A)			
DS7834, DS7839	−55	+125	°C
DS8834, DS8839	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	µA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Diasbled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	µA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage	V_{CC} = Max		DS7834, DS7839	1.4	1.75	2.1	V
				DS8834, DS8839	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage	V_{CC} = Min		DS7834, DS7839	0.8	1.35	1.6	V
				DS8834, DS8839	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	µA
			V_{CC} = 0V			5.0	80	µA
		V_{CC} = Max, V_{SUS} = 0.4V, Disable Input = 2.0V					−40	µA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834, DS7839	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS7834, DS8839	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834, DS7839	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834, DS8839	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834, DS7839	−28	−40	−70	mA
				DS8834, DS8839	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7834, DS7839 and across the 0°C to +70°C range for the DS8834, DS8839. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

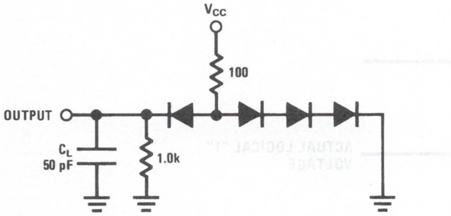
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

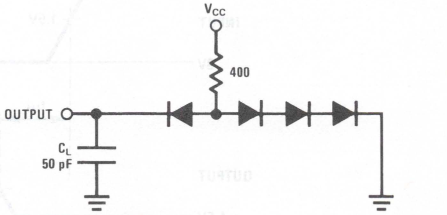
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7839/DS8839		24	45	ns
			DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7839/DS8839		12	30	ns
			DS7834/DS8834		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)* Driver Only			8	20	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)* Driver Only			20	35	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)* Driver Only			24	40	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)* Driver Only			19	35	ns

AC Test Circuit


VCC
100
OUTPUT
CL
50 pF
1.0k

TL/F/5809-3

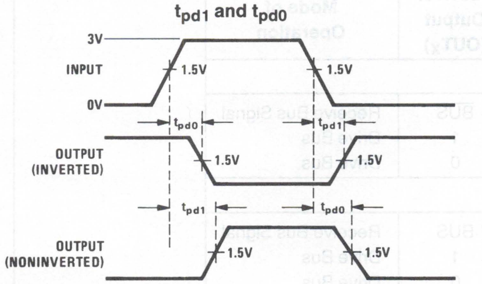
FIGURE 1. Driver Output Load


VCC
400
OUTPUT
CL
50 pF

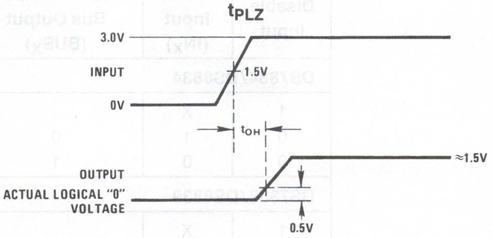
TL/F/5809-4

FIGURE 2. Receiver Output Load

Switching Time Waveforms


tpd1 and tpd0
3V
INPUT
0V
1.5V
1.5V
tpd0
tpd1
OUTPUT (INVERTED)
1.5V
1.5V
tpd1
tpd0
OUTPUT (NONINVERTED)
1.5V
1.5V

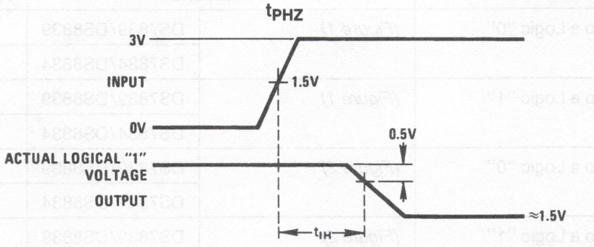
TL/F/5809-5


tPLZ
3.0V
INPUT
1.5V
0V
tOH
≈1.5V
OUTPUT
ACTUAL LOGICAL "0" VOLTAGE
0.5V

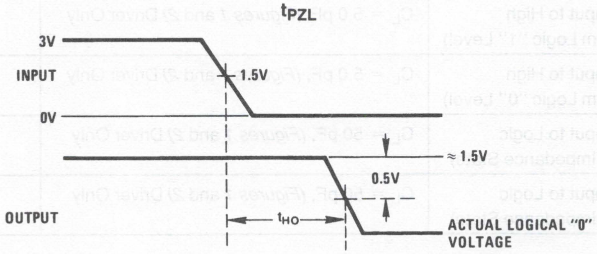
TL/F/5809-6

f = 1 MHz
t_r = t_f ≤ 10 ns (10% to 90%)
Duty Cycle = 50%

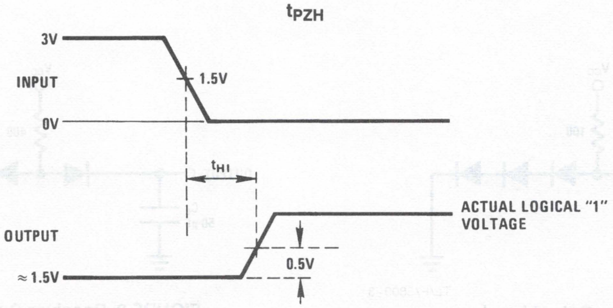
Switching Time Waveforms (Continued)


tPHZ
3V
INPUT
1.5V
0V
0.5V
ACTUAL LOGICAL "1" VOLTAGE
OUTPUT
≈1.5V
tIH

TL/F/5809-7


tPZL
3V
INPUT
1.5V
0V
≈1.5V
0.5V
OUTPUT
tHO
ACTUAL LOGICAL "0" VOLTAGE

TL/F/5809-8


tPZH
3V
INPUT
1.5V
0V
tHI
OUTPUT
ACTUAL LOGICAL "1" VOLTAGE
0.5V
≈1.5V

TL/F/5809-9

Truth Table

Disable Input	Driver Input (IN_X)	Receiver Input/ Bus Output (BUS_X)	Receiver Output (OUT_X)	Mode of Operation
DS7834/DS8834				
1	X		$\overline{\text{BUS}}$	Receive Bus Signal
0	1	0	1	Drive Bus
0	0	1	0	Drive Bus
DS7839/DS8839				
1	X		BUS	Receive Bus Signal
0	1	1	1	Drive Bus
0	0	0	0	Drive Bus

X = Don't care

National Semiconductor

DS7836/DS8836 Quad NOR Unified Bus Receiver

General Description

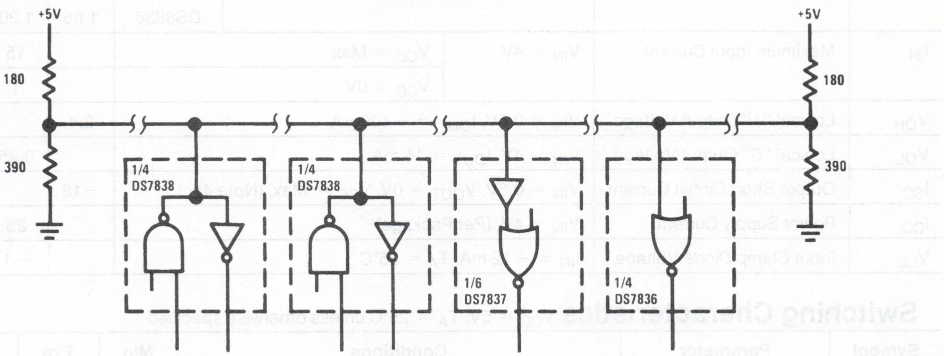
The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Performance is optimized for systems with bus rise and fall times ≤ 1.0 µs/V.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (15 µA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

Typical Application

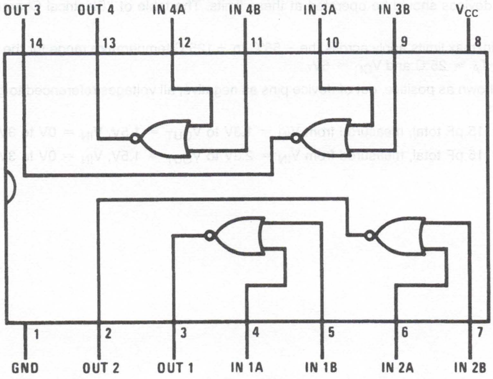
120Ω Unified Data Bus


+5V
180
390
1/4 DS7838
1/4 DS7838
1/6 DS7837
1/4 DS7836
+5V
180
390

TL/F/5810-1

Connection Diagram

Dual-In-Line Package


OUT 3
OUT 4
IN 4A
IN 4B
IN 3A
IN 3B
V_{CC}
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND
OUT 2
OUT 1
IN 1A
IN 1B
IN 2A
IN 2B

TL/F/5810-2

Top View

Order Number DS7836J, DS8836J or DS8836N
See NS Package Number J14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Current Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260 °C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	High Level Input Threshold	$V_{CC} = \text{Max}$	DS7836	1.65	2.25	2.65	V
			DS8836	1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	$V_{CC} = \text{Min}$	DS7836	0.97	1.30	1.63	V
			DS8836	1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = \text{Max}$		15	50	μA
			$V_{CC} = 0V$		1	50	μA
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.5V$, $I_{OUT} = -400\ \mu A$		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 4V$, $I_{OUT} = 16\ mA$			0.25	0.4	V
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OUT} = 0V$, $V_{CC} = \text{Max}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA
V_{CL}	Input Clamp Diode Voltage	$I_{IN} = -12\ mA$, $T_A = 25°C$			−1	−1.5	V

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Ouptut		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, $C_{LOAD} = 15\ pF$ total, measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15\ pF$ total, measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

National Semiconductor

DS7837/DS8837 Hex Unified Bus Receiver

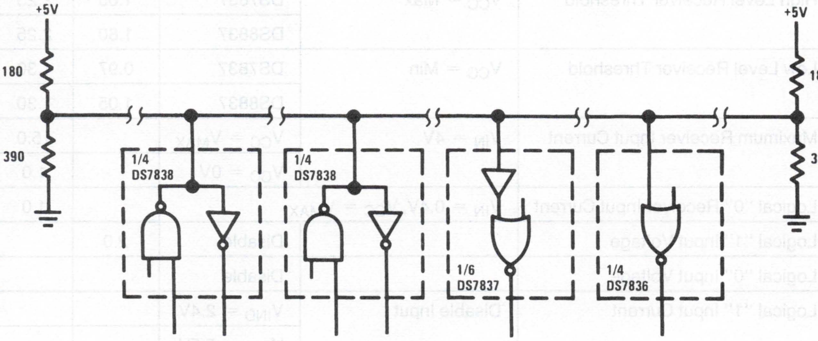
General Description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are TTL compatible. Performance is optimized for systems with bus rise and fall times ≤1.0 μs/V.

Features

- Low receiver input current for normal V_{CC} or $V_{CC} = 0V$ (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

Typical Application

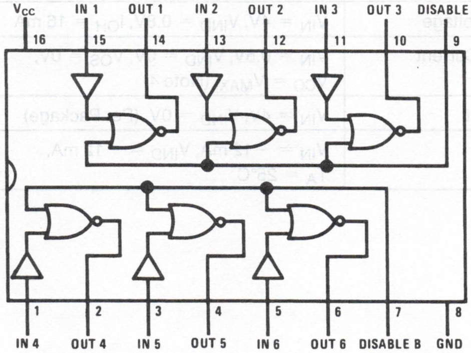


+5V
180
390
1/4 DS7838
1/4 DS7838
1/6 DS7837
1/4 DS7836
+5V
180
390

TL/F/5811–1

Connection Diagram

Dual-In-Line Package



V_CC
IN 1
OUT 1
IN 2
OUT 2
IN 3
OUT 3
DISABLE A
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN 4
OUT 4
IN 5
OUT 5
IN 6
OUT 6
DISABLE B
GND

TL/F/5811–2

Top View

Order Number DS7837J, DS8837J,
DS8837M or DS8837N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	High Level Receiver Threshold	V_{CC} = Max	DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold	V_{CC} = Min	DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	µA
			V_{CC} = 0V		1.0	50.0	µA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	µA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	µA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400 µA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OH} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	$V_{IND} = 0V$, Receiver	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
		Input = 0V, Disable, (Note 7)	Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 7: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

National Semiconductor

DS7838/DS8838 Quad Unified Bus Transceiver

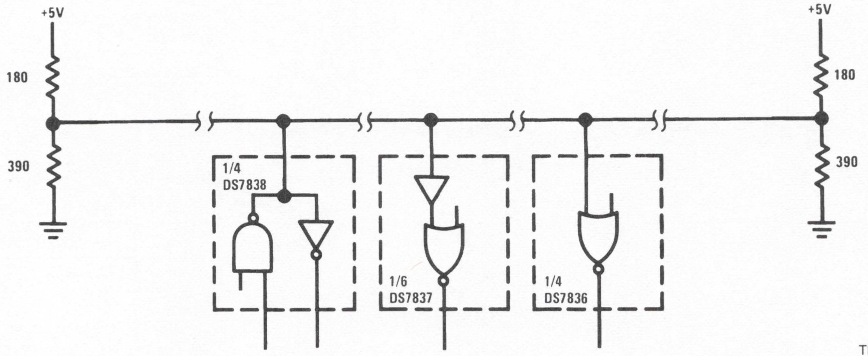
General Description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when $V_{CC} = 0V$. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ≤ 1.0 μs/V.

Features

- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20 μA typical bus terminal current with normal V_{CC} or with $V_{CC} = 0V$
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

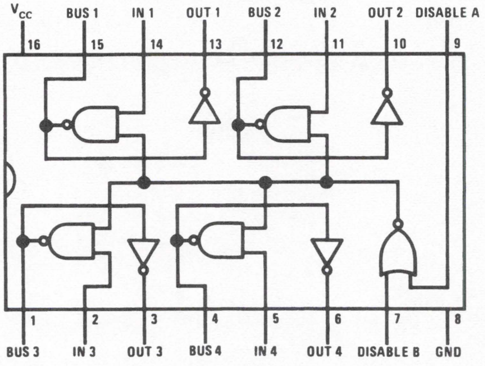
Typical Application



TL/F/5812-1

Connection Diagram

Dual-In-Line Package



TL/F/5812-2

Top View

Order Number DS7838J, DS8838J, DS8838M or DS8838N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature, (Soldering, 4 sec.)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Operating Temperature Range	
DS7838	−55°C to +125°C
DS8838	0°C to +70°C

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$				1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$			20	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $I_{OL} = 16$ mA V_{CC} = Max	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA V_{CC} = Min	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (Per Package)			50	70	mA

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)						
t_{pd}	Propagation Delays (Note 8)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"	(Note 5)		15	23	ns
	Driver Input to Bus "1"	(Note 5)		17	25	ns
	Driver Input to Bus "0"	(Note 5)		9	15	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 7: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 8: These apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise speicified.

National Semiconductor

DS8T26A/DS8T26AM/DS8T28/DS8T28M 4-Bit Bidirectional Bus Transceivers

General Description

The DS8T26A, DS8T28 consist of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

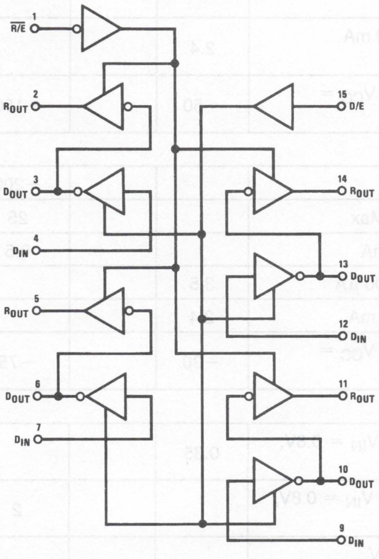
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

Logic and Connection Diagrams

DS8T26A


1 R/E
2 ROUT
3 DOUT
4 DIN
5 ROUT
6 DOUT
7 DIN
15 D/E
14 ROUT
13 DOUT
12 DIN
11 ROUT
10 DOUT
9 DIN

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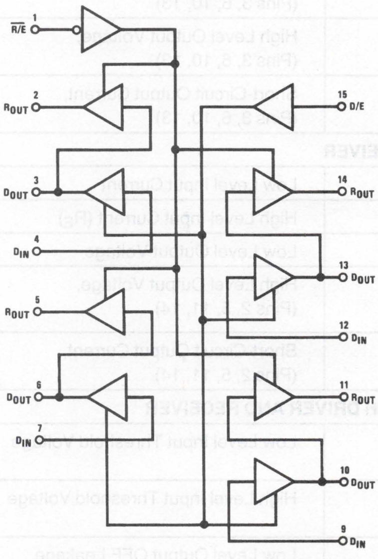
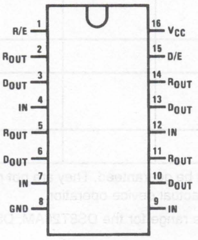
DS8T28


1 R/E
2 ROUT
3 DOUT
4 DIN
5 ROUT
6 DOUT
7 DIN
15 D/E
14 ROUT
13 DOUT
12 DIN
11 ROUT
10 DOUT
9 DIN

TL/F/5813-2

Dual-In-Line Package


R/E 1
ROUT 2
DOUT 3
IN 4
ROUT 5
DOUT 6
IN 7
GND 8
16 VCC
15 D/E
14 ROUT
13 DOUT
12 IN
11 ROUT
10 DOUT
9 IN

TL/F/5813-3

Top View

Order Number DS8T26AJ, DS8T26AMJ, DS8T28J, DS8T28MJ, DS8T26AN or DS8T28N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1V to +5.5V
Output Currents	±150 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8T26A, DS8T28	4.75	5.25	V
DS8T26AM, DS8T28M	4.5	5.5	V
Temperature (T_A)			
DS8T26A, DS8T28	0	70	°C
DS8T26AM, DS8T28M	−55	+125	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER						
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			200	µA
I_{IL}	Low Level Input Current (Disabled)	$V_{IN} = 0.4V$			−25	µA
I_{IH}	High Level Input Current (D_{IN}, D_E)	$V_{IN} = V_{CC}$ Max			25	µA
V_{OL}	Low Level Output Voltage (Pins 3, 6, 10, 13)	$I_{OUT} = 48$ mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 3, 6, 10, 13)	$I_{OUT} = -10$ mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 3, 6, 10, 13)	$V_{OUT} = 0V$, $V_{CC} = V_{CC}$ Max	−50		−150	mA
RECEIVER						
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−200	µA
I_{IH}	High Level Input Current (R_E)	$V_{IN} = V_{CC}$ Max			25	µA
V_{OL}	Low Level Output Voltage	$I_{OUT} = 20$ mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 2, 5, 11, 14)	$I_{OUT} = -100$ µA	3.5			V
		$I_{OUT} = -2$ mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 2, 5, 11, 14)	$V_{OUT} = 0V$, $V_{CC} = V_{CC}$ Max	−30		−75	mA
BOTH DRIVER AND RECEIVER						
V_{TL}	Low Level Input Threshold Voltage	$V_{CC} =$ Min, $V_{IN} = 0.8V$, $I_{OL} =$ Max	0.85			V
V_{TH}	High Level Input Threshold Voltage	$V_{CC} =$ Max, $V_{IN} = 0.8V$, $I_{OH} =$ Max			2	V
I_{OZ}	Low Level Output OFF Leakage Current	$V_{OUT} = 0.5V$			−100	µA
I_{OZ}	High Level Output OFF Leakage Current	$V_{OUT} = 2.4V$			100	µA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA			−1.0	V
I_{CC}	Power Supply Current DS8T26A	$V_{CC} = V_{CC}$ Max			87	mA
	DST28	$V_{CC} = V_{CC}$ Max			110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS8T26AM, DS8T28M and across the 0°C to +70°C range for the DS8T26A, DS8T28. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

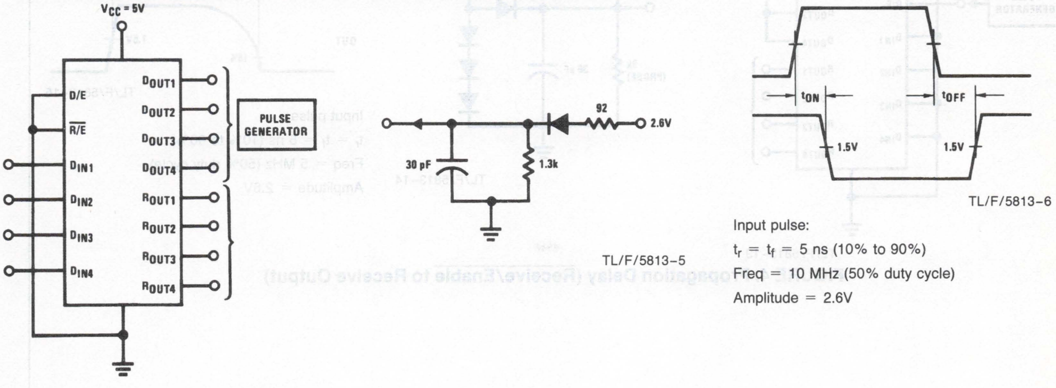
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	DS8T26A Max	DS8T28 Max	Units
Propagation Delay					
t_{ON}	D_{OUT} to R_{OUT}, *(Figure 1)*	$C_L = 30$ pF	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}, *(Figure 1)*		14	17	ns
t_{ON}	D_{IN} to D_{OUT}, *(Figure 2)*	$C_L = 300$ pF	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}, *(Figure 2)*		14	17	ns
Data Enable to Data Output					
t_{PZL}	High Z to 0, *(Figure 3)*	$C_L = 300$ pF	25	28	ns
t_{PLZ}	0 to High Z, *(Figure 3)*		20	23	ns
Receiver Enable to Receiver Output					
t_{PZL}	High Z to 0, *(Figure 4)*	$C_L = 30$ pF	20	23	ns
t_{PLZ}	0 to High Z, *(Figure 4)*		15	18	ns

AC Test Circuits and Switching Time Waveforms



$V_{CC} = 5V$
D/E
R/E
D_{IN1}
D_{IN2}
D_{IN3}
D_{IN4}
D_{OUT1}
D_{OUT2}
D_{OUT3}
D_{OUT4}
R_{OUT1}
R_{OUT2}
R_{OUT3}
R_{OUT4}
PULSE GENERATOR
92
2.6V
30 pF
1.3k
t_{ON}
t_{OFF}
1.5V
1.5V

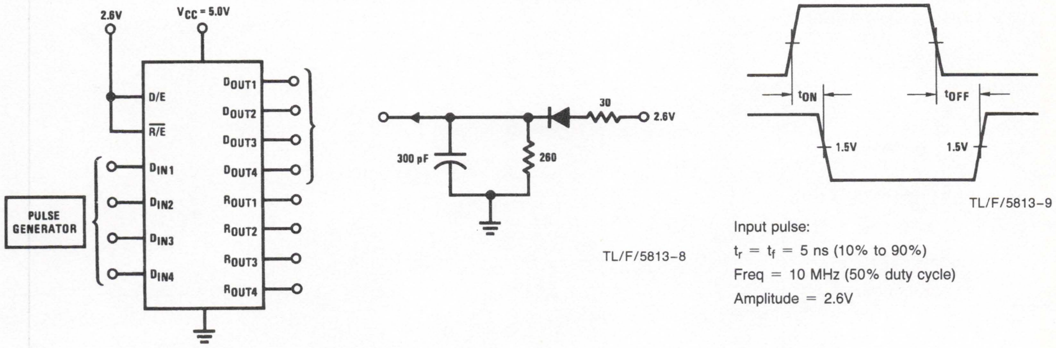
TL/F/5813-4

TL/F/5813-5

TL/F/5813-6

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 1. Propagation Delay (D_{OUT} to R_{OUT})



2.6V
$V_{CC} = 5.0V$
D/E
R/E
D_{IN1}
D_{IN2}
D_{IN3}
D_{IN4}
D_{OUT1}
D_{OUT2}
D_{OUT3}
D_{OUT4}
R_{OUT1}
R_{OUT2}
R_{OUT3}
R_{OUT4}
PULSE GENERATOR
30
2.6V
300 pF
260
t_{ON}
t_{OFF}
1.5V
1.5V

TL/F/5813-7

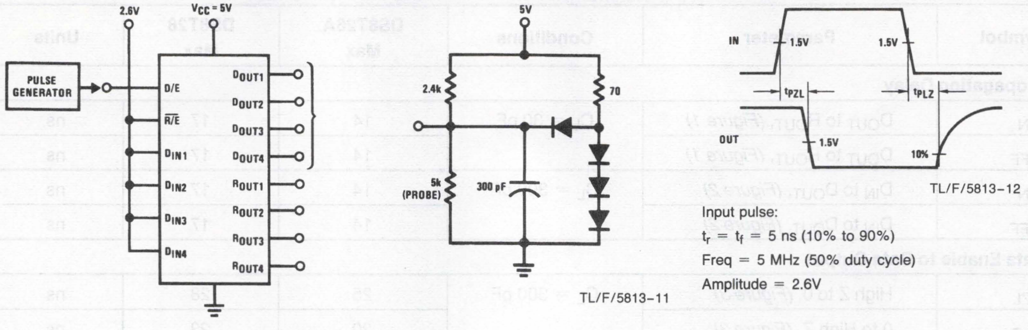
TL/F/5813-8

TL/F/5813-9

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 2. Propagation Delay (D_{IN} to D_{OUT})

AC Test Circuits and Switching Time Waveforms (Continued)


2.6V
VCC = 5V
PULSE GENERATOR
D/E
R/E
DIN1
DIN2
DIN3
DIN4
DOUT1
DOUT2
DOUT3
DOUT4
ROUT1
ROUT2
ROUT3
ROUT4
5V
2.4k
70
5k (PROBE)
300 pF
IN
1.5V
1.5V
tPZL
tPLZ
OUT
1.5V
10%

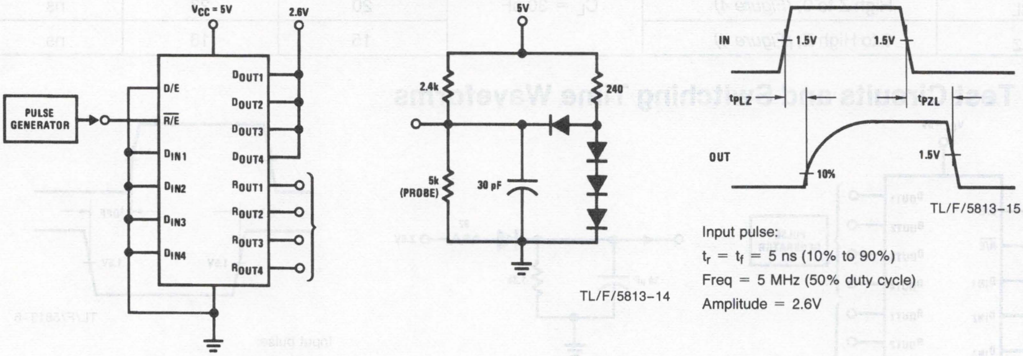
TL/F/5813-10

TL/F/5813-11

TL/F/5813-12

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 3. Propagation Delay (Data Enable to Data Output)


VCC = 5V
2.6V
PULSE GENERATOR
D/E
R/E
DIN1
DIN2
DIN3
DIN4
DOUT1
DOUT2
DOUT3
DOUT4
ROUT1
ROUT2
ROUT3
ROUT4
5V
2.4k
240
5k (PROBE)
30 pF
IN
1.5V
1.5V
tPLZ
tPZL
OUT
1.5V
10%

TL/F/5813-13

TL/F/5813-14

TL/F/5813-15

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 4. Propagation Delay ($\overline{\text{Receive/Enable}}$ to Receive Output)

Section 3

Peripheral Power Drivers

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National Semiconductor

Peripheral/Power Drivers

Peripheral/power drivers is a broad definition given to interface power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage and are driven by standard logic gates. They serve many applications including relay drivers, printer hammer drivers, lamp drivers, bus drivers, core memory drivers, voltage level translators, stepper motor drivers and solenoid drivers.

Unlike standard logic devices, peripheral drivers have many varied load situations depending on the application. This requires the design engineer to interpret device specifications in greater detail. Designers at National Semiconductor have incorporated many technically advanced and useful features into their broad line of peripheral driver devices.

Some of these features include:

- Short circuit protection at individual outputs
- Glitch-free power up/down
- Fail-safe operation
- Inductive fly-back protection
- Negative transient protection
- High input impedance for CMOS/NMOS compatibility

For further information on National Semiconductor's broad line of peripheral drivers, refer to the selection guide to follow and application notes within this section.

PERIPHERAL/POWER DRIVERS

Device Number and Temperature Range		Drivers/ Package	Logic Function (Driver On)	Input Compatibility (Logic)	Output High Voltage (V)	Latch-Up Voltage (Note 3) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	On Power Supply Current (mA)	Page No.
0°C to +70°C	−55°C to +125°C										
DP8310	DP7310	8	(Note 5)	TTL	30		0.5	100	40	152	3-5
DP8311	DP7311	8	(Note 6)	TTL	30		0.5	100	40	125	3-5
DS2001C		7	NAND	TTL	50		1.6	350	5000		3-65
µA9665C											3-65
DS2002C	DS2002M	7	NAND	PMOS	50		1.6	350	5000		3-65
µA9666C	µA9666M										3-65
DS2003C	DS2003M	7	NAND	TTL/CMOS	50		1.6	350	5000		3-65
µA9667C	µA9667M										3-65
DS2004C	DS2004M	7	NAND	CMOS/PMOS	50		1.6	350	5000		3-65
µA9668C	µA9668M										3-65
DS3631	DS1631	2	AND	CMOS	56	40	1.4	300	150	8	3-12
DS3632	DS1632	2	NAND	CMOS	56	40	1.4	300	150	8	3-12
DS3633	DS1633	2	OR	CMOS	56	40	1.4	300	150	8	3-12
DS3634	DS1634	2	NOR	CMOS	56	40	1.4	300	150	8	3-12
DS3654		10	(Note 2)	(Note 2)	(Note 1)	45	1.6	250	1000	70	3-17
DS3656		4	NAND	TTL/LS	65	30	1.5	600		65	3-21
DS3658		4	NAND	TTL/LS	70	35	0.7	600	2430	65	3-23
DS3668		4	NAND	TTL/LS	70	(Note 7)	1.5	600	2000	80	3-26
DS3669		4	AND	TTL/LS	70	35	0.7	600		65	3-29
DS3680		4	(Note 4)	TTL/CMOS	−2.1	−60	−60	−50	10,000	4.4	3-32
DS3686		2	NAND	TTL/CMOS	(Note 1)	56	1.3	300	1000	28	3-35
DS3687	DS1687	2	NAND	TTL/CMOS	(Note 1)	−56	−1.3	300	1000	2.8	3-38
DS75450		2	AND	TTL	30	20	0.7	300	31	55	3-41
DS75451	DS55451	2	AND	TTL	30	20	0.7	300	31	55	3-41
DS75452	DS55452	2	NAND	TTL	30	20	0.7	300	31	55	3-41
DS75453	DS55453	2	OR	TTL	30	20	0.7	300	31	55	3-41
DS75454	DS55454	2	NOR	TTL	30	20	0.7	300	31	55	3-41
DS75461	DS55461	2	AND	TTL	35	30	0.7	300	33	55	3-57
DS75462	DS55462	2	NAND	TTL	35	30	0.7	300	33	55	3-57
DS75463	DS55463	2	OR	TTL	35	30	0.7	300	33	55	3-57
DS75464	DS55464	2	NOR	TTL	35	30	0.7	300	33	55	3-57
MM74C908,		2	AND	CMOS	13.5	15	$V_{CC} - 1.8$	300	150	0.015	CMOS
MM74C918											CMOS

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascaded to be a 20 or 30-bit shift register.

Note 3: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 4: DS3680 has a differential input circuit.

Note 5: DS8310 inverting, positive edge latching.

Note 6: DS8311 inverting, fall through latch.

Note 7: DS3668 35V, latch-up with output fault protection.

National Semiconductor

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30V. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are positive edge latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

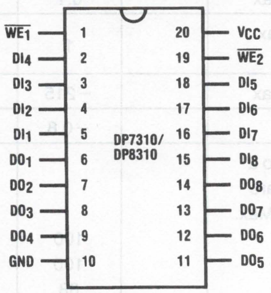
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

Connection Diagrams

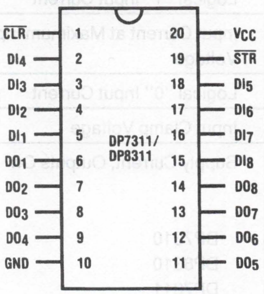
Dual-In-Line Package


WE1 1
DI4 2
DI3 3
DI2 4
DI1 5
DO1 6
DO2 7
DO3 8
DO4 9
GND 10
20 VCC
19 WE2
18 DI5
17 DI6
16 DI7
15 DI8
14 DO8
13 DO7
12 DO6
11 DO5
DP7310/DP8310

TL/F/5246-1

Top View

Dual-In-Line Package


CLR 1
DI4 2
DI3 3
DI2 4
DI1 5
DO1 6
DO2 7
DO3 8
DO4 9
GND 10
20 VCC
19 STR
18 DI5
17 DI6
16 DI7
15 DI8
14 DO8
13 DO7
12 DO6
11 DO5
DP7311/DP8311

TL/F/5246-2

Top View

Order Number DP7310J, DP7311J, DP8310J, DP8311J, DP8310N or DP8311N

See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
DP8310/DP8311	2005 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 12.1 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = Min.				
	DP7310/DP7311	I_{OL} = 75 mA			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = Min.				
	DP7310/DP7311	V_{OH} = 25V			500	µA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	µA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = Max		0.1	25	µA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = Max		1	250	µA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = Max		−215	−300	µA
V_{clamp}	Input Clamp Voltage	I_{IN} = 12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All Inputs are at logical "1", V_{CC} = Max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: V_{CC} = 4.5V, T_A = −55°C to +125°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	*(Figure 1)*		40	120	ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	*(Figure 1)*		70	150	ns
t_{SETUP}	Minimum Set-Up Time Data in to Write Enable Input	t_{HOLD} = 0 ns *(Figure 1)*	45	20		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	*(Figure 1)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 1)*		16	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 1)*		38	70	ns
C_{IN}	"N" Package (Note 4)			5	15	pF

AC Electrical Characteristics DP7311/DP8311: V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	*(Figure 2)*		30	60	ns
t_{pd1}	Low to High Propagation Delay Data to Output	*(Figure 2)*	70	100		ns
t_{SETUP}	Minimum Set-Up Time Data in to Strobe Input	t_{HOLD} = 0 ns *(Figure 2)*	0	−25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	*(Figure 2)*	60	35		ns
t_{pdC}	Propagation Delay Clear to Data Output	*(Figure 2)*		70	135	ns
t_{pWC}	Minimum Clear Input Pulse Width	*(Figure 2)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 2)*		20	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 2)*		38	60	ns
C_{IN}	Input Capacitance—Any Input	(Note 4)		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Input capacitance is guaranteed by periodic testing. f_{TEST} = 10 kHz at 300 mV, T_A = 25°C.

Logic Table

DP7310/DP8310

Write Enable 1 $\overline{WE_1}$	Write Enable 2 $\overline{WE_2}$	Data Input DI_{1-8}	Data Output DO_{1-8}
0	0	X	Q
0	↗	0	1
0	↗	1	0
↗	0	0	1
↗	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

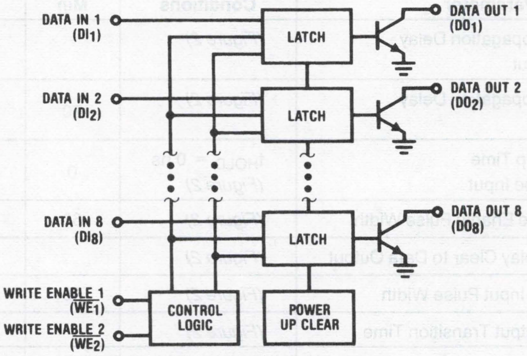
DP7311/DP8311

Clear $\overline{CLR}$	Strobe $\overline{STR}$	Data Input DI_{1-8}	Data Output DO_{1-8}
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↗ = Positive Edge Transition

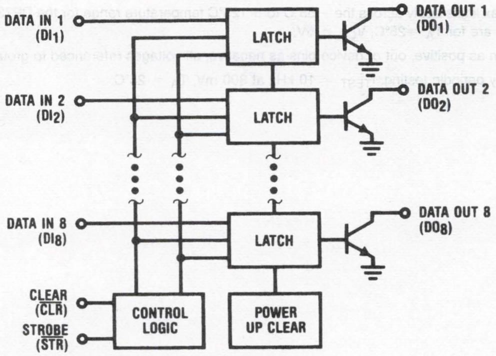
Block Diagrams

DP7310/DP8310


DATA IN 1 (DI_1)
DATA IN 2 (DI_2)
DATA IN 8 (DI_8)
WRITE ENABLE 1 ($\overline{WE_1}$)
WRITE ENABLE 2 ($\overline{WE_2}$)
LATCH
LATCH
LATCH
CONTROL LOGIC
POWER UP CLEAR
DATA OUT 1 (DO_1)
DATA OUT 2 (DO_2)
DATA OUT 8 (DO_8)

TL/F/5246-3

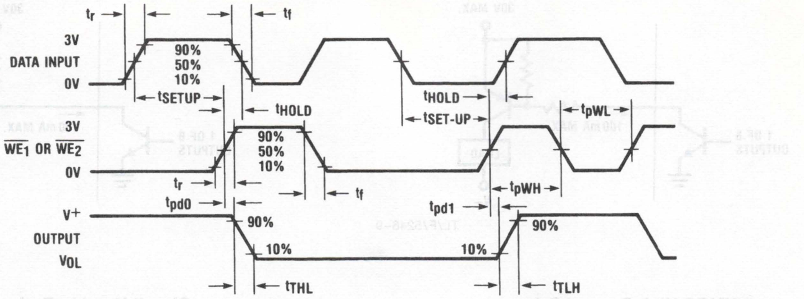
DP7311/DP8311


DATA IN 1 (DI_1)
DATA IN 2 (DI_2)
DATA IN 8 (DI_8)
CLEAR ($\overline{CLR}$)
STROBE ($\overline{STR}$)
LATCH
LATCH
LATCH
CONTROL LOGIC
POWER UP CLEAR
DATA OUT 1 (DO_1)
DATA OUT 2 (DO_2)
DATA OUT 8 (DO_8)

TL/F/5246-4

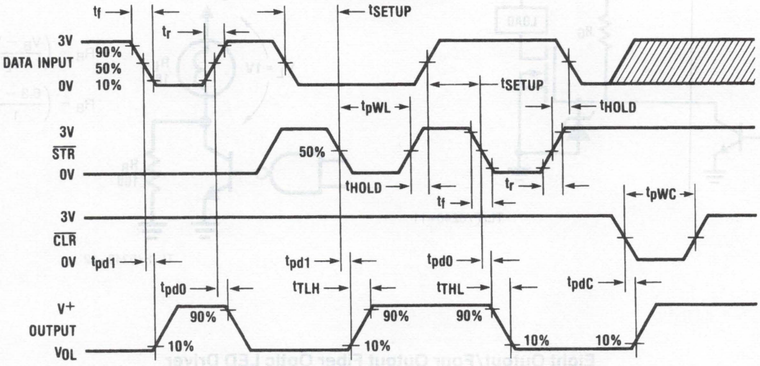
Switching Time Waveforms

DP7310/DP8310


tr
tf
3V
DATA INPUT
0V
90%
50%
10%
tSETUP
tHOLD
tHOLD
tSET-UP
tpWL
3V
WE1 OR WE2
0V
tr
tf
tpWH
tpd0
tpd1
V+
OUTPUT
VOL
90%
10%
10%
90%
tTHL
tTLH

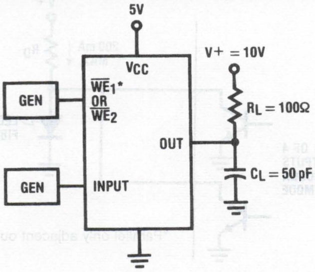
TL/F/5246-5

DP7311/DP8311


tf
tr
tSETUP
3V
DATA INPUT
0V
90%
50%
10%
tSETUP
tpWL
tHOLD
3V
STR
0V
50%
tHOLD
tf
tr
tpWC
3V
CLR
0V
tpd1
tpd1
tpd0
tpd0
tTLH
tTHL
tpdC
V+
OUTPUT
VOL
90%
10%
90%
10%
90%
10%
10%

TL/F/5246-6

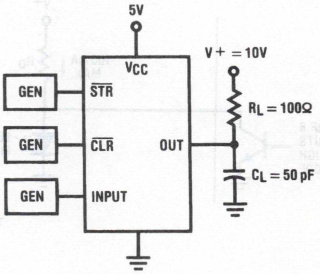
Switching Time Test Circuits


5V
VCC
V+ = 10V
GEN
WE1*
OR
WE2
RL = 100Ω
OUT
GEN
INPUT
CL = 50 pF

TL/F/5246-7

*$\overline{WE}_1$ = 0V When the Input = $\overline{WE}_2$

FIGURE 1. DP7310/DP8310


5V
VCC
V+ = 10V
GEN
STR
RL = 100Ω
GEN
CLR
OUT
CL = 50 pF
GEN
INPUT

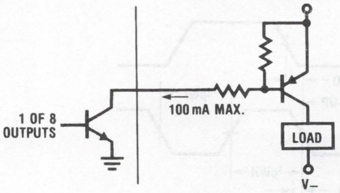
TL/F/5246-8

Pulse Generator Characteristics:
$Z_O = 50\Omega$, $t_r = t_f = 5$ ns

FIGURE 2. DP7311/DP8311

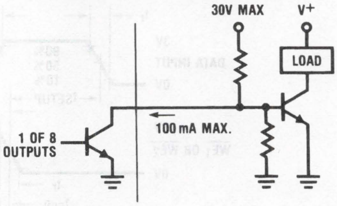
Typical Applications DP8310/11 Buffering High Current Device (Notes 1 and 2)

PNP High Current Driver


30V MAX.
100 mA MAX.
1 OF 8
OUTPUTS
LOAD
V−

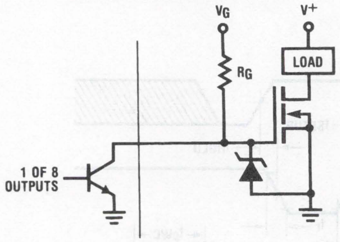
TL/F/5246-9

NPN High Current Driver


30V MAX
V+
LOAD
1 OF 8
OUTPUTS
100 mA MAX.

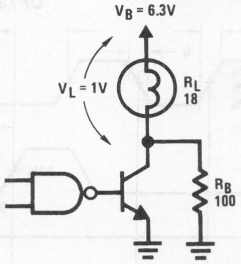
TL/F/5246-10

VMOS High Current Driver


VG
V+
RG
LOAD
1 OF 8
OUTPUTS

TL/F/5246-11

Circuit Used to Reduce Peak Transient Lamp Current


VB = 6.3V
VL = 1V
RL
18
RB
100

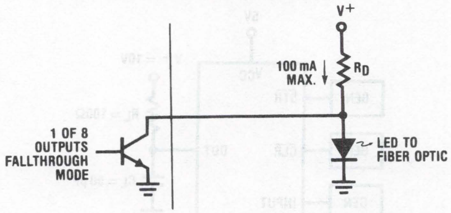
$$R_B = \left(\frac{V_B - V_L}{V_L}\right) R_L$$

$$R_B = \left(\frac{6.3 - 1}{1}\right) 18\Omega = 95.4 \approx 100\Omega$$

TL/F/5246-12

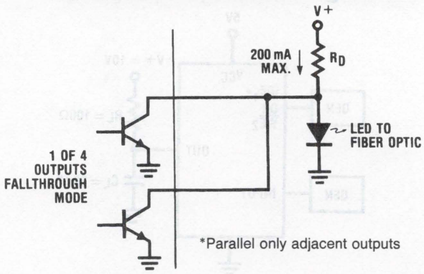
Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers


V+
100 mA
MAX.
RD
LED TO
FIBER OPTIC
1 OF 8
OUTPUTS
FALLTHROUGH
MODE

TL/F/5246-13

DP8311 Parallel Outputs (200 mA) Drivers*

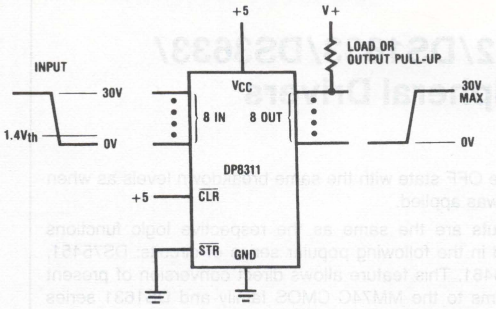

V+
200 mA
MAX.
RD
LED TO
FIBER OPTIC
1 OF 4
OUTPUTS
FALLTHROUGH
MODE

*Parallel only adjacent outputs

TL/F/5246-14

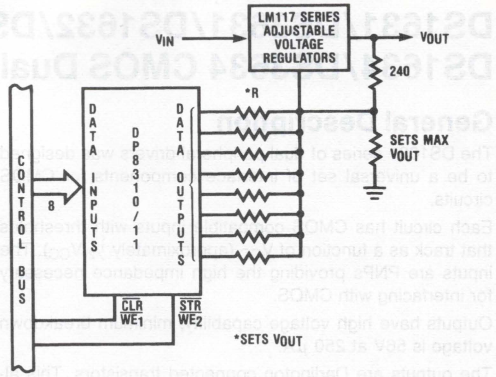
Typical Applications (Continued)

8-Bit Level Translator-Driver


+5
V+
LOAD OR
OUTPUT PULL-UP
INPUT
30V
1.4V
0V
VCC
8 IN
8 OUT
30V
MAX
0V
DP8311
+5
CLR
STR
GND

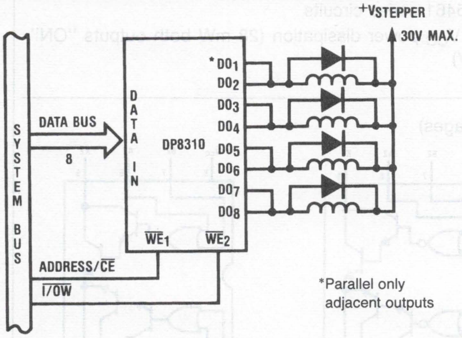
TL/F/5246-15

Digital Controlled 256 Level Power Supply from 1.2V to 30V


LM117 SERIES
ADJUSTABLE
VOLTAGE
REGULATORS
VIN
VOUT
240
*R
SETS MAX
VOUT
CONTROL BUS
8
DATA INPUTS
DP8310/1
DATA OUTPUTS
CLR
WE1
STR
WE2
*SETS VOUT

TL/F/5246-16

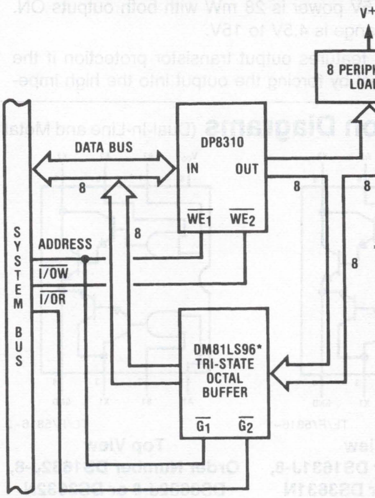
200 mA Drive for a 4 Phase Bifilar Stepper Motor


+VSTEPPER
30V MAX.
*DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
DATA IN
DP8310
DATA BUS
8
SYSTEM BUS
WE1
WE2
ADDRESS/CE
I/OW

*Parallel only adjacent outputs

TL/F/5246-17

Reading the State of the Latched Peripherals


V+
8 PERIPHERAL
LOADS
DATA BUS
DP8310
IN
OUT
8
8
8
WE1
WE2
8
SYSTEM BUS
ADDRESS
I/OW
I/OR
8
DM81LS96*
TRI-STATE
OCTAL
BUFFER
G1
G2

*High Level Input Voltage must not Exceed V_{CC} of the DM81LS96

TL/F/5246-18

Note 1: Always use good V_{CC} bypass and ground techniques to suppress transients caused by peripheral loads.

Note 2: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).

National Semiconductor

DS1631/DS3631/DS1632/DS3632/DS1633/DS3633/DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately ½ V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250 μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

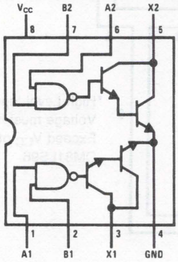
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL compatible at V_{CC} = 5V.

Features

■ CMOS compatible inputs	
■ High impedance inputs	PNP's
■ High output voltage breakdown	56V min
■ High output current capability	300 mA max
■ Same pin-outs and logic functions as DS75451 and DS75461 series circuits	
■ Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)	

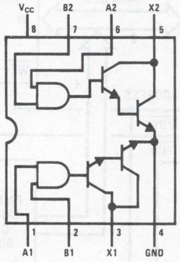
Connection Diagrams (Dual-In-Line and Metal Can Packages)



TL/F/5816–1

Top View

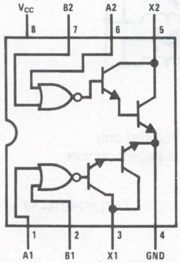
Order Number DS1631J-8, DS3631J-8 or DS3631N



TL/F/5816–2

Top View

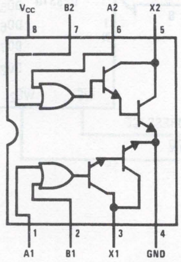
Order Number DS1632J-8, DS3632J-8 or DS3632N



TL/F/5816–3

Top View

Order Number DS1633J-8, DS3633J-8 or DS3633N

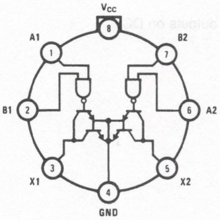


TL/F/5816–4

Top View

Order Number DS1634J-8, DS3634J-8 or DS3634N

See NS Package Number J08A or N08E

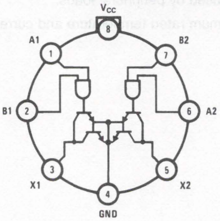


TL/F/5816–5

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1631H or DS3631H

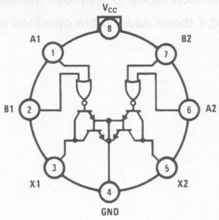


TL/F/5816–6

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1632H or DS3632H

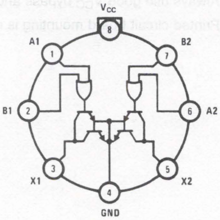


TL/F/5816–7

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1633H or DS3633H



TL/F/5816–8

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1634H or DS3634H

See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} + 0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
ALL CIRCUITS								
V_{IH}	Logical “1” Input Voltage	(*Figure 1*)	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical “0” Input Voltage	(*Figure 1*)	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical “1” Input Current	V_{CC} = 15V, V_{IN} = 15V, (*Figure 2*)				0.1	10	μA
I_{IL}	Logical “0” Input Current	V_{IN} = 0.4V, (*Figure 3*)	V_{CC} = 5V			−50	−120	μA
			V_{CC} = 15V			−200	−360	μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250 μA, (*Figure 1*)			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, (*Figure 1*), DS1631, DS1632, DS1633, DS1634	I_{OL} = 100 mA			0.85	1.1	V
			I_{OL} = 300 mA			1.1	1.4	V
		V_{CC} = Min, (*Figure 1*), DS3631, DS3632, DS3633, DS3634	I_{OL} = 100 mA			0.85	1.0	V
			I_{OL} = 300 mA			1.1	1.3	V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7	11	mA
			V_{CC} = 15V	Both Drivers		14	20	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	3	mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5	10	mA
t_{PD1}	Propagation to “1”	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to “0”	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		8	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		2.5	3.5	mA
			V_{CC} = 15V			9	14	mA
t_{PD1}	Propagation to “1”	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to “0”	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

Electrical Characteristics (Notes 2 and 3) (Continued)

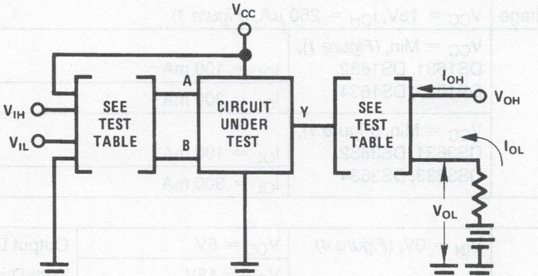
Symbol	Parameter	Conditions			Min	Typ	Max	Units
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V			16	23	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	4	mA
			V_{CC} = 15V, V_{IN} = 15V			7.2	15	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		3	5	mA
			V_{CC} = 15V			11	18	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Test Circuits



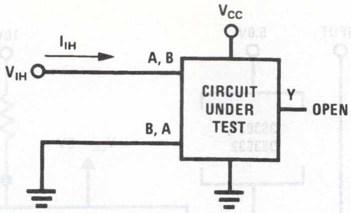
TL/F/5816-9

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS3631	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS3632	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
DS3633	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS3634	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

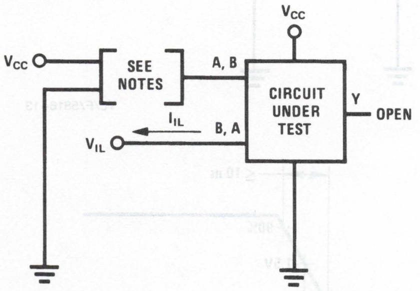
Test Circuits (Continued)


V_{CC}
I_{IH}
A, B
V_{IH}
CIRCUIT UNDER TEST
Y
OPEN
B, A

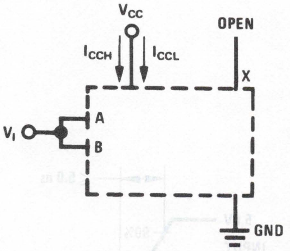
TL/F/5816-10

Each input is tested separately.

FIGURE 2. I_{IH}


V_{CC}
V_{CC}
SEE NOTES
A, B
CIRCUIT UNDER TEST
Y
OPEN
I_{IL}
B, A
V_{IL}

TL/F/5816-11


V_{CC}
OPEN
I_{CCH}
I_{CCL}
X
V_I
A
B
GND

TL/F/5816-12

Both gates are tested simultaneously.

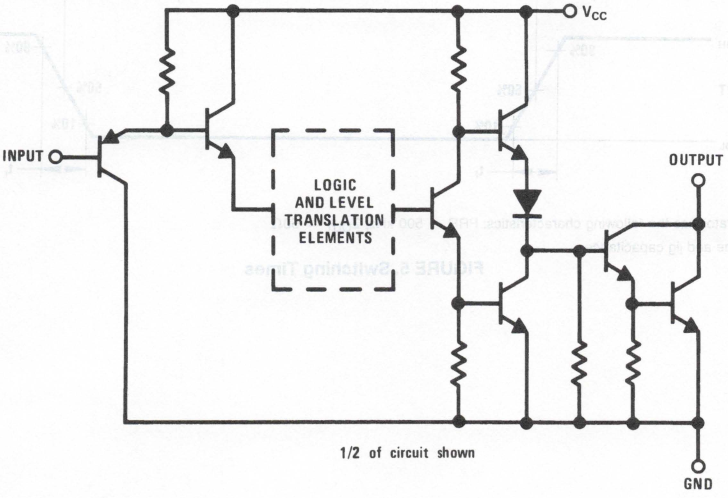
FIGURE 4. I_{CC} for AND and NAND Circuits

Note A: Each input is tested separately.

Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

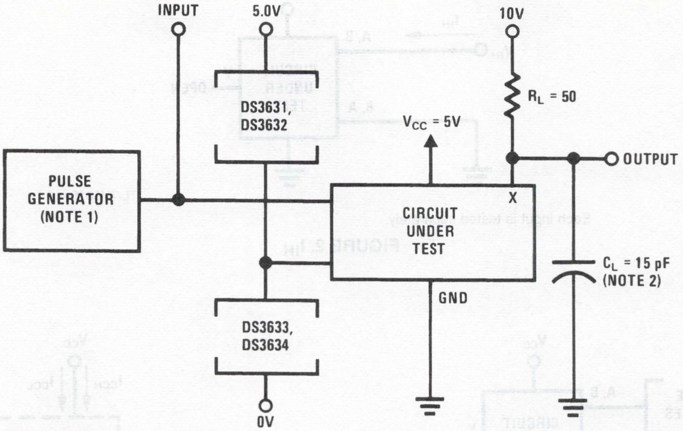
FIGURE 3. I_{IL}

Schematic Diagram (Equivalent Circuit)

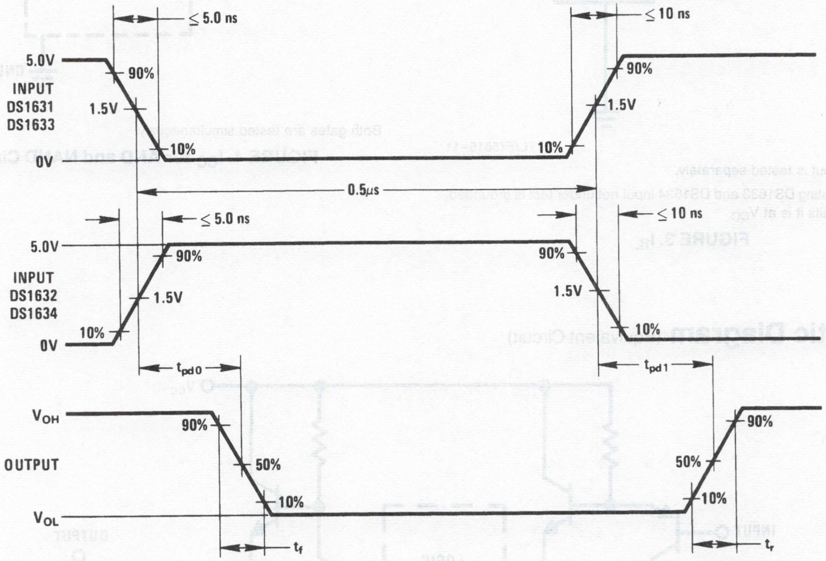

V_{CC}
INPUT
LOGIC AND LEVEL TRANSLATION ELEMENTS
OUTPUT
1/2 of circuit shown
GND

TL/F/5816-15

Switching Time Waveforms


INPUT
5.0V
10V
DS3631,
DS3632
R_L = 50
V_{CC} = 5V
OUTPUT
PULSE
GENERATOR
(NOTE 1)
X
CIRCUIT
UNDER
TEST
GND
C_L = 15 pF
(NOTE 2)
DS3633,
DS3634
0V

TL/F/5816–13


≤ 5.0 ns
≤ 10 ns
5.0V
90%
INPUT
DS1631
DS1633
1.5V
10%
0V
90%
1.5V
10%
0.5μs
≤ 5.0 ns
≤ 10 ns
5.0V
90%
INPUT
DS1632
DS1634
1.5V
10%
0V
90%
1.5V
10%
t_{pd0}
t_{pd1}
V_{OH}
90%
OUTPUT
50%
10%
V_{OL}
t_f
90%
50%
10%
t_r

TL/F/5816–14

Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$

Note 2: C_L includes probe and jig capacitance

FIGURE 5. Switching Times

National Semiconductor

DS3654 Printer Solenoid Driver

General Description

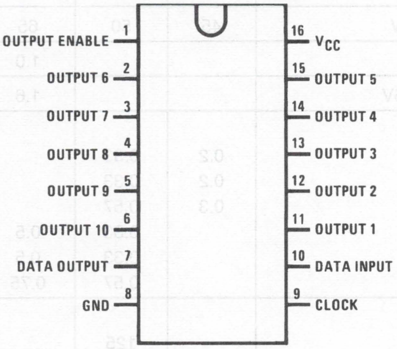
The DS3654 is a serial-to-parallel 10-bit shift register with a clock and data input, a data output from the tenth bit, and 10 open-collector clamped relay driver outputs suitable for driving printer solenoids.

Timing for the circuit is shown in *Figure 1*. Data input is sampled on the positive clock edge. Data output changes on the negative clock edge, and is always active. Enable transfers data from the shift register to the open-collector outputs. Internal circuitry inhibits output enable for power supply voltage less than 6V.

Each output sinks 250 mA and is internally clamped to ground at 50V to dissipate energy stored in inductive loads.

Connection Diagram

Dual-In-Line Package


OUTPUT ENABLE 1
OUTPUT 6 2
OUTPUT 7 3
OUTPUT 8 4
OUTPUT 9 5
OUTPUT 10 6
DATA OUTPUT 7
GND 8
16 VCC
15 OUTPUT 5
14 OUTPUT 4
13 OUTPUT 3
12 OUTPUT 2
11 OUTPUT 1
10 DATA INPUT
9 CLOCK

TL/F/5817–1

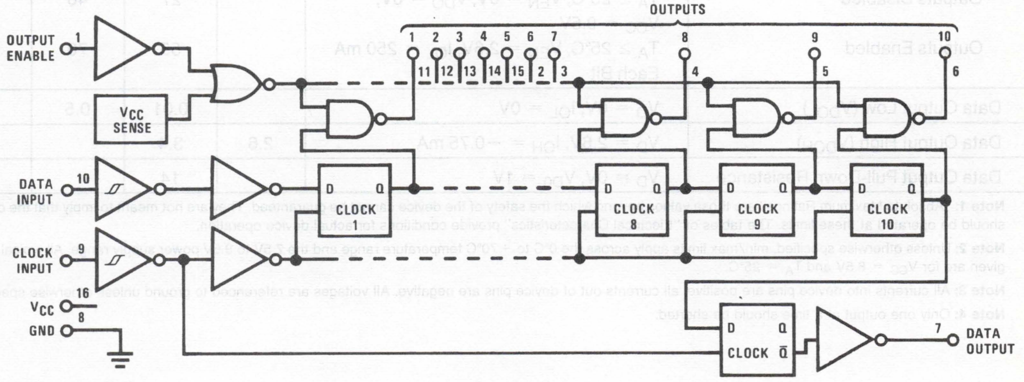
Top View

Order Number DS3654J or DS3654N
See NS Package Number J16A or N16A

Pin Descriptions

Pin No.	Function
1	Output Enable
2	Output 6
3	Output 7
4	Output 8
5	Output 9
6	Output 10
7	Data Output
8	Ground
9	Clock Input
10	Data Input
11	Output 1
12	Output 2
13	Output 3
14	Output 4
15	Output 5
16	V_{CC}

Logic Diagram


OUTPUT ENABLE 1
VCC SENSE
DATA INPUT 10
CLOCK INPUT 9
VCC 16
GND 8
OUTPUTS
1 2 3 4 5 6 7
11 12 13 14 15 2 3
8 4
9 5
10 6
D Q CLOCK 1
D Q CLOCK 8
D Q CLOCK 9
D Q CLOCK 10
D Q CLOCK Q̄
7 DATA OUTPUT

TL/F/5817–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	9.5V Max
Input Voltage	−0.5V Min. 9.5V Max
Output Supply, Vp-p	45V Max
Storage Temperature Range	−65°C to +150°C
Output Current (Single Output)	0.4A
Ground Current	4.0A
Peak Power Dissipation $t < 10$ ms, Duty Cycle $< 5\%$	4.5W Max
Maximum Power Dissipation* at 25°C	
Cavity Package	1635 mW
Molded Package	1687 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.9 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	7.5	9.5	V
Temperature (T_A)	0	+70	°C
Output Supply (Vp-p)		40	V

Electrical Characteristics (Notes 2, 3 and 4) Vp-p = 30V unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage		2.6			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage Clamp	$I_{CLAMP} = 0.1A$, $V_{EN} = 0V$	45	50	65	V
Logical "1" Output Current	$V_{OH} = 40V$, $V_{EN} = 0V$			1.0	mA
Logical "0" Output Current	$I_{OL} = 250$ mA, $V_{EN} = 2.6V$			1.6	V
Logical "1" Input Current					
Clock	$T_A = 70°C$, $V_{CL} = 2.6V$	0.2	0.33		mA
Enable	$T_A = 70°C$, $V_{EN} = 2.6V$	0.2	0.33		mA
Data	$T_A = 70°C$, $V_D = 2.6V$	0.3	0.57		mA
Clock	$T_A = 0°C$, $V_{CL} = 2.6V$		0.33	0.5	mA
Enable	$T_A = 0°C$, $V_{EN} = 2.6V$		0.33	0.5	mA
Data	$T_A = 0°C$, $V_D = 2.6V$		0.57	0.75	mA
Logical "0" Input Current					
Clock	$T_A = 70°C$, $V_{CL} = 1V$		125		μA
Enable	$T_A = 70°C$, $V_{EN} = 1V$		125		μA
Data	$T_A = 70°C$, $V_D = 1V$		220		μA
Input Pull-Down Resistance					
Clock	$T_A = 25°C$, $V_{CL} < V_{CC}$		8		kΩ
Enable	$T_A = 25°C$, $V_{EN} < V_{CC}$		8		kΩ
Data	$T_A = 25°C$, $V_D < V_{CC}$		4.5		kΩ
Supply Current (I_{CC})					
Outputs Disabled	$T_A \geq 25°C$, $V_{EN} = 0V$, $V_{DO} = 0V$, $V_{CC} = 9.5V$		27	40	mA
Outputs Enabled	$T_A \geq 25°C$, $V_{EN} = 2.6V$, $I_{OL} = 250$ mA Each Bit		55	70	mA
Data Output Low (V_{DOL})	$V_D = 0V$, $I_{OL} = 0V$		0.01	0.5	V
Data Output High (V_{DOH})	V_D 2.6V, $I_{OH} = -0.75$ mA	2.6	3.4		V
Data Output Pull-Down Resistance	$V_D = 0V$, $V_{D0} = 1V$		14		kΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 7.5V to 9.5V power supply range. All typical values given are for $V_{CC} = 8.5V$ and $T_A = 25°C$.

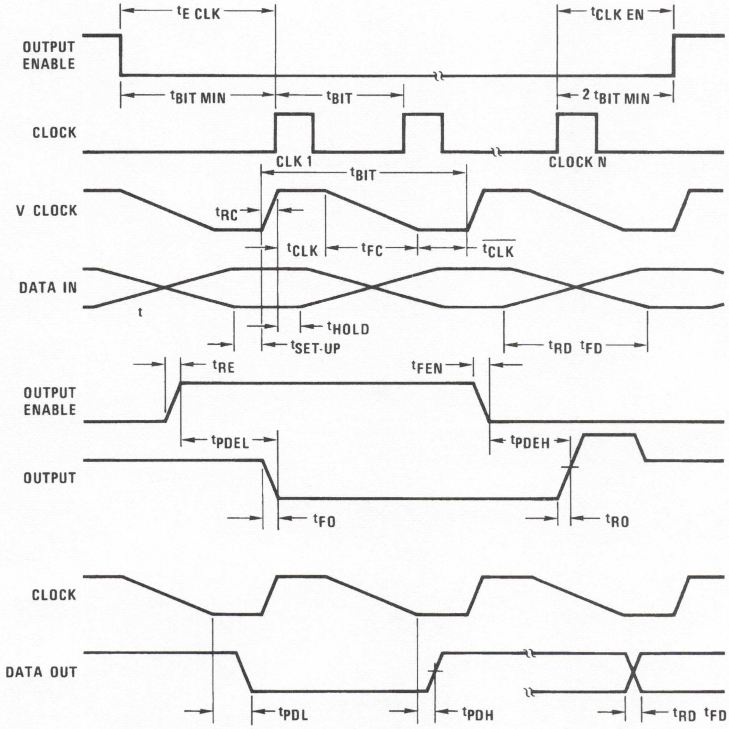
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics 0°C to +70°C, T_A = 25°C, nominal power supplies unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Clk, Data and Enable Inputs	*(Figure 1)*				
t_{FC}				2.0	μs
t_{RC}	$t_{BIT} \geq 10$ μs			2.0	μs
t_{CLK}		2			μs
$\overline{t_{CLK}}$		3.5			μs
t_{HOLD}				1.0	μs
$t_{SET\text{-}UP}$				1.0	μs
t_{RE}, $t_{RD\ IN}$				1.0	μs
t_{FE}, $t_{FD\ IN}$				5.0	μs
Output 1–10	Vp-p = 20V				
t_{RO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{FO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{PDEH}			3.5		μs
t_{PDEL}			3.0		μs
Data Output					
t_{PDH}, t_{PDL}	$R_L = 5\ k\Omega$, $C_L \leq 10$ pF		0.8	2.5	μs
t_{RD}			0.4		μs
t_{FD}			0.4		μs
Clock to Enable Delay					
t_{CE}		2 t_{BIT}			μs
Enable to Clock Delay		t_{BIT}			μs

Switching Time Waveforms



tE CLK
tCLK EN
OUTPUT ENABLE
tBIT MIN
tBIT
2 tBIT MIN
CLOCK
CLK 1
CLOCK N
tBIT
V CLOCK
tRC
tCLK
tFC
tCLK
DATA IN
t
tHOLD
tSET-UP
tRD tFD
tRE
tFEN
OUTPUT ENABLE
tPDEL
tPDEH
OUTPUT
tFO
tRO
CLOCK
DATA OUT
tPDL
tPDH
tRD tFD

TL/F/5817–3

FIGURE 1. Shift Timing

Definition of Terms

Vp-p: Output power supply voltage. The return for open-collector relay driver outputs.

t_{BIT}: Period of the incoming clock.

V_{CLK}: The voltage at the clock input.

t_{CLK}: The portion of t_{BIT} when $V_{CLK} \geq 2.6V$

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$

$t_{SET\text{-}UP}$: The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

t_{HOLD}: The time following the start of t_{CLK} required to transfer data within the shift register.

National Semiconductor

DS3656 Quad Peripheral Driver

General Description

The DS3656 is a quad peripheral driver designed for use in automotive applications. Logically it is an open collector NAND function with all inputs compatible with 74LS and CMOS series products. An enable input is provided that is common to each driver. When taken to a logic zero level all outputs will turn off. Also, overvoltage is detected.

The DS3656 has features associated with the output structure that make it highly versatile to many applications. Each output is capable of 600 mA sink currents and offers 65V standoff voltage in non-inductive applications. A clamp network capable of handling 800 mA is incorporated in each output which eliminates the need of an external network to quench the high voltage backswing caused when switching inductive loads up to 30V (reference AN-213).

The DS3656 is intended to operate from a 12V automotive battery. Internal to the device is its own voltage regulator which permits the device to operate during the wide voltage variation seen in many automotive applications. An overvoltage-protection circuit is incorporated that will cause the outputs to turn off when the supply exceeds 30V. The circuit is designed to withstand worst case fault conditions that occur in automotive applications, such as high voltage transients and reverse battery connection. In this type of environment an external 100Ω resistor must be connected in series with the V_{CC} line.

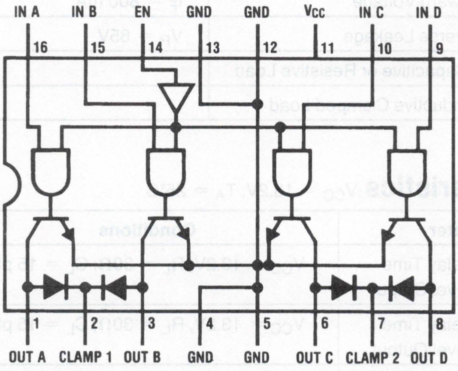
The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a copper PC board the power rating of the device will significantly improve.

Features

- Quad automotive peripheral driver
- 600 mA output current capability
- High voltage outputs—65V
- Clamp diode provided for inductive loads
- Built in regulator
- Overvoltage failsafe
- TTL/LS/CMOS compatible diode clamped inputs
- High power dissipation package
- Guaranteed to withstand worst case fault conditions

Connection Diagram

Dual-In-Line Package



TL/F/5818-1

Top View

Order Number DS3656N
See NS Package Number N16A

Truth Table

Enable	In X	Out X
H	H	L
H	L	H
L	X	H

H = High level L = Low level X = Irrelevant

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 2)	65V
Input Voltage	7V
Output Voltage	65V
Continuous Output Current	1.2A
Junction Temperature	150°C
Thermal Resistance (Junction to Ambient)	
DS3656N Plugged in a Socket	60°C/W
DS3656N Soldered in a PC Board	35°C/W
DS3656N Soldered in a PC Board with 6 in^2 Cn Foil	20°C/W
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	10.5	17.0	V
Temperature	−40	105	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply Voltage		10.5	17	V
I_{CC}	Power Supply Current			65	mA
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.7V$		20	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$		−360	μA
V_{ICL}	Input Clamp Voltage	$I_{IN} = -10$ mA		−1.5	V
V_{OL}	Low Level Output Voltage	$I_L = 600$ mA, $V_{CC} = 10.5V$		1.5	V
I_{OH}	High Level Leakage Current	$V_{OH} = 65V$		1.0	mA
V_F	Output Diode Forward Voltage	$I_F = 800$ mA		2.5	V
I_R	Output Diode Reverse Leakage	$V_R = 65V$		1.0	mA
B_{VCER}	V_{OH1} Switching Capacitive or Resistive Load			65	V
L_{VCEO}	V_{OH2} Switching Inductive Clamped Load			30	V

Switching Characteristics $V_{CC} = 13.2V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{PHL}	Propagation Delay Time High to Low Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{TLH}	Transition Time Low to High Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		500	ns
t_{THL}	Transition Time High to Low Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		500	ns
t_{PLH}	Enable to Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{PHL}	Enable to Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: Unless otherwise specified min/max limits apply across the −40°C to +105°C temperature range.

National Semiconductor

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

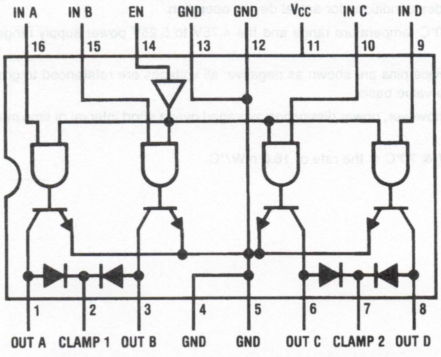
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5819–1

Top View

Order Number DS3658N
See NS Package Number N16A

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	H	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @ 25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = 5.25V, V_{CC} = 5.25V$		1.0	10	μA
I_{IL}	Input Low Current	$V_{IN} = 0.4V$			±10	μA
V_{IK}	Input Clamp Voltage	$I_I = -12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L = 300$ mA		0.2	0.4	V
		$I_L = 600$ mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	$V_{CE} = 70V, V_{IN} = 0.8V$			100	μA
V_F	Diode Forward Voltage	$I_F = 800$ mA		1.0	1.6	V
I_R	Diode Leakage Current	$V_R = 70V$			100	μA
I_{CC}	Supply Current	All Inputs High		50	65	mA
		All Inputs Low		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L = 60\Omega, V_L = 30V$		226	500	ns
t_{LH}	Turn Off Delay	$R_L = 60\Omega, V_L = 30V$		2430	8000	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

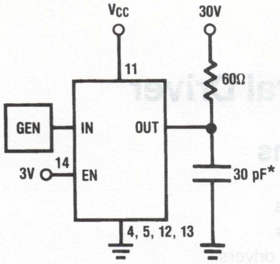
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

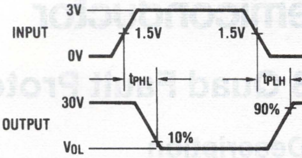
AC Test Circuit


VCC
30V
11
60Ω
GEN
IN
OUT
3V
14
EN
30 pF*
4, 5, 12, 13

TL/F/5819-2

*Includes probe and jig capacitance

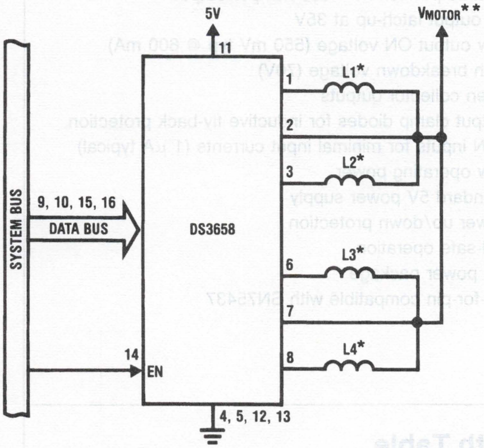
Switching Waveforms


3V
INPUT
1.5V
1.5V
0V
tPHL
tPLH
30V
90%
OUTPUT
10%
VOL

TL/F/5819-3

Typical Applications

Stepping Motor Driver

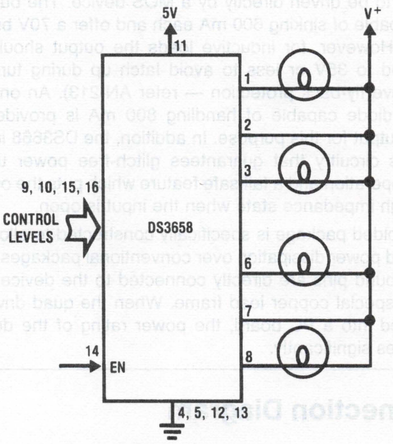

5V
VMOTOR**
11
SYSTEM BUS
1
L1*
2
L2*
3
9, 10, 15, 16
DATA BUS
DS3658
L3*
6
7
L4*
14
EN
8
4, 5, 12, 13

TL/F/5819-4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor

**V_{MOTOR} is the supply voltage of the motor

Lamp Driver


5V
V+
11
1
2
3
9, 10, 15, 16
CONTROL LEVELS
DS3658
6
7
14
EN
8
4, 5, 12, 13

TL/F/5819-5

National Semiconductor

DS3668 Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protection circuit is incorporated on each output. When the load current exceeds 1.0A (approximately) on any output for more than a built-in delay time, nominally 12 μs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 1.0 μs. This built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

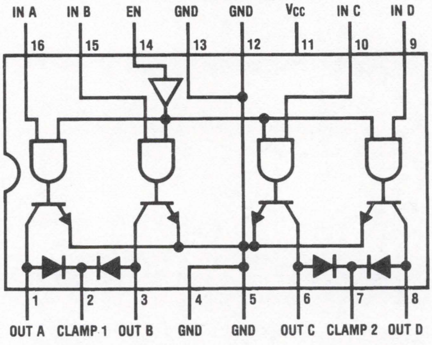
- Relay drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current—600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5225-1

Top View

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

Order Number DS3668N
See NS Package Number N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Continuous Power Dissipation @ 25°C Free-Air(5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = 5.25V, V_{CC} = 5.25V$		1.0	20	μA
I_{IL}	Input Low Current	$V_{IN} = 0.4V$			±10	μA
V_{IK}	Input Clamp Voltage	$I_I = -12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L = 300$ mA		0.2	0.7	V
		$I_L = 600$ mA (Note 4)		0.55	1.5	V
I_{CEX}	Output Leakage Current	$V_{CE} = 70V, V_{IN} = 0.8V$			100	μA
V_F	Diode Forward Voltage	$I_F = 800$ mA		1.2	1.6	V
I_R	Diode Leakage Current	$V_R = 70V$			100	μA
I_{CC}	Supply Current	All Inputs High		62	80	mA
		All Inputs Low		20		mA
I_{TH}	Protection Circuit Threshold Current			1	1.4	A

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L = 60\Omega, V_L = 30V$		0.3	1.0	μs
t_{LH}	Turn Off Delay	$R_L = 60\Omega, V_L = 30V$		2	10.0	μs
t_{FZ}	Protection Enable Delay (after Detection of Fault)		6	12		μs
t_{RL}	Input Low Time for Protection Circuit Reset		1.0			μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

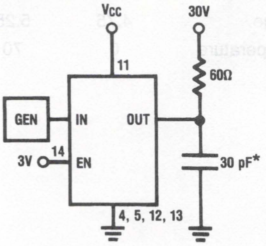
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

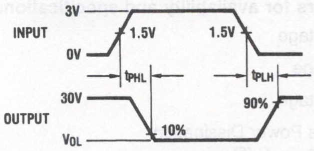
AC Test Circuit


VCC
30V
11
60Ω
GEN
IN
OUT
3V
14
EN
30 pF*
4, 5, 12, 13

TL/F/5225-2

*Includes probe and jig capacitance.

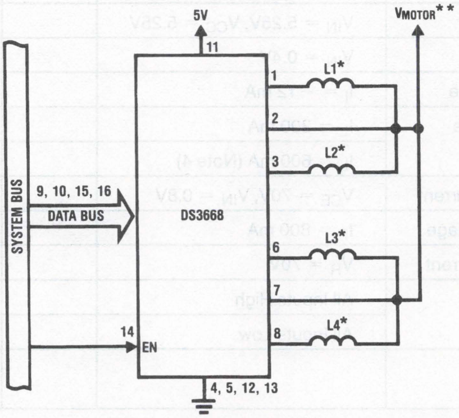
Switching Waveforms


3V
INPUT
1.5V
1.5V
0V
tPHL
tPLH
30V
90%
OUTPUT
10%
VOL

TL/F/5225-3

Typical Application

Stepping Motor Driver

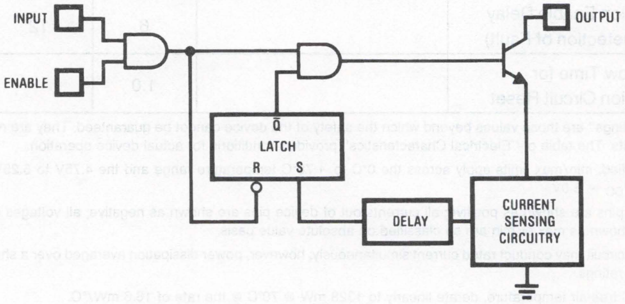

5V
VMOTOR**
11
1
L1*
2
3
L2*
SYSTEM BUS
9, 10, 15, 16
DATA BUS
DS3668
6
L3*
7
14
EN
8
L4*
4, 5, 12, 13

TL/F/5225-4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Protection Circuit Block Diagram


INPUT
ENABLE
OUTPUT
Q̄
LATCH
R
S
DELAY
CURRENT
SENSING
CIRCUITRY

TL/F/5225-5

National Semiconductor

DS3669 Quad High Current Peripheral Driver

General Description

The DS3669 is a non-inverting quad peripheral driver similar to the DS3658. These drivers are designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3669 incorporates circuitry that guarantees glitch-free power up or down operation.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

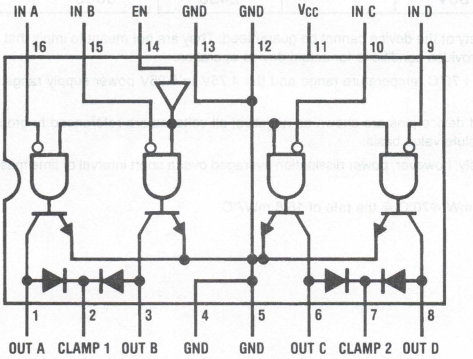
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- 2W power package

Connection Diagram

Dual-In-Line Package



TL/F/5820-1

Top View

Order Number DS3669N
See NS Package Number N16A

Truth Table

IN	EN	OUT
L	H	L
H	H	Z
L	L	Z
H	L	Z

H = High state
L = Low state
Z = High impedance state

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = 5.25V$, $V_{CC} = 5.25V$		1.0	10	µA
I_{IL}	Input Low Current	$V_{IN} = 0.4V$			±10	µA
V_{IK}	Input Clamp Voltage	$I_I = -12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L = 300$ mA		0.2	0.4	V
		$I_L = 600$ mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	$V_C = 70V$, $V_{IN} = 2V$, $V_{EN} = 0.8V$			100	µA
V_F	Diode Forward Voltage	$I_F = 800$ mA		1.0	1.6	V
I_R	Diode Leakage Current	$V_R = 70V$			100	µA
I_{CC}	Supply Current	All Inputs Low EN = 2.0V		50	65	mA
		All Inputs High		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L = 60\Omega$, $V_L = 30V$		226	500	ns
t_{LH}	Turn Off Delay	$R_L = 60\Omega$, $V_L = 30V$		2430	8000	ns

Note 1: "Absolute Maximium Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

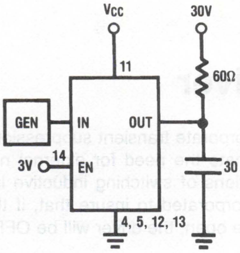
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @70°C @ the rate of 16.6 mW/°C.

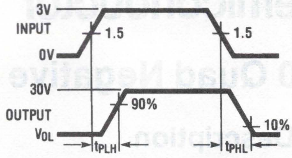
AC Test Circuit


VCC
30V
11
60Ω
GEN
IN
OUT
3V
14
EN
30 pF*
4, 5, 12, 13

TL/F/5820–2

*Includes probe and jig capacitance

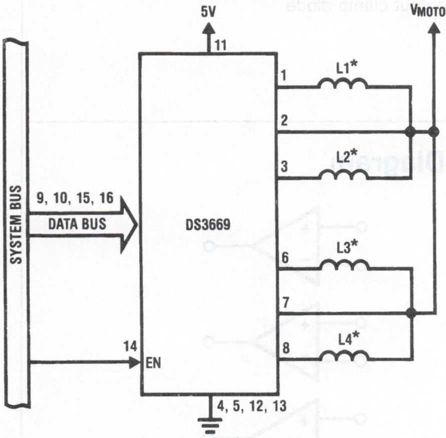
Switching Waveforms


3V
INPUT
0V
1.5
1.5
30V
OUTPUT
VOL
90%
10%
tPLH
tPHL

TL/F/5820–3

Typical Applications

Stepping Motor Driver

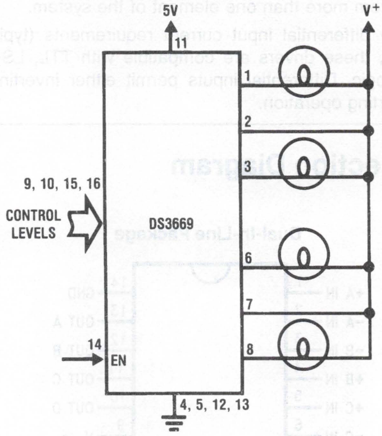

5V
VMOTOR**
11
SYSTEM BUS
9, 10, 15, 16
DATA BUS
DS3669
14
EN
4, 5, 12, 13
1
2
3
6
7
8
L1*
L2*
L3*
L4*

TL/F/5820–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Lamp Driver


5V
V+
11
9, 10, 15, 16
CONTROL LEVELS
DS3669
14
EN
4, 5, 12, 13
1
2
3
6
7
8

TL/F/5820–5

National Semiconductor

DS3680 Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range (±20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which pemits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

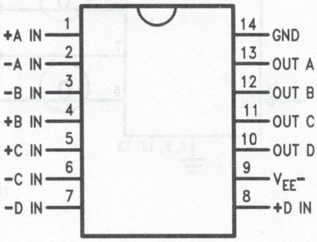
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to insure that, if the +IN input or both inputs are open, the driver will be OFF.

Features

- −10V to −60V operation
- Quad 50 mA sink capability
- TTL/LS/COMS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Connection Diagram

Dual-In-Line Package

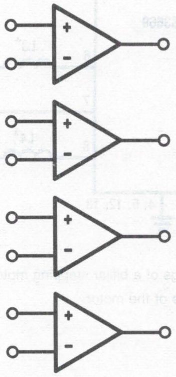


TL/F/5821-1

Top View

Order Number DS3680J, DS3680M or DS3680N
See NS Package Number J14A, M14A, N14A

Logic Diagram



TL/F/5821-2

Truth Table

Differential Inputs	Outputs
$V_{ID} \geq 2V$	On
$V_{ID} \leq 0.8V$	Off
Open	Off

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (GND to $V_{EE}-$, and Any Pin)	−70V
Positive Input Voltage (Input to GND)	20V
Negative Input Voltage (Input to $V_{EE}-$)	−5V
Differential Voltage (+IN to −IN)	±20V
Inductive Load	$L_L \leq 5h$
	$I_L \leq 50$ mA
Output Current	−100 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1398 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded dip package 11.2 mW/°C above 25°C; derate SO package 8.02 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (GND to $V_{EE}-$)	−10	−60	V
Input Voltage (Input to GND)	−20	20	V
Logic ON Voltage (+IN)			
Referenced to −IN	2	20	V
Logic OFF Voltage (+IN)			
Referenced to −IN	−20	0.8	V
Temperature Range	−25	+85	°C

Electrical Characteristics (Notes 2 and 3)

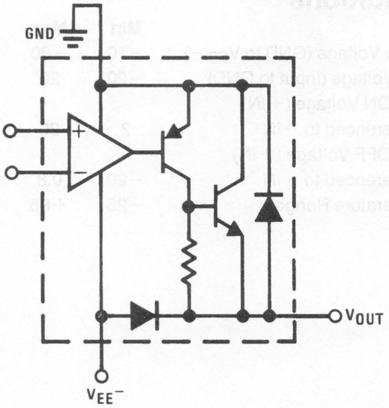
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage		2.0	1.3		V
V_{IL}	Logic "0" Input Voltage			1.3	0.8	V
I_{INH}	Logic "1" Input Current	V_{IN} = 2V V_{IN} = 7V		40 375	100 1000	μA μA
I_{INL}	Logic "0" Input Current	V_{IN} = 0.4V V_{IN} = −7V		−0.01 −1	−5 −100	μA μA
V_{OL}	Output ON Voltage	I_{OL} = 50 mA		−1.6	−2.1	V
I_{OFF}	Output Leakage	$V_{OUT} = V_{EE}-$		−2	−100	μA
I_{FS}	Fail-Safe Output Leakage	$V_{OUT} = V_{EE}-$ (Inputs Open)		−2	−100	μA
I_{LC}	Output Clamp Leakage Current	V_{OUT} = GND		2	100	μA
V_C	Output Clamp Voltage	I_{CLAMP} = −50 mA Referenced to $V_{EE}-$		−2	−1.2	V
V_P	Positive Output Clamp Voltage	I_{CLAMP} = 50 mA Referenced to GND		0.9	1.2	V
$I_{EE(ON)}$	ON Supply Current	All Drivers ON		−2	−4.4	mA
$I_{EE(OFF)}$	OFF Supply Current	All Drivers OFF		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver ON	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver OFF	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

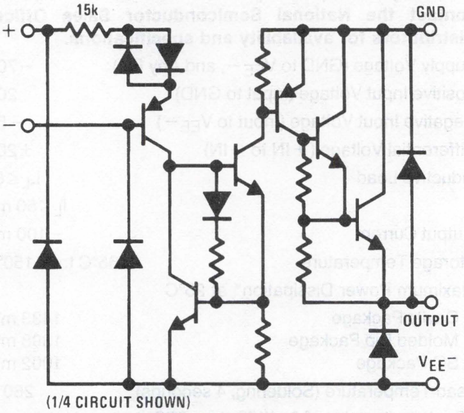
Note 2: Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the table of "Operating Conditions". All typical values are given for $V_{EE}-$ = 52V, and T_A = 25°C.

Note 3: All current into device pins shown as positive, out of the device as negative. All voltages are referenced to ground unless otherwise noted.

Schematic Diagrams


GND
+
−
V_OUT
V_EE⁻

TL/F/5821-3


15k
+
−
GND
OUTPUT
V_EE⁻

(1/4 CIRCUIT SHOWN)

TL/F/5821-4

National Semiconductor

DS3686 Dual Positive Voltage Relay Driver

General Description

The DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

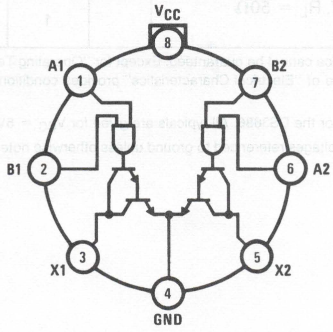
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

Metal Can Package



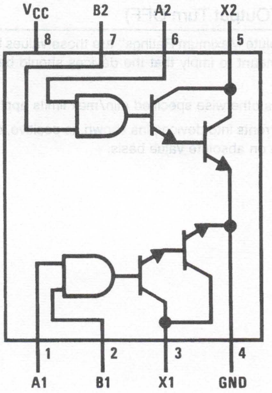
TL/F/5822–1

Top View

Pin 4 is in electrical contact with the case

Order Number DS3686H
See NS Package Number H08C

Dual-In-Line Package



TL/F/5822–2

Top View

Order Number DS3686J-8 or DS3686N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	±70	°C

Electrical Characteristics (Notes 2 and 3)

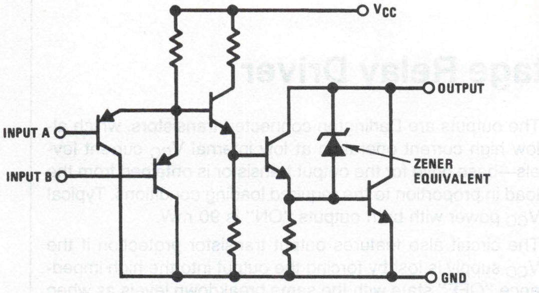
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 2.5V$	2.0			V
I_{IH}	Logical "1" Input Current	$V_{CC} = \text{Max}$, $V_{IN} = 5.5V$		0.01	40	μA
V_{IL}	Logical "0" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 53.8V$			0.8	V
I_{IL}	Logical "0" Input Current	$V_{CC} = \text{Max}$, $V_{IN} = 0.4V$		−150	−250	μA
V_{CD}	Input Clamp Voltage	$V_{CC} = 5V$, $I_{CLAMP} = -12$ mA, $T_A = 25°C$		−1.0	−1.5	V
V_{OH}	Output Breakdown	$V_{CC} = \text{Max}$, $V_{IN} = 0V$, $I_{OUT} = 5$ mA	56	65		V
I_{OH}	Output Leakage	$V_{CC} = \text{Max}$, $V_{IN} = 0.4V$, $V_{OUT} = 54V$		0.5	250	μA
V_{OL}	Output ON Voltage	$V_{CC} = \text{Min}$, $V_{IN} = 2.4V$; DS3686; $I_{OL} = 100$ mA		0.85	1.0	V
		$I_{OL} = 300$ mA		1.0	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	$V_{CC} = \text{Max}$, $V_{IN} = 0V$, Outputs Open		2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	$V_{CC} = \text{Max}$, $V_{IN} = 3V$, Outputs Open		18	28	mA
t_{PD0}	Propagation Delay to a Logical "0" (Output Turn ON)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$ $T_A = 25°C$, $V_{CC} = 5V$		50		ns
t_{PD1}	Propagation Delay to a Logical "1" (Output Turn OFF)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$ $T_A = 25°C$, $V_{CC} = 5V$		1		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3686. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagram


V_CC
OUTPUT
INPUT A
INPUT B
ZENER EQUIVALENT
GND

TL/F/5822-3

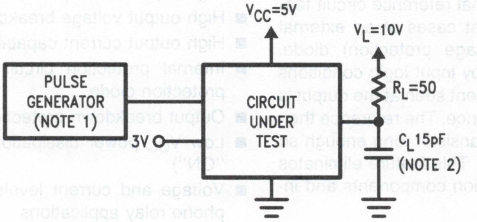
Truth Table

Positive logic: $\overline{AB} = X$

A	B	Output X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

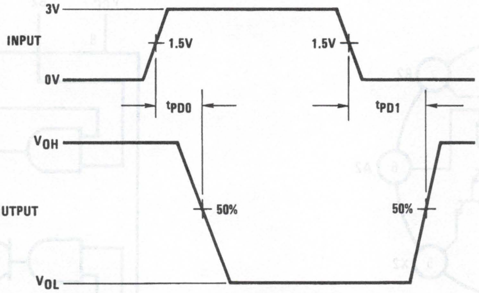
AC Test Circuit and Switching Time Waveforms


V_CC=5V
V_L=10V
R_L=50
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST
3V
C_L 15pF (NOTE 2)

TL/F/5822-4

Note 1: The pulse generator has the following characteristics: PRR = 100 kHz, 50% duty cycle, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.


3V
INPUT
0V
1.5V
1.5V
t_PD0
t_PD1
V_OH
OUTPUT
50%
50%
V_OL

TL/F/5822-5

National Semiconductor

DS1687/DS3687 Negative Voltage Relay Driver

General Description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

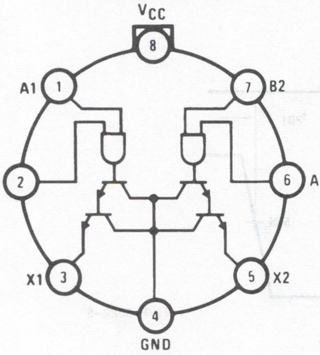
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

Metal Can Package



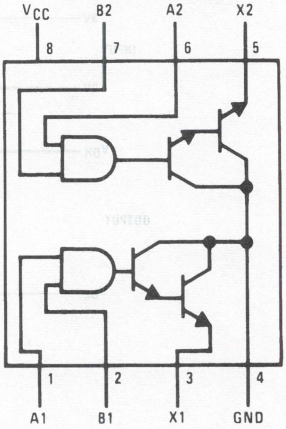
TL/F/5823-1

Top View

Pin 4 is in electrical contact with the case

Order Number DS1687H or DS3687H
See NS Package Number H08C

Dual-In-Line Package



TL/F/5823-2

Top View

Order Number DS1687J-8, DS3687J-8 or DS3687N
See NS Package Number J08A or N08E

Truth Table

Positive logic: $\overline{AB} = X$

A	B	Output X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

Electrical Characteristics (Note 2 and 3)

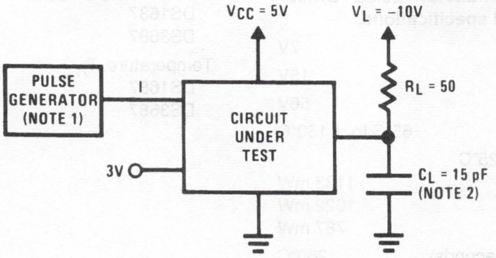
Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				1.0		μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−150	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−56	−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				−0.5	−250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, V_{IN} = 2V	DS1687	I_{OL} = −100 mA		−0.9	−1.1	V
				I_{OL} = −300 mA		−1.0	−1.3	V
			DS3687	I_{OL} = −100 mA		−0.9	−1.0	V
				I_{OL} = −300 mA		−1.0	−1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18	28	mA
$t_{PD(ON)}$	Propagation Delay to a Logical "0" (Output Turn ON)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				50		ns
$t_{PD(OFF)}$	Propagation Delay to a Logical "1" (Output Turn OFF)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				1.0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperture range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

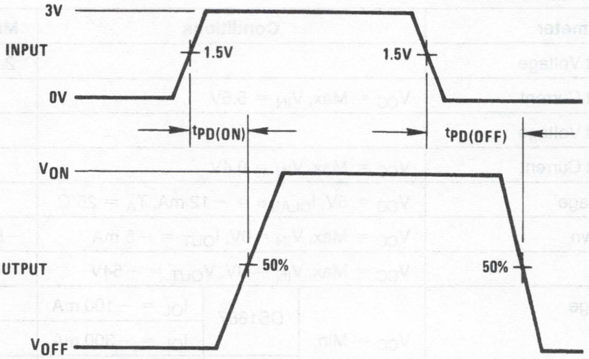
AC Test Circuit and Switching Time Waveforms


V_{CC} = 5V
V_L = −10V
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST
3V
R_L = 50
C_L = 15 pF (NOTE 2)

TL/F/5823-4

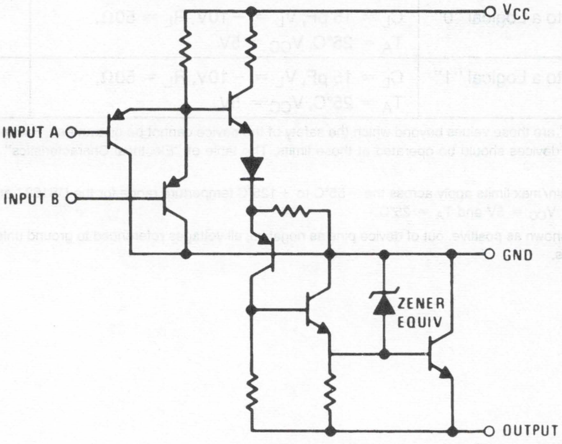
Note 1: The pulse generator has the following characteristics: PRR = MHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \le 10$ ns.

Note 2: C_L includes probe and jig capacitance.


3V
INPUT
1.5V
1.5V
0V
$t_{PD(ON)}$
$t_{PD(OFF)}$
V_{ON}
OUTPUT
50%
50%
V_{OFF}

TL/F/5823-5

Schematic Diagram


V_{CC}
INPUT A
INPUT B
GND
ZENER EQUIV
OUTPUT

TL/F/5823-3

National Semiconductor

DS55451/2/3/4, DS75450/1/2/3/4 Series Dual Peripheral Drivers

General Description

The DS75450 series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

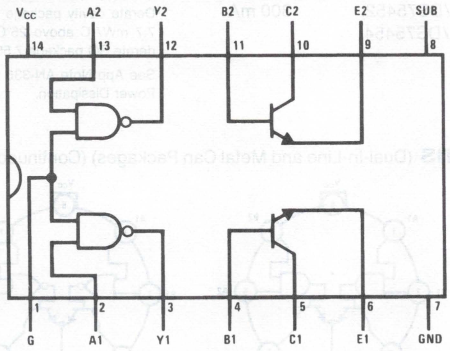
The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)

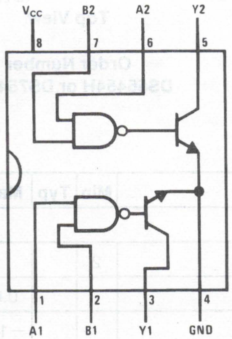


TL/F/5824-1

Top View

Order Number DS75450J or DS75450N

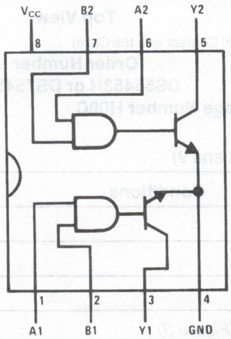
See NS Package Number J14A or N14A



TL/F/5824-2

Top View

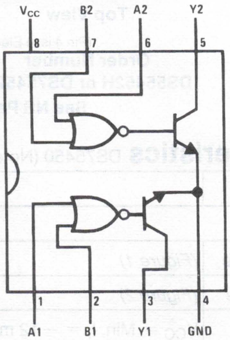
Order Number DS55451J-8, DS75451J-8, DS75451M or DS75451N



TL/F/5824-3

Top View

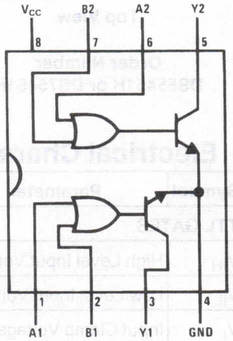
Order Number DS55452J-8, DS75452J-8, DS75452M or DS75452N



TL/F/5824-4

Top View

Order Number DS55453J-8, DS75453J-8, DS75453M or DS75453N



TL/F/5824-5

Top View

Order Number DS55454J-8, DS75454J-8 or DS75454N

See NS Package Numbers J08A, M08A* or N08E

*See Note 6 and AN-336 regarding S.O. package power dissipation constraints.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS75450	35V
Collector-to-Substrate Voltage	
DS75450	35V
Collector-Base Voltage	
DS75450	35V
Collector-Emitter Voltage (Note 4)	
DS75450	30V
Emitter-Base Voltage	
DS75450	5.0V
Output Voltage (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6)	
DS75450	300 mA
Output Current (Note 6)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75450 Maximum Power (Note 6)	
Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
DS75451/2/3/4 Maximum Power (Note 6)	
Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions (Note 7)

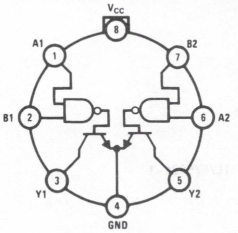
	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

†Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

See App Note AN-336 for further information on Understanding Package Power Dissipation.

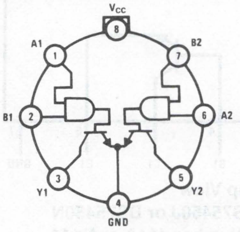
Connection Diagrams (Dual-In-Line and Metal Can Packages) (Continued)



TL/F/5824-6

Top View

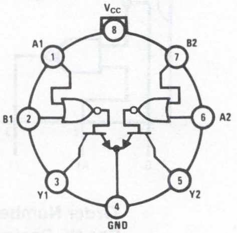
Order Number DS55451H or DS75451H



TL/F/5824-7

Top View

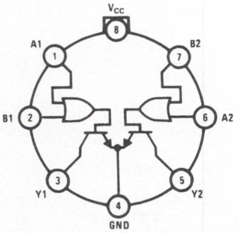
Order Number DS55452H or DS75452H



TL/F/5824-8

Top View

Order Number DS55453H or DS75453H



TL/F/5824-9

Top View

Order Number DS55454H or DS75454H

(Pin 4 is in Electrical Contact with the Case)

See NS Package Number H08C

Electrical Characteristics DS75450 (Notes 8 and 9)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TTL GATES							
V_{IH}	High Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400 µA, *(Figure 2)*		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*			0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A			1	mA
			Input G			2	mA

Electrical Characteristics DS75450 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
TTL GATES (Continued)								
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*		Input A			40	µA
				Input G			80	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*		Input A			−1.6	mA
				Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)			−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				6	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 µA, I_E = 0 µA			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 µA, R_{BE} = 500Ω			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 µA, I_C = 0 µA			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	T_A = +25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			T_A = 0°C	I_C = 100 mA	20			
				I_C = 300 mA	25			
V_{BE}	Base-Emitter Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	µA
					DS75451, DS75453			100	µA
				V_{IL} = 0.8V	DS55452, DS55454			300	µA
					DS75452, DS75454			100	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V	DS55451/DS75451		7	11	mA
			V_I = 0V	DS55452/DS75452		11	14	mA
			V_I = 5V	DS55453/DS75453		8	11	mA
			V_I = 0V	DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V	DS55451/DS75451		52	65	mA
			V_I = 5V	DS55452/DS75452		56	71	mA
			V_I = 0V	DS55453/DS75453		54	68	mA
			V_I = 5V	DS55454/DS75454		61	79	mA

Switching Characteristics DS75450 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, I_C ≈ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S − 6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time				12	20	ns
t_S	Storage Time				7	15	ns
t_F	Full Time				6	15	ns

Switching Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, I_O ≈ 300 mA, *(Figure 15)*		V_S − 6.5			mV

Switching Characteristics (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle < 2%.

Note 12: Applies to output transistors only.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55452/DS75452

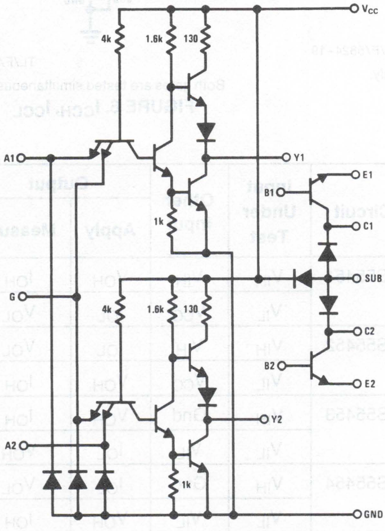
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55454/DS75454

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

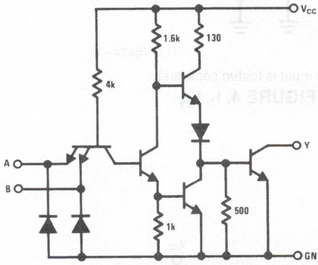
Schematic Diagrams

DS75450



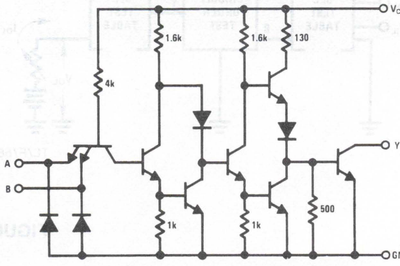
Resistor values shown are nominal. TL/F/5824-10

DS55451/DS75451



Resistor values shown are nominal. TL/F/5824-11

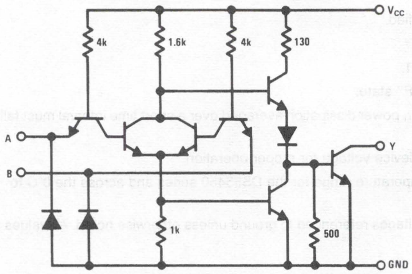
DS55452/DS75452



Resistor values shown are nominal. TL/F/5824-12

Schematic Diagrams (Continued)

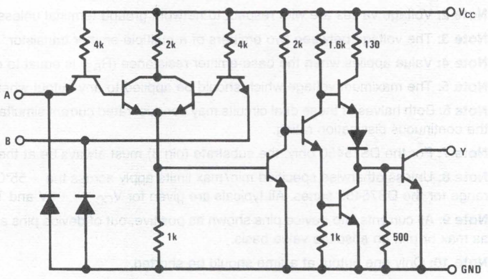
DS55453/DS75453


V_{CC}
4k
1.6k
4k
130
A
B
Y
1k
500
GND

Resistor values shown are nominal.

TL/F/5824-13

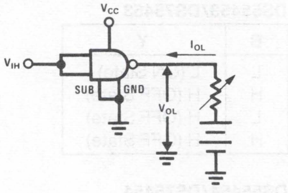
DS55454/DS75454


V_{CC}
4k
2k
4k
2k
1.6k
130
A
B
Y
1k
1k
500
GND

Resistor values shown are nominal.

TL/F/5824-14

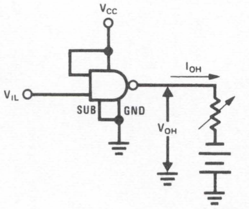
DC Test Circuits


V_{CC}
V_{IH}
I_{OL}
SUB
GND
V_{OL}

TL/F/5824-15

Both inputs are tested simultaneously.

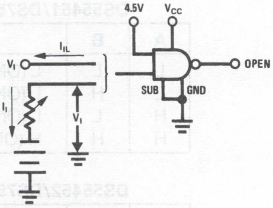
FIGURE 1. V_{IH}, V_{OL}


V_{CC}
V_{IL}
I_{OH}
SUB
GND
V_{OH}

TL/F/5824-16

Each input is tested separately.

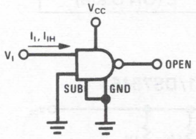
FIGURE 2. V_{IL}, V_{OH}


4.5V
V_{CC}
I_{IL}
V_I
OPEN
I_I
V_I
SUB
GND

TL/F/5824-17

Each input is tested separately.

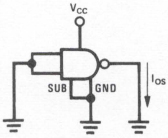
FIGURE 3. V_I, I_{IL}


V_{CC}
I_I, I_{IH}
V_I
OPEN
SUB
GND

TL/F/5824-18

Each input is tested separately.

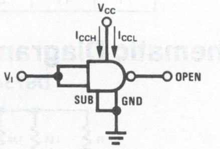
FIGURE 4. I_I, I_{IH}


V_{CC}
SUB
GND
I_{OS}

TL/F/5824-19

Each input is tested separately.

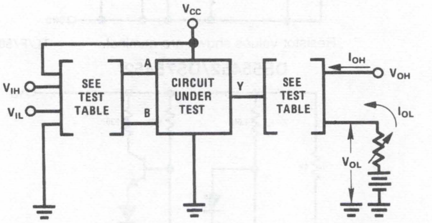
FIGURE 5. I_{OS}


V_{CC}
I_{CCH}
I_{CCL}
V_I
OPEN
SUB
GND

TL/F/5824-20

Both gates are tested simultaneously.

FIGURE 6. I_{CCH}, I_{CCL}

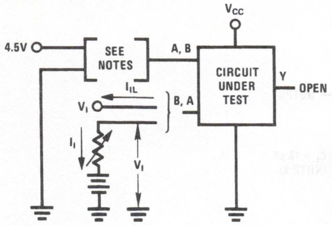

V_{CC}
V_{IH}
V_{IL}
SEE TEST TABLE
A
B
CIRCUIT UNDER TEST
Y
SEE TEST TABLE
I_{OH}
V_{OH}
I_{OL}
V_{OL}

TL/F/5824-21

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

DC Test Circuits (Continued)

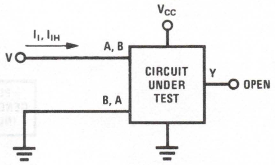

VCC
4.5V
SEE NOTES
A, B
CIRCUIT UNDER TEST
Y
OPEN
IIL
VI
B, A
II
VI

Note A: Each input is tested separately.

Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded. For all other circuits it is at 4.5V.

TL/F/5824–22

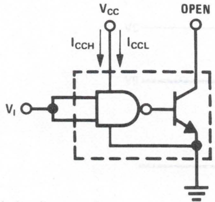
FIGURE 8. V_I, V_{IL}


VCC
II, IIH
V
A, B
CIRCUIT UNDER TEST
Y
OPEN
B, A

Each input is tested separately.

TL/F/5824–23

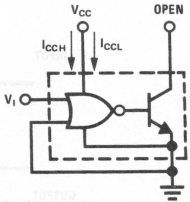
FIGURE 9. I_I, I_{IH}


VCC
OPEN
ICCH
ICCL
VI

Both gates are tested simultaneously.

TL/F/5824–24

FIGURE 10. I_{CCH}, I_{CCL} **for AND, NAND Circuits**

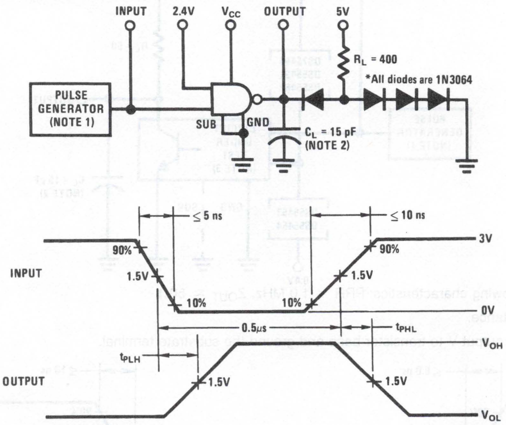

VCC
OPEN
ICCH
ICCL
VI

Both gates are tested simultaneously.

TL/F/5824–25

FIGURE 11. I_{CCH}, I_{CCL} **for OR, NOR Circuits**

AC Test Circuits and Switching Time Waveforms


INPUT
2.4V
VCC
OUTPUT
5V
RL = 400
*All diodes are 1N3064
PULSE GENERATOR (NOTE 1)
SUB
GND
CL = 15 pF (NOTE 2)
≤ 5 ns
≤ 10 ns
3V
90%
90%
INPUT
1.5V
1.5V
10%
10%
0V
0.5μs
tPHL
VOH
tPLH
OUTPUT
1.5V
1.5V
VOL

TL/F/5824–26

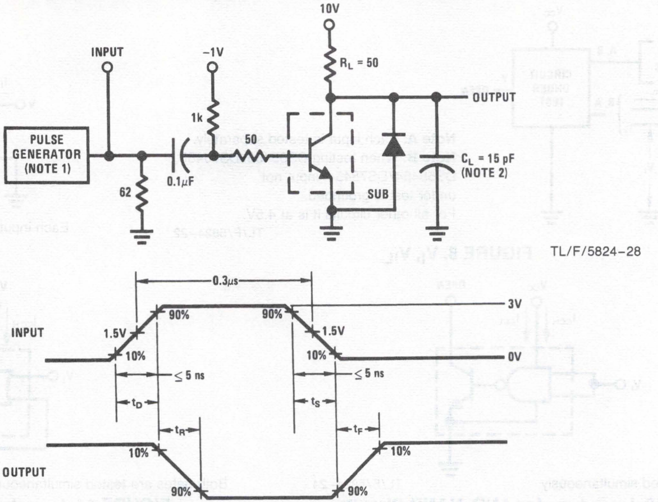
TL/F/5824–27

Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)

AC Test Circuits and Switching Time Waveforms (Continued)


10V
INPUT
−1V
R_L = 50
OUTPUT
1k
PULSE GENERATOR (NOTE 1)
50
0.1μF
62
C_L = 15 pF (NOTE 2)
SUB
0.3μs
INPUT
90%
1.5V
10%
3V
0V
≤ 5 ns
t_D
t_S
t_R
t_F
OUTPUT
10%
90%

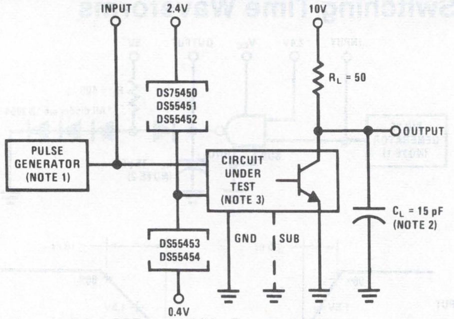
TL/F/5824-28

TL/F/5824-29

Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS75450 Only)

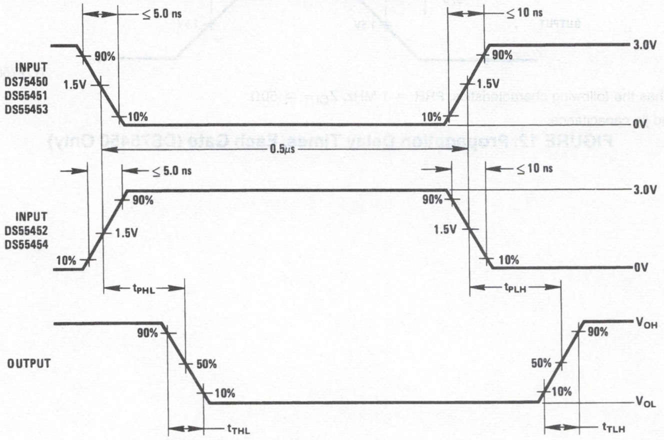

INPUT
2.4V
10V
DS75450
DS55451
DS55452
R_L = 50
OUTPUT
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST (NOTE 3)
C_L = 15 pF (NOTE 2)
GND
SUB
DS55453
DS55454
0.4V

Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

TL/F/5824-30

Note 2: C_L includes probe and jig capacitance.

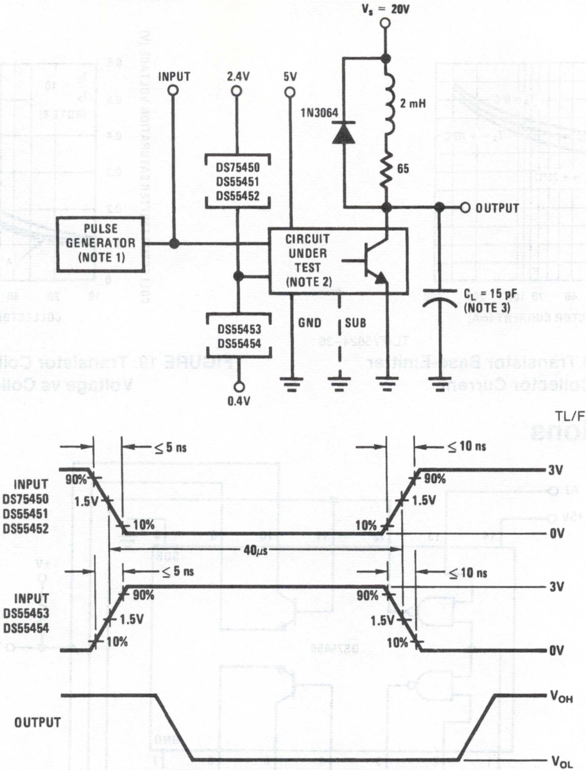
Note 3: When testing DS75450, connect output V to transistor base and ground the substrate terminal.


≤ 5.0 ns
≤ 10 ns
INPUT DS75450 DS55451 DS55453
90%
1.5V
10%
3.0V
0V
0.5μs
INPUT DS55452 DS55454
t_PHL
t_PLH
OUTPUT
50%
V_OH
V_OL
t_THL
t_TLH

TL/F/5824-31

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)


V_s = 20V
INPUT
2.4V
5V
1N3064
2 mH
65
DS75450
DS55451
DS55452
OUTPUT
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST (NOTE 2)
C_L = 15 pF (NOTE 3)
GND
SUB
DS55453
DS55454
0.4V
≤ 5 ns
≤ 10 ns
INPUT
DS75450
DS55451
DS55452
90%
1.5V
10%
40μs
3V
0V
INPUT
DS55453
DS55454
OUTPUT
V_OH
V_OL

TL/F/5824-32

TL/F/5824-33

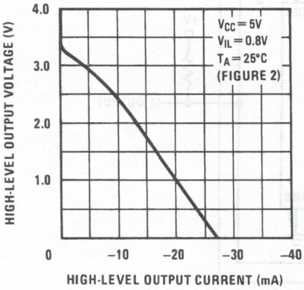
Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: When testing DS75450, connect output V to transistor base with a 600Ω resistor from there to ground and ground the substrate terminal.

Note 3: C_L includes probe and jig capacitance.

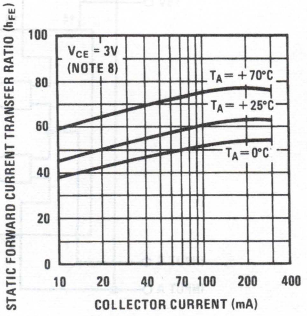
FIGURE 15. Latch-UP Test of Complete Drivers

Typical Performance Characteristics



TL/F/5824-34

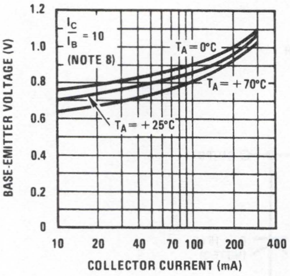
FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current



TL/F/5824-35

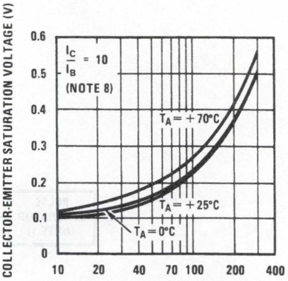
FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)



TL/F/5824–36

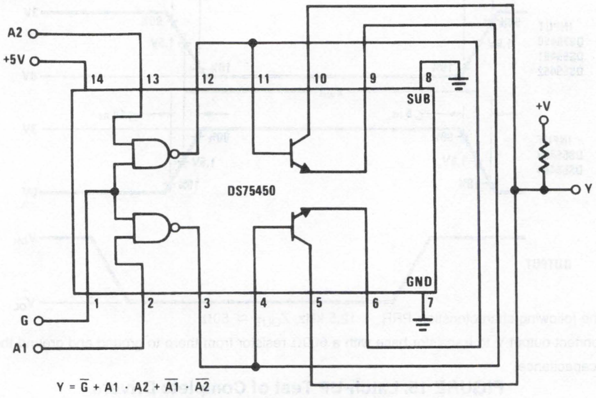
FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current



TL/F/5824–37

FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

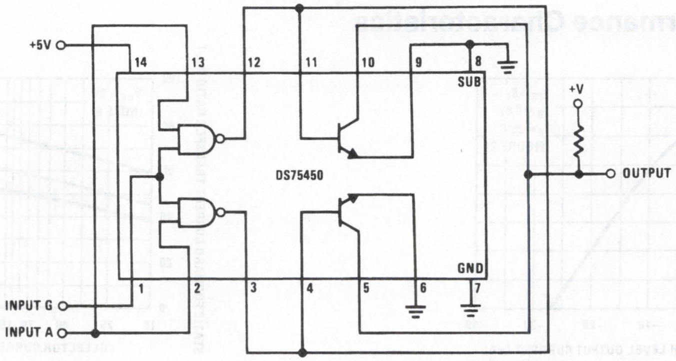
Typical Applications


A2
+5V
14
13
12
11
10
9
8
SUB
+V
Y
DS75450
GND
1
2
3
4
5
6
7
G
A1

$Y = \overline{G} + A1 \cdot A2 + \overline{A1} \cdot \overline{A2}$

TL/F/5824–38

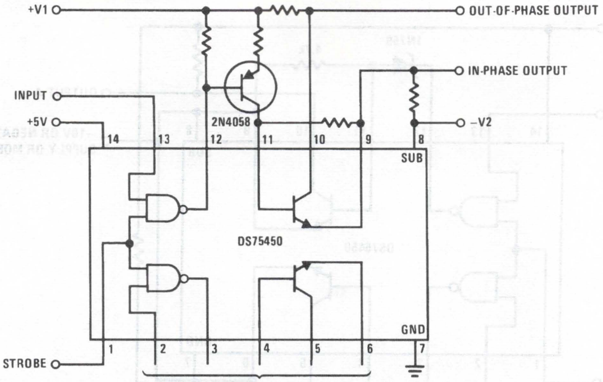
FIGURE 20. Gated Comparator


+5V
14
13
12
11
10
9
8
SUB
+V
OUTPUT
DS75450
GND
1
2
3
4
5
6
7
INPUT G
INPUT A

TL/F/5824–39

FIGURE 21. 500 mA Sink

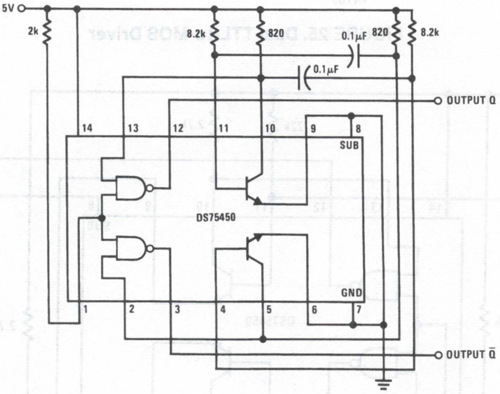
Typical Applications (Continued)


+V1
OUT-OF-PHASE OUTPUT
IN-PHASE OUTPUT
INPUT
+5V
−V2
2N4058
14
13
12
11
10
9
8
SUB
DS75450
GND
STROBE
1
2
3
4
5
6
7

This side can perform the same or another function.

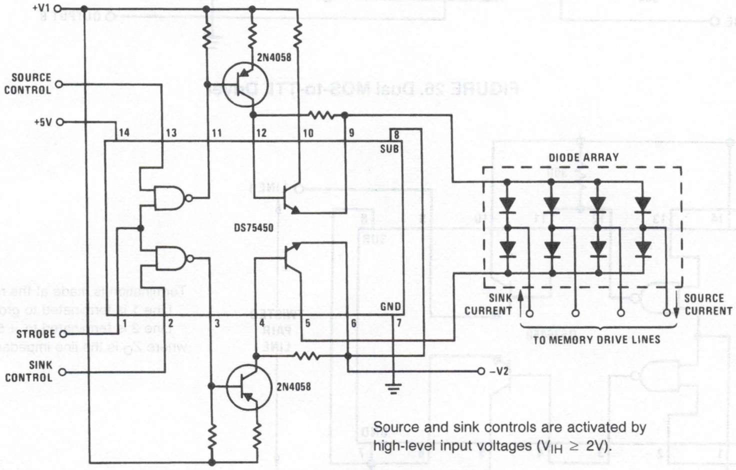
TL/F/5824-40

FIGURE 22. Floating Switch


5V
2k
8.2k
820
0.1 μF
820
8.2k
0.1 μF
OUTPUT Q
14
13
12
11
10
9
8
SUB
DS75450
GND
1
2
3
4
5
6
7
OUTPUT Q̄

TL/F/5824-41

FIGURE 23. Square-Wave Generator

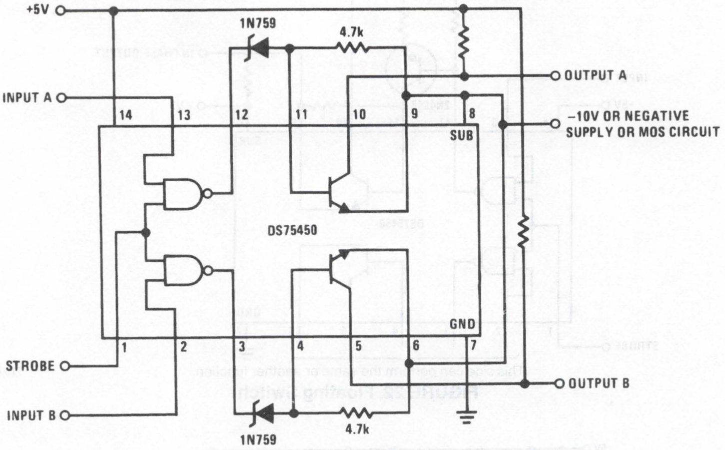

+V1
2N4058
SOURCE CONTROL
+5V
14
13
11
12
10
9
8
SUB
DIODE ARRAY
DS75450
GND
STROBE
1
2
3
4
5
6
7
SINK CONTROL
−V2
2N4058
SINK CURRENT
SOURCE CURRENT
TO MEMORY DRIVE LINES

Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

TL/F/5824-42

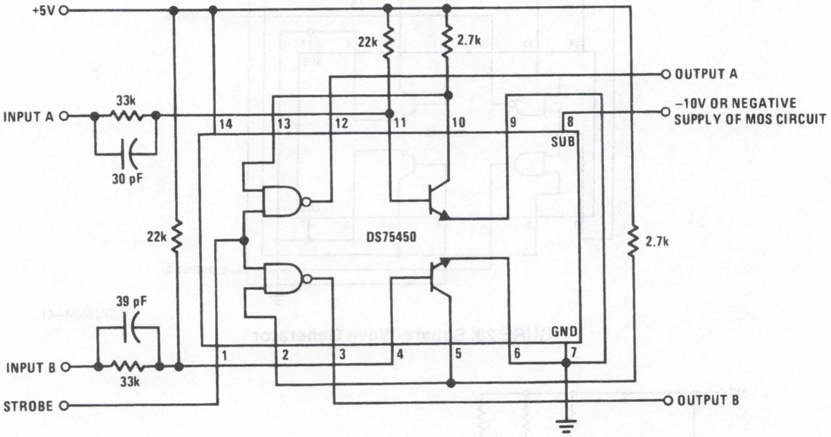
FIGURE 24. Core Memory Driver

Typical Applications (Continued)


+5V
INPUT A
STROBE
INPUT B
1N759
4.7k
1N759
4.7k
14
13
12
11
10
9
8
SUB
DS75450
GND
1
2
3
4
5
6
7
OUTPUT A
−10V OR NEGATIVE SUPPLY OR MOS CIRCUIT
OUTPUT B

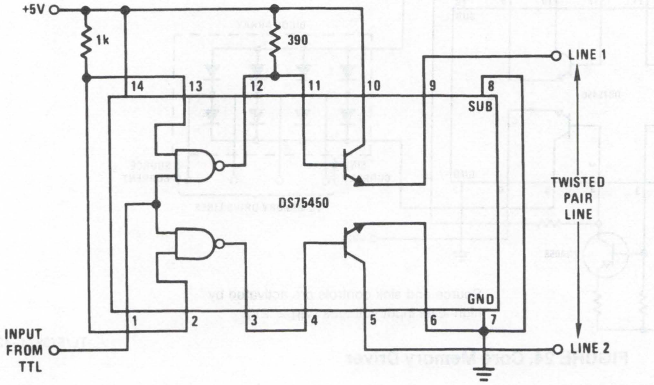
TL/F/5824-43

FIGURE 25. Dual TTL-to-MOS Driver


+5V
INPUT A
33k
30 pF
22k
39 pF
INPUT B
33k
STROBE
22k
2.7k
14
13
12
11
10
9
8
SUB
DS75450
GND
1
2
3
4
5
6
7
2.7k
OUTPUT A
−10V OR NEGATIVE SUPPLY OF MOS CIRCUIT
OUTPUT B

TL/F/5824-44

FIGURE 26. Dual MOS-to-TTL Driver

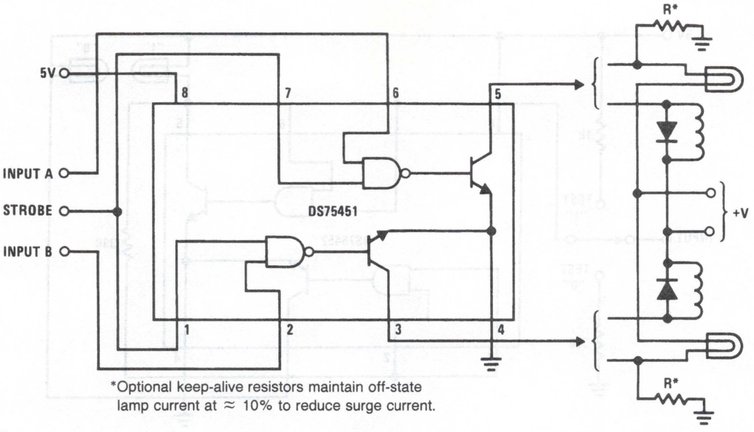

+5V
1k
390
14
13
12
11
10
9
8
SUB
DS75450
GND
1
2
3
4
5
6
7
INPUT FROM TTL
LINE 1
TWISTED PAIR LINE
LINE 2

Termination is made at the receiving end as follows:
Line 1 is terminated to ground through Z_O/Z;
Line 2 is terminated to +5V through Z_O/Z;
where Z_O is the line impedance.

TL/F/5824-45

FIGURE 27. Balanced Line Driver

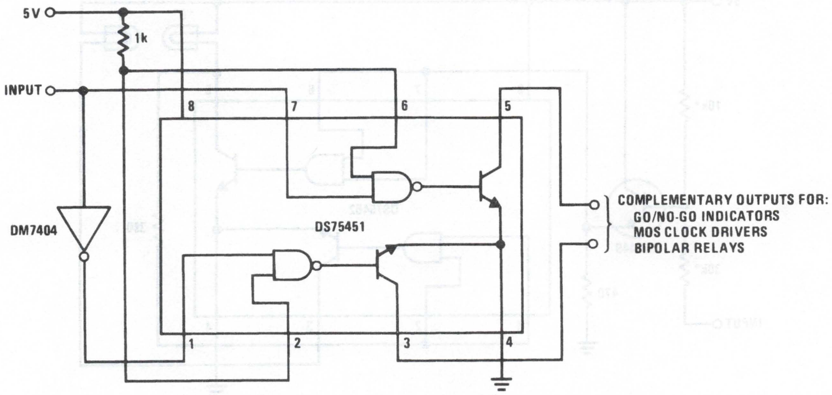
Typical Applications (Continued)


R*
5V
8
7
6
5
INPUT A
STROBE
INPUT B
DS75451
1
2
3
4
+V
R*

*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

TL/F/5824-46

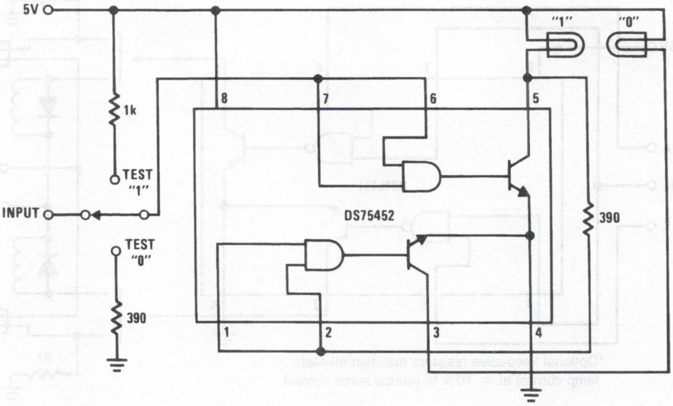
FIGURE 28. Dual Lamp or Relay Driver


5V
1k
INPUT
8
7
6
5
DM7404
DS75451
1
2
3
4
COMPLEMENTARY OUTPUTS FOR:
GO/NO-GO INDICATORS
MOS CLOCK DRIVERS
BIPOLAR RELAYS

TL/F/5824-47

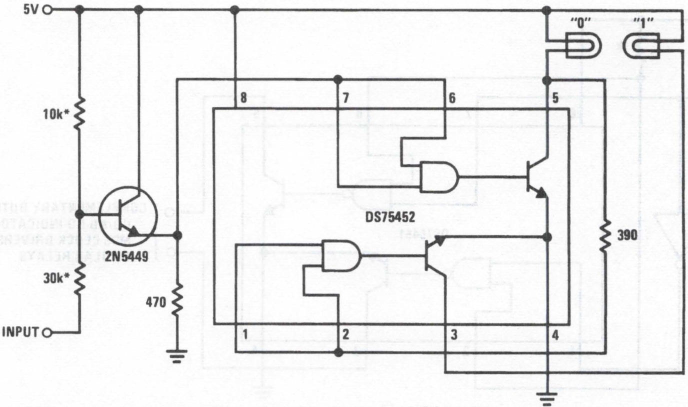
FIGURE 29. Complementary Driver

Typical Applications (Continued)


5V
1k
TEST
"1"
INPUT
TEST
"0"
390
8
7
6
5
"1"
"0"
DS75452
390
1
2
3
4

TL/F/5824-48

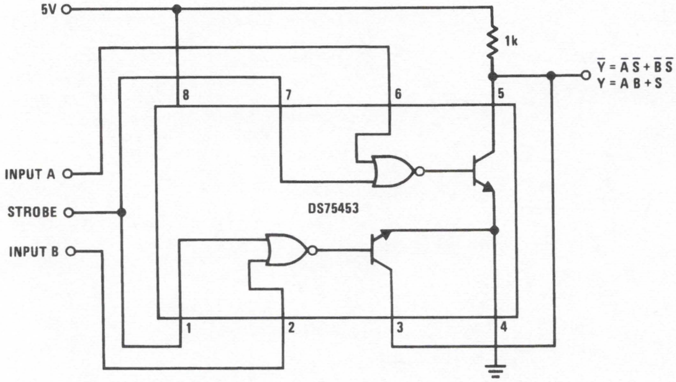
FIGURE 30. TTL or DTL Positive Logic-Level Detector


5V
10k*
2N5449
30k*
470
INPUT
8
7
6
5
"0"
"1"
DS75452
390
1
2
3
4

*The two input resistors must be adjusted for the level of MOS input.

TL/F/5824-49

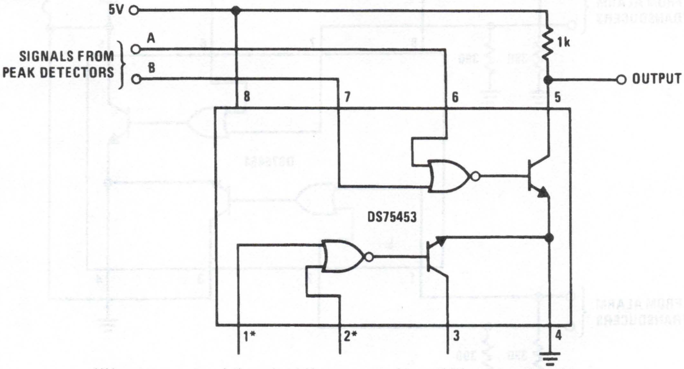
FIGURE 31. MOS Negative Logic-Level Detector


5V
1k
$\overline{Y} = \overline{A}\,\overline{S} + \overline{B}\,\overline{S}$
$Y = AB + S$
8
7
6
5
INPUT A
STROBE
INPUT B
DS75453
1
2
3
4

TL/F/5824-50

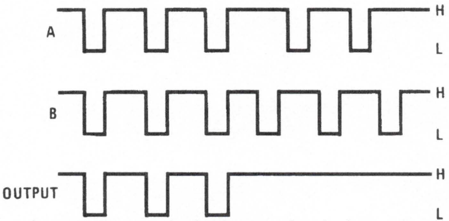
FIGURE 32. Logic Signal Comparator

Typical Applications (Continued)


5V
SIGNALS FROM PEAK DETECTORS
A
B
1k
OUTPUT
8
7
6
5
DS75453
1*
2*
3
4

*If inputs are unused, they should be connected to +5V through a 1k resistor.

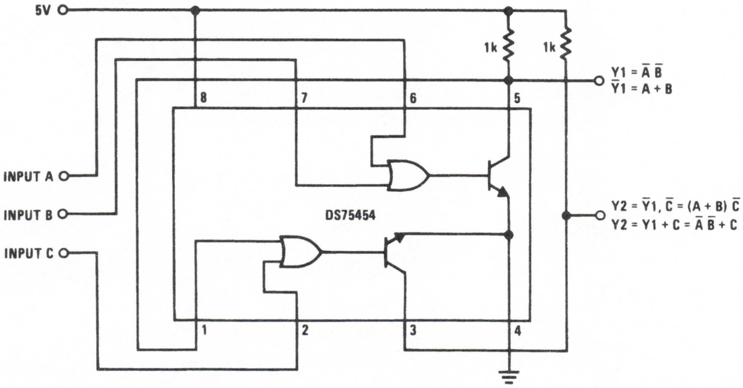
TL/F/5824-51



Low output occurs only when inputs are low simultaneously.

TL/F/5824-52

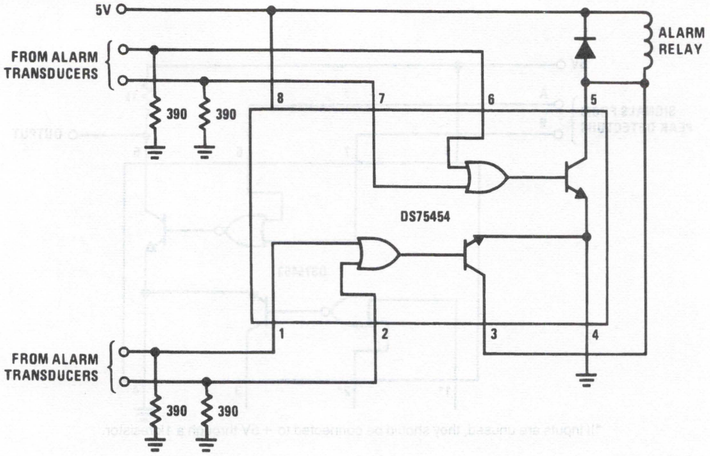
FIGURE 33. In-Phase Detector


5V
1k
1k
$Y1 = \overline{A}\,\overline{B}$
$\overline{Y1} = A + B$
8
7
6
5
INPUT A
INPUT B
INPUT C
DS75454
$Y2 = \overline{Y1}, \overline{C} = (A + B)\,\overline{C}$
$\overline{Y2} = Y1 + C = \overline{A}\,\overline{B} + C$
1
2
3
4

TL/F/5824-53

FIGURE 34. Multifunction Logic-Signal Comparator

Typical Applications (Continued)


5V
FROM ALARM TRANSDUCERS
390
390
8
7
6
5
ALARM RELAY
DS75454
1
2
3
4
FROM ALARM TRANSDUCERS
390
390

TL/F/5824-54

FIGURE 35. Alarm Detector

National Semiconductor

DS55461/2/3/4, DS75461/2/3/4 Series Dual Peripheral Drivers

General Description

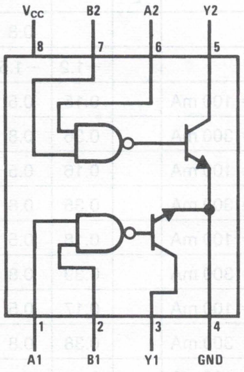
The DS55461/2/3/4 series of dual peripheral drivers are functionally interchangeable with DS55451/2/3/4 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages

Connection Diagrams (Dual-In-Line and Metal Can Packages)

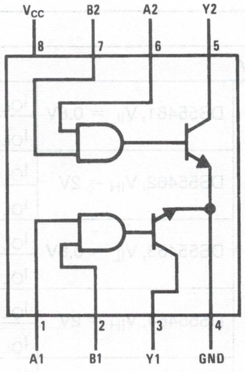


VCC
B2
A2
Y2
8
7
6
5
1
2
3
4
A1
B1
Y1
GND

TL/F/5825-1

Top View

Order Number DS55461J-8, DS75461J-8 or DS75461N

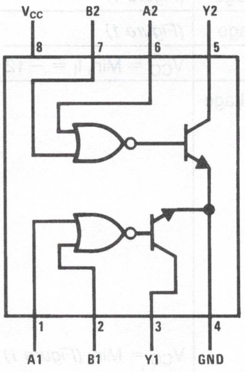


VCC
B2
A2
Y2
8
7
6
5
1
2
3
4
A1
B1
Y1
GND

TL/F/5825-2

Top View

Order Number DS55462J-8, DS75462J-8 or DS75462N

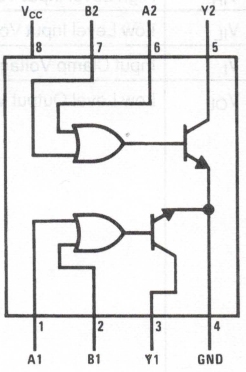


VCC
B2
A2
Y2
8
7
6
5
1
2
3
4
A1
B1
Y1
GND

TL/F/5825-3

Top View

Order Number DS55463J-8, DS75463J-8 or DS75463N



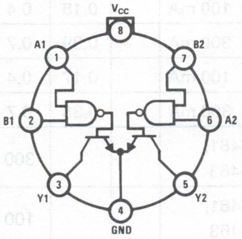
VCC
B2
A2
Y2
8
7
6
5
1
2
3
4
A1
B1
Y1
GND

TL/F/5825-4

Top View

Order Number DS55464J-8, DS75464J-8 or DS75464N

See NS Package Numbers J08A or N08E



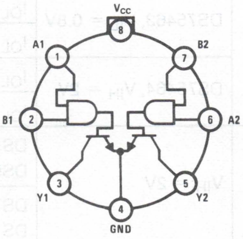
VCC
8
A1
1
B2
7
B1
2
6
A2
3
Y1
5
Y2
4
GND

TL/F/5825-5

Top View

Pin 4 is in electrical contact with the case.

Order Number DS55461H or DS75461H



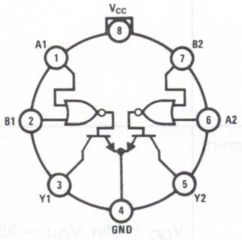
VCC
8
A1
1
B2
7
B1
2
6
A2
3
Y1
5
Y2
4
GND

TL/F/5825-6

Top View

Pin 4 is in electrical contact with the case.

Order Number DS55462H or DS75462H



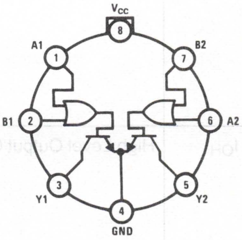
VCC
8
A1
1
B2
7
B1
2
6
A2
3
Y1
5
Y2
4
GND

TL/F/5825-7

Top View

Pin 4 is in electrical contact with the case.

Order Number DS55463H or DS75463H



VCC
8
A1
1
B2
7
B1
2
6
A2
3
Y1
5
Y2
4
GND

TL/F/5825-8

Top View

Pin 4 is in electrical contact with the case.

Order Number DS55464H or DS75464H

See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Output Current (Note 5)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1090 mW
Molded Package	957 mW
TO-5 Package	760 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 1)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 1)*	V_{IH} = 2V	DS55461, DS55463			300	µA
				DS75461, DS75463			100	µA
			V_{IL} = 0.8V	DS55462, DS55464			300	µA
				DS75462, DS75464			100	µA

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 3)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 3)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 2)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figures 4* and *5)*	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figures 4* and *5)*	V_I = 0V	DS55461/ DS75461		61	76	mA
				S55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time High-To-Low Level Output	$I_o \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 $V_{CC} = 5V$, $T_A = 25°C$ (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-To-High Level Output	$I_o \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_o = \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	$V_S = 30V$, $I_o \approx 300$ mA, *(Figure 7)*		$V_S - 10$			mV

Note 1: "Absoulte Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This is the maximum voltage which shoud be applied to any output when it is in the "OFF" state.

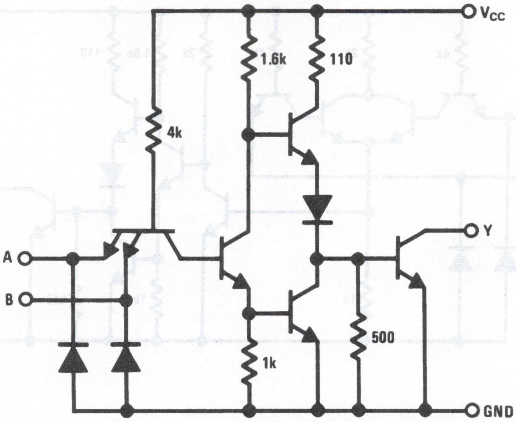
Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS44XXX series and across the 0°C to +70°C range for the DS75XXX series. All typicals are given for $V_{CC} = +5V$ and $T_A = 25°C$.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless othewise noted. All values shown as max or min on absolute value basis.

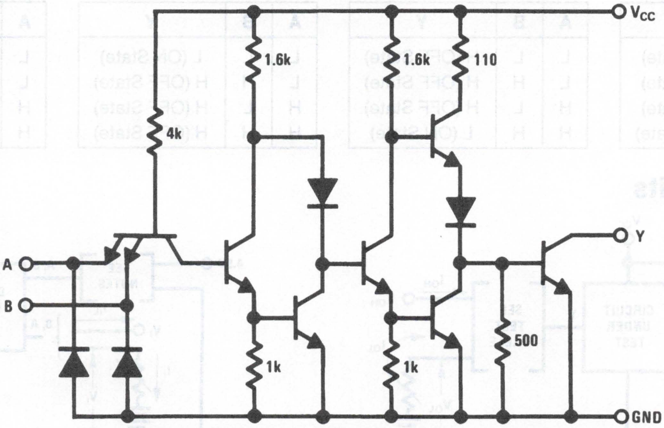
Schematic Diagrams

DS55461/DS75461


VCC
1.6k
110
4k
Y
A
B
500
1k
GND

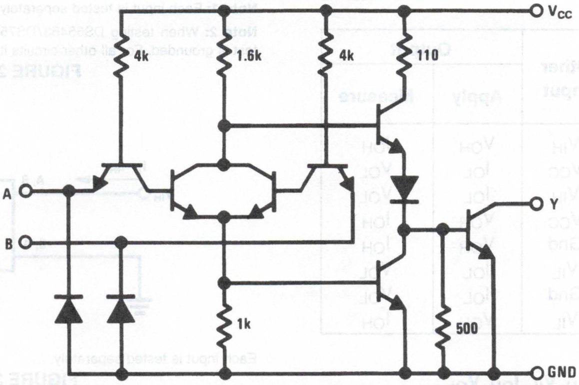
TL/F/5825-9

DS55462/DS75462


VCC
1.6k
1.6k
110
4k
Y
A
B
500
1k
1k
GND

TL/F/5825-10

DS55463/DS75463

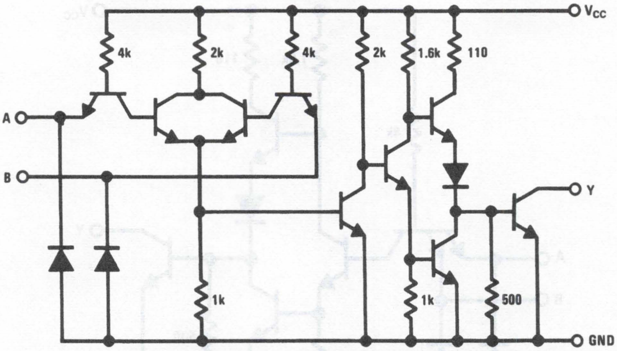

VCC
4k
1.6k
4k
110
A
Y
B
1k
500
GND

TL/F/5825-11

Resistor values shown are nominal.

Schematic Diagrams (Continued)

DS55464/DS75464



VCC
4k
2k
4k
2k
1.6k
110
A
B
Y
1k
1k
500
GND

TL/F/5825-12

Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

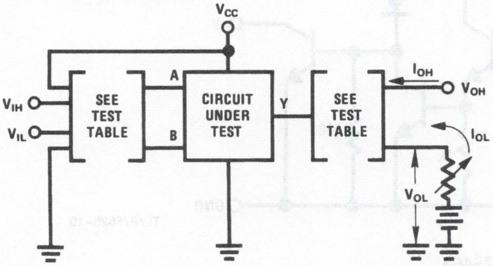
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits



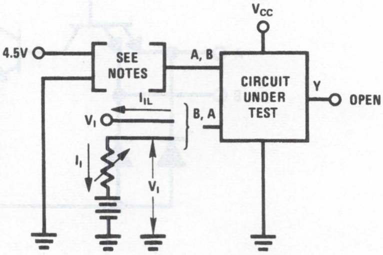
VCC
VIH
VIL
SEE TEST TABLE
A
B
CIRCUIT UNDER TEST
Y
SEE TEST TABLE
IOH
VOH
IOL
VOL

TL/F/5825-13

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55461	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55462	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55463	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS55464	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, I_{OH}, V_{OL}



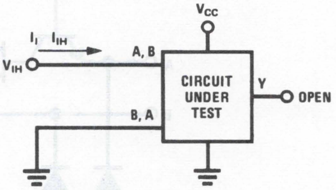
VCC
4.5V
SEE NOTES
A, B
IIL
VI
B, A
CIRCUIT UNDER TEST
Y
OPEN
II
VI

TL/F/5825-14

Note 1: Each input is tested separately.

Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 2. V_I, I_{IL}



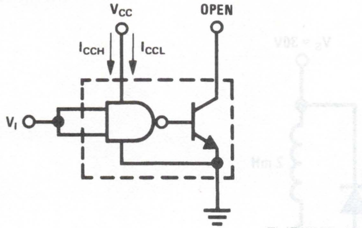
VCC
II IIH
VIH
A, B
B, A
CIRCUIT UNDER TEST
Y
OPEN

TL/F/5825-15

Each input is tested separately.

FIGURE 3. I_I, I_{IH}

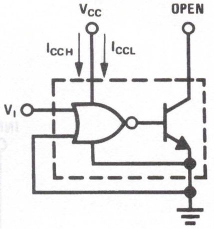
DC Test Circuits (Continued)


V_{CC}
OPEN
I_{CCH}
I_{CCL}
V_I

TL/F/5825–16

Both gates are tested simultaneously.

FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits

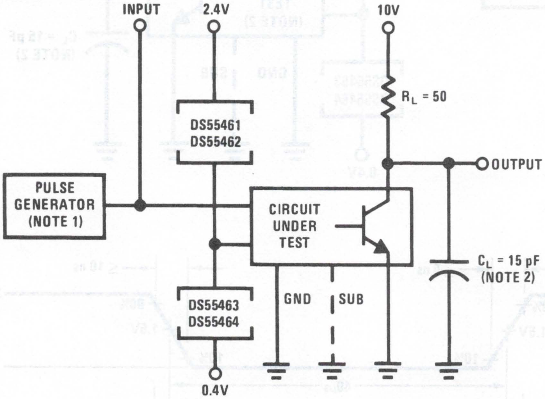

V_{CC}
OPEN
I_{CCH}
I_{CCL}
V_I

TL/F/5825–17

Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

Switching Characteristics

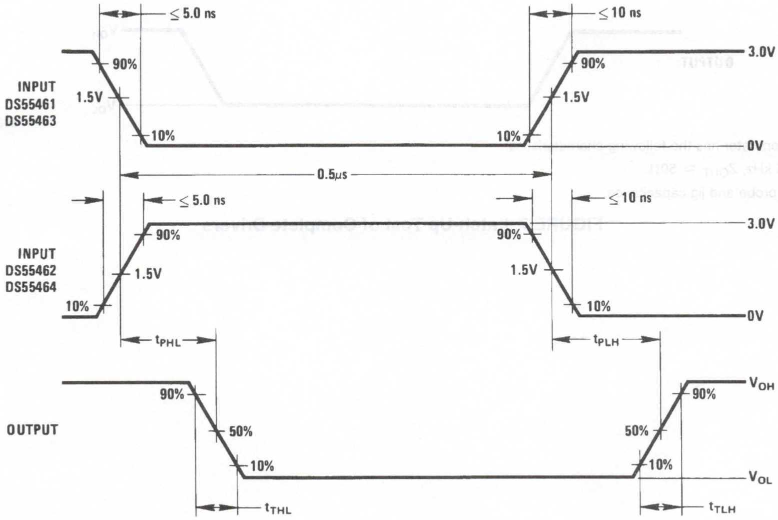

INPUT
2.4V
10V
R_L = 50
DS55461
DS55462
OUTPUT
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST
C_L = 15 pF (NOTE 2)
DS55463
DS55464
GND
SUB
0.4V

TL/F/5825–18

Note 1: The pulse generator has the following characteristics:

PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

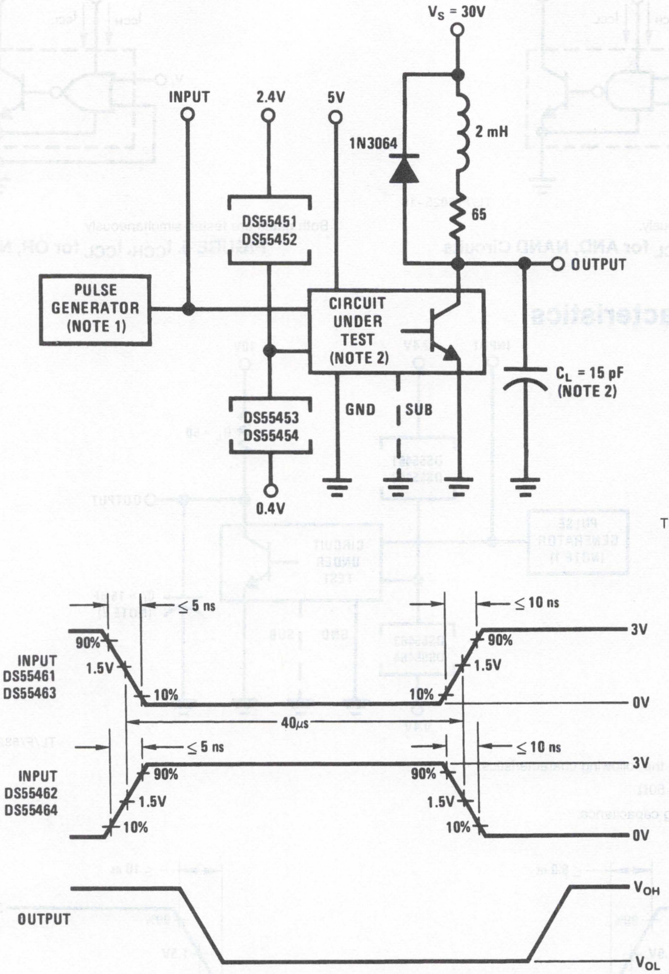
Note 2: C_L includes probe and jig capacitance.


≤ 5.0 ns
≤ 10 ns
3.0V
90%
90%
INPUT
DS55461
DS55463
1.5V
1.5V
10%
10%
0V
0.5μs
≤ 5.0 ns
≤ 10 ns
3.0V
90%
90%
INPUT
DS55462
DS55464
1.5V
1.5V
10%
10%
0V
t_{PHL}
t_{PLH}
V_{OH}
90%
90%
OUTPUT
50%
50%
10%
10%
V_{OL}
t_{THL}
t_{TLH}

TL/F/5825–19

FIGURE 6. Switching Times of Complete Drivers

Switching Characteristics (Continued)


V_S = 30V
INPUT
2.4V
5V
2 mH
1N3064
65
DS55451
DS55452
OUTPUT
PULSE GENERATOR (NOTE 1)
CIRCUIT UNDER TEST (NOTE 2)
C_L = 15 pF (NOTE 2)
DS55453
DS55454
GND
SUB
0.4V
≤ 5 ns
≤ 10 ns
3V
90%
1.5V
10%
0V
INPUT DS55461 DS55463
40μs
INPUT DS55462 DS55464
OUTPUT
V_OH
V_OL

TL/F/5825-20

TL/F/5825-21

Note 1: The pulse generator has the following characteristics:

PRR = 1.25 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 7. Latch-Up Test of Complete Drivers

National Semiconductor

DS2001/μA9665/DS2002/μA9666 DS2003/μA9667/DS2004/μA9668 High Current/Voltage Darlington Drivers

General Description

The DS2001/μA9665/DS2002/μA9666/DS2003/μA9667 DS2004/μA9668 are comprised of seven high voltage, high current NPN Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter base resistors for leakage.

The DS2001/μA9665 is a general purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

The DS2002/μA9666 version does away with the need for any external discrete resistors, since each unit has a resistor and a Zener diode in series with the input. The DS2002/μA9666 was specifically designed for direct interface from PMOS logic (operating at supply voltages from 14V to 25V) to solenoids or relays.

The DS2003/μA9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0V.

The DS2004/μA9668 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6.0V to 15V.

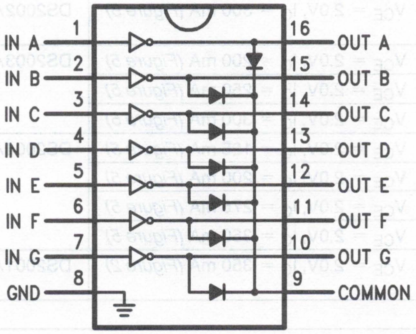
The DS2001/μA9665/DS2002/μA9666/DS2003/μA9667 DS2004/μA9668 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Features

- Seven high gain Darlington pairs
- High output voltage (V_{CE} = 50V)
- High output current (I_C = 350 mA)
- DTL, TTL, PMOS, CMOS compatible
- Suppression diodes for inductive loads
- Extended temperature range

Connection Diagram

16-Lead DIP



TL/F/9647–1

Top View

Order Number DS2001CN, μA9665PC, DS2002CN, μA9666PC, DS2003CN, μA9667PC or DS2004CN, μA9668PC
See NS Package Number N16A

Order Number DS2001CJ, μA9665DC, DS2002CJ, DS2002MJ, μA9666DC, μA9666DM, DS2003CJ, DS2003MJ, μA9667DC, μA9667DM or DS2004CJ, DS2004MJ, μA9668DC, μA9668DM
See NS Package Number J16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
DS2002M/µA9666M	−55°C to +125°C
DS2003M/µA9667M	−55°C to +125°C
DS2004M/µA9668M	−55°C to +125°C
DS2001/µA9665C	0°C to +70°C
DS2002/µA9666C	0°C to +70°C
DS2003/µA9667C	0°C to +70°C
DS2004/µA9668C	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	265°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C.

Input Voltage	30V
Output Voltage	55V
Emitter-Base Voltage	6.0V
Continuous Collector Current	500 mA
Continuous Base Current	25 mA

Electrical Characteristics $T_A = 25°C$, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CEX}	Output Leakage Current	$T_A = 70°C$ for Commercial $V_{CE} = 50V$ *(Figure 1a)*				100	µA
		$V_{CE} = 50V$, $V_I = 6.0V$ *(Figure 1b)*	DS2002/µA9666			500	
		$V_{CE} = 50V$, $V_I = 1.0V$ *(Figure 1b)*	DS2004/µA9668			500	
$V_{CE(Sat)}$	Collector-Emitter Saturation Voltage	$I_C = 350$ mA, $I_B = 500$ µA *(Figure 2)* (Note 3)			1.25	1.6	V
		$I_C = 200$ mA, $I_B = 350$ µA *(Figure 2)*			1.1	1.3	
		$I_C = 100$ mA, $I_B = 250$ µA *(Figure 2)*			0.9	1.1	
$I_{I(ON)}$	Input Current	$V_I = 17V$ *(Figure 3)*	DS2002/µA9666		0.85	1.3	mA
		$V_I = 3.85V$ *(Figure 3)*	DS2003/µA9667		0.93	1.35	
		$V_I = 5.0V$ *(Figure 3)*	DS2004/µA9668		0.35	0.5	
		$V_I = 12V$ *(Figure 3)*			1.0	1.45	
$I_{I(OFF)}$	Input Current (Note 4)	$T_A = 70°C$ for Commercial $I_C = 500$ µA *(Figure 4)*		50	65		µA
$V_{I(ON)}$	Input Voltage (Note 5)	$V_{CE} = 2.0V$, $I_C = 300$ mA *(Figure 5)*	DS2002/µA9666			13	V
		$V_{CE} = 2.0V$, $I_C = 200$ mA *(Figure 5)*	DS2003/µA9667			2.4	
		$V_{CE} = 2.0V$, $I_C = 250$ mA *(Figure 5)*				2.7	
		$V_{CE} = 2.0V$, $I_C = 300$ mA *(Figure 5)*				3.0	
		$V_{CE} = 2.0V$, $I_C = 125$ mA *(Figure 5)*	DS2004/µA9668			5.0	
		$V_{CE} = 2.0V$, $I_C = 200$ mA *(Figure 5)*				6.0	
		$V_{CE} = 2.0V$, $I_C = 275$ mA *(Figure 5)*				7.0	
		$V_{CE} = 2.0V$, $I_C = 350$ mA *(Figure 5)*				8.0	
h_{FE}	DC Forward Current Transfer Ratio	$V_{CE} = 2.0V$, $I_C = 350$ mA *(Figure 2)*	DS2001/µA9665	1000			
C_I	Input Capacitance				15	30	pF
t_{PLH}	Turn-On Delay	0.5 V_I to 0.5 V_O			1.0	5.0	µs
t_{PHL}	Turn-Off Delay	0.5 V_I to 0.5 V_O			1.0	5.0	µs
I_R	Clamp Diode Leakage Current	$V_R = 50V$ *(Figure 6)*				50	µA
V_F	Clamp Diode Forward Voltage	$I_F = 350$ mA *(Figure 7)*			1.7	2.0	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All limits apply to the complete Darlington series except as specified for a single device type.

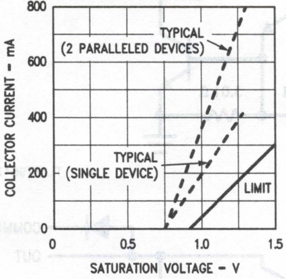
Note 3: Under normal operating conditions these units will sustain 350 mA per output with $V_{CE\,(Sat)} = 1.6V$ at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

Note 4: The $I_{I(OFF)}$ current limit guaranteed against partial turn-on of the output.

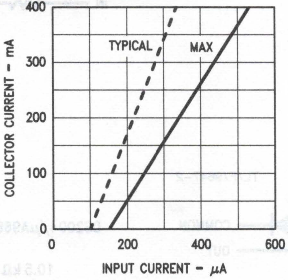
Note 5: The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

Typical Performance Characteristics

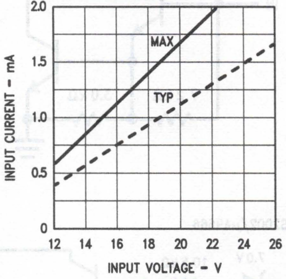
Collector Current vs Saturation Voltage



Collector Current vs Input Current



DS2002/μA9666 Input Current vs Input Voltage



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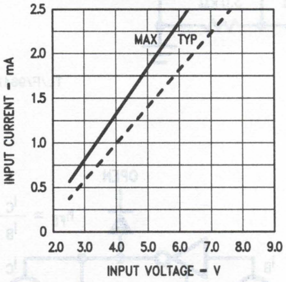
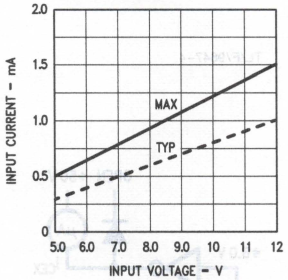
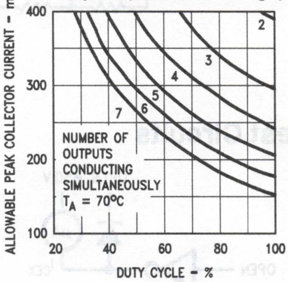
DS2003/μA9667 Input Current vs Input Voltage



DS2004/μA9668 Input Current vs Input Voltage



Peak Collector Current vs Duty Cycle and Number of Outputs (Molded Package)



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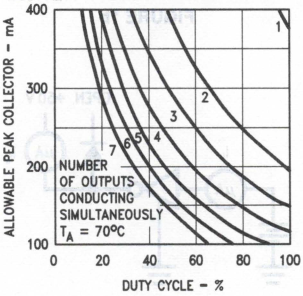
Peak Collector Current vs Duty Cycle and Number of Outputs (Ceramic Package)



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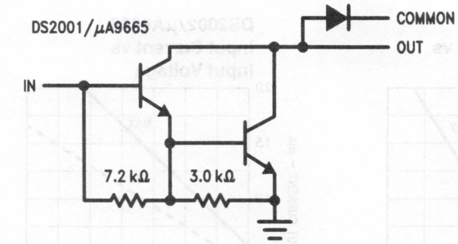
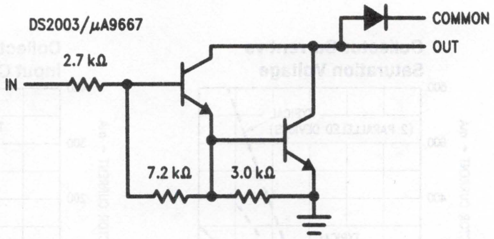
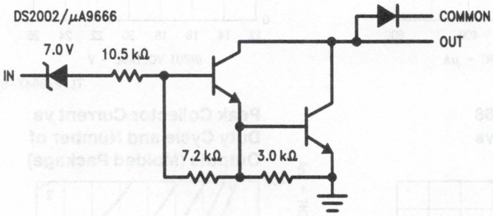
Equivalent Circuits


DS2001/μA9665
COMMON
OUT
IN
7.2 kΩ
3.0 kΩ

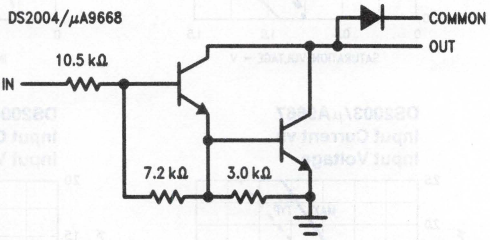
TL/F/9647-2


DS2003/μA9667
COMMON
OUT
2.7 kΩ
IN
7.2 kΩ
3.0 kΩ

TL/F/9647-3


DS2002/μA9666
COMMON
OUT
7.0 V
10.5 kΩ
IN
7.2 kΩ
3.0 kΩ

TL/F/9647-4


DS2004/μA9668
COMMON
OUT
10.5 kΩ
IN
7.2 kΩ
3.0 kΩ

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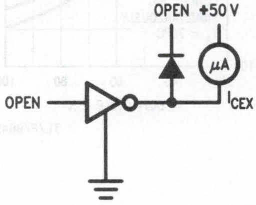
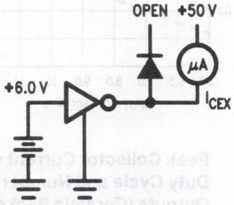
Test Circuits


OPEN
+50 V
μA
OPEN
I_{CEX}

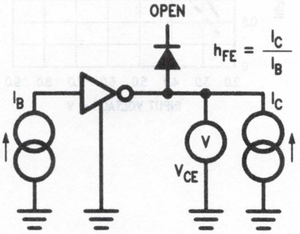
TL/F/9647-7

FIGURE 1a


OPEN
+50 V
μA
+6.0 V
I_{CEX}

TL/F/9647-8

FIGURE 1b


OPEN
$h_{FE} = \frac{I_C}{I_B}$
I_B
I_C
V
V_{CE}

TL/F/9647-9

FIGURE 2

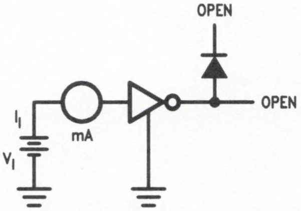

OPEN
OPEN
I_I
mA
V_I

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FIGURE 3

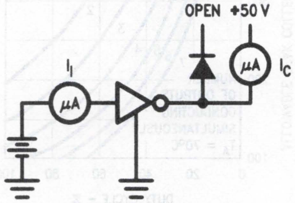
OPEN
+50 V
I_I
μA
μA
I_C

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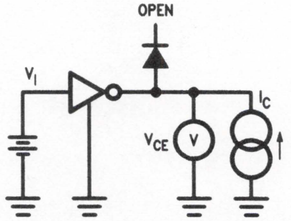
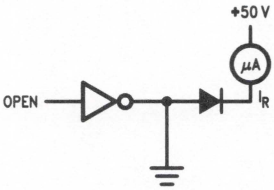
FIGURE 4


OPEN
V_I
I_C
V_{CE}
V

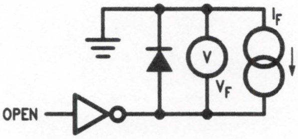
TL/F/9647-12

FIGURE 5


+50 V
μA
OPEN
I_R

TL/F/9647-13

FIGURE 6

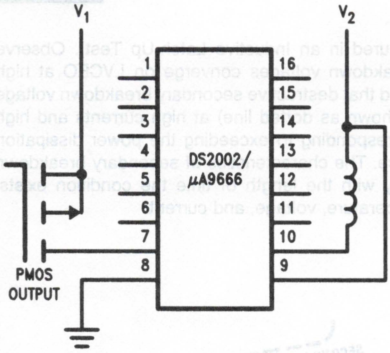


TL/F/9647-14

FIGURE 7

Typical Applications

PMOS to Load


V1
V2
DS2002/
µA9666
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
PMOS
OUTPUT

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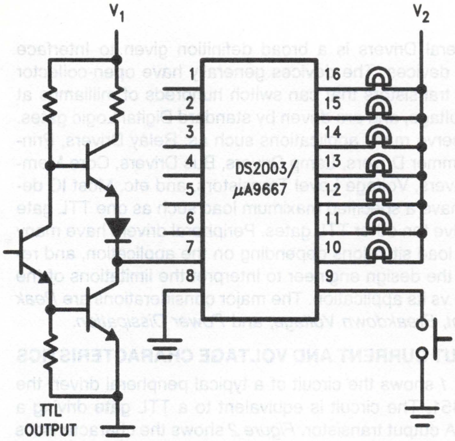
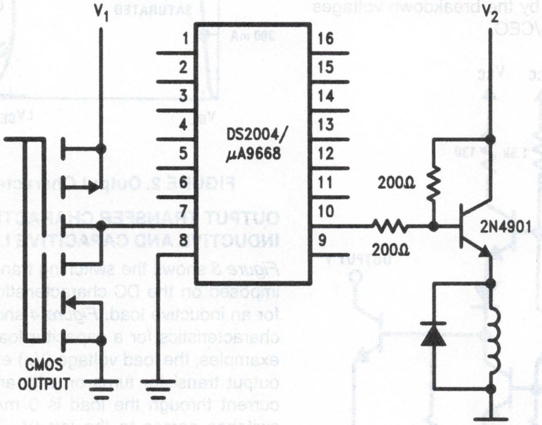
Buffer for Higher Current Loads


V1
V2
DS2003/
µA9667
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LAMP
TEST
TTL
OUTPUT

TL/F/9647–16

TTL to Load


V1
V2
DS2004/
µA9668
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200Ω
200Ω
2N4901
CMOS
OUTPUT

TL/F/9647–17

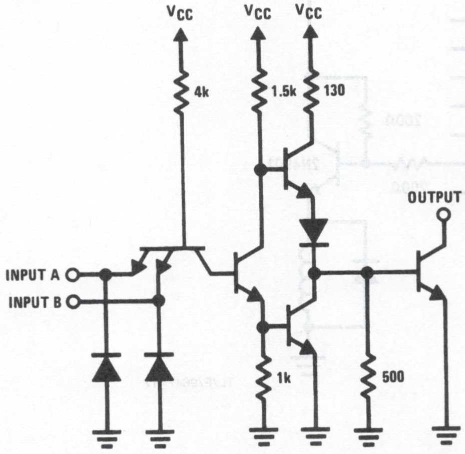
Safe Operating Areas for Peripheral Drivers

National Semiconductor
Application Note 213
Bill Fowler

Peripheral Drivers is a broad definition given to Interface Power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage, and are driven by standard Digital Logic gates. They serve many applications such as: Relay Drivers, Printer Hammer Drivers, Lamp Drivers, Bus Drivers, Core Memory Drivers, Voltage Level Transistors, and etc. Most IC devices have a specified maximum load such as one TTL gate can drive ten other TTL gates. Peripheral drivers have many varied load situations depending on the application, and requires the design engineer to interpret the limitations of the device vs its application. The major considerations are *Peak Current, Breakdown Voltage,* and *Power Dissipation.*

OUTPUT CURRENT AND VOLTAGE CHARACTERISTICS

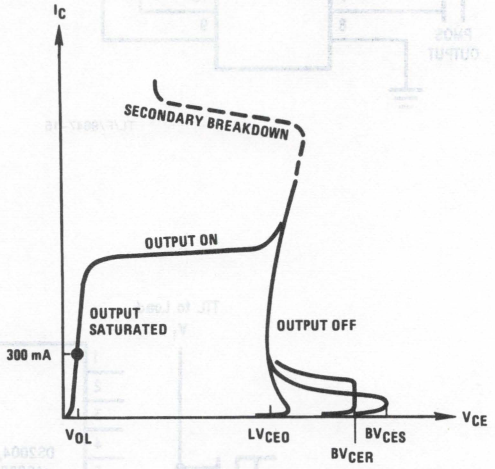
Figure 1 shows the circuit of a typical peripheral driver, the DS75451. The circuit is equivalent to a TTL gate driving a 300 mA output transistor. *Figure 2* shows the characteristics of the output transistor when it is ON and when it is OFF. The output transistor is capable of sinking more than one amp of current when it is ON, and is specified at a $V_{OL} = 0.7V$ at 300 mA. The output transistor is also specified to operate with voltages up to 30V without breaking down, but there is more to that as shown by the breakdown voltages labeled BVCES, BVCER, and LVCEO.



TL/F/5860–1

FIGURE 1. Typical Peripheral Driver DS75451

BVCES corresponds to the breakdown voltage when the output transistor is held off by the lower output transistor of the TTL gate, as would happen if the power supply (V_{CC}) was 5V. BVCER corresponds to the breakdown voltage when the output transistor is held off by the 500 resistor, as would happen if the power supply (V_{CC}) was off (0V). LVCEO corresponds to the breakdown voltage of the output transistor if it could be measured with the base open. LVCEO can be measured by exceeding the breakdown voltage BVCES and measuring the voltage at output currents of 1 to 10 mA on a transistor curve tracer (LVCEO is sometimes measured in an Inductive Latch-Up Test). Observe that all breakdown voltages converge on LVCEO at high currents, and that destructive secondary breakdown voltage occurred (shown as dotted line) at high currents and high voltage corresponding to exceeding the power dissipation of the device. The characteristics of secondary breakdown voltage vary with the length of time the condition exists, device temperature, voltage, and current.



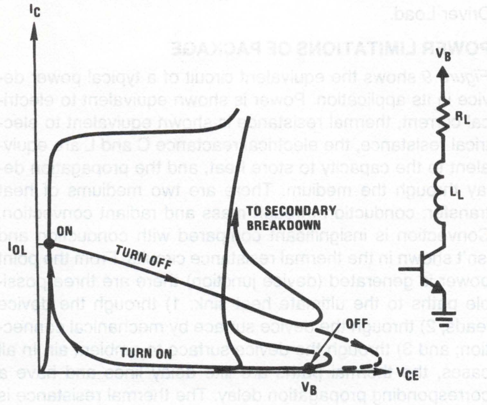
TL/F/5860–2

FIGURE 2. Output Characteristics ON and OFF

OUTPUT TRANSFER CHARACTERISTICS VS INDUCTIVE AND CAPACITIVE LOADS

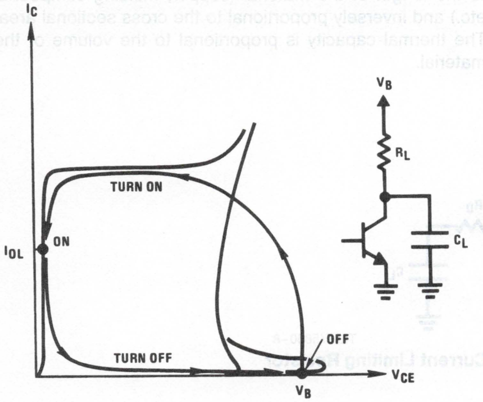
Figure 3 shows the switching transfer characteristics superimposed on the DC characteristics of the output transistor for an inductive load. *Figure 4* shows the switching transfer characteristics for a capacitor load. In both cases in these examples, the load voltage (V_B) exceeds LVCEO. When the output transistor turns on with an inductive load the initial current through the load is 0 mA, and the transfer curve switches across to the left (V_{OL}) and slowly charges the inductor. When the output transistor turns off with an inductive load, the initial current is I_{OL}, which is sustained by the inductor and the transistor curve switches across to the right (V_B) through a high current and high voltage area which exceeds LVCEO and instead of turning off (shown as dotted line) the device goes into secondary breakdown. It is generally not a good practice to let the output transistor's voltage exceed LVCEO with an inductive load.

In a similar case with a capacitive load shown in *Figure 4*, the switching transfer characteristics rotate counter-clockwise through the DC characteristics, unlike the inductive load which rotated clockwise. Even though the switching transfer curve exceeds LVCEO, it didn't go into secondary breakdown. Therefore, it is an acceptable practice to let the output transistor voltage exceed LVCEO, but not exceed BVCER with a capacitive load.


IC
VB
RL
LL
TO SECONDARY BREAKDOWN
ON
IOL
TURN OFF
OFF
TURN ON
VCE
VB

TL/F/5860-3

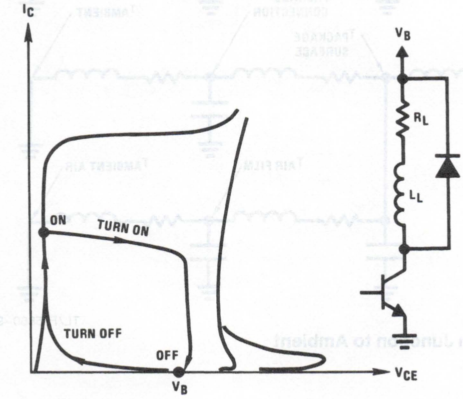
FIGURE 3. Inductive Load Transfer Characteristics


IC
VB
RL
CL
TURN ON
ON
IOL
TURN OFF
OFF
VCE
VB

TL/F/5860-4

FIGURE 4. Capacitive Load Transfer Characteristics

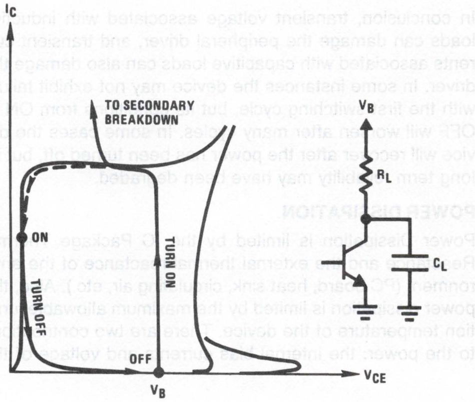
Figure 5 shows an acceptable application with an inductive load. The load voltage (V_B) is less than LVCEO, and the inductive voltage spike caused by the initial inductive current is quenched by a diode connected to V_B.


IC
VB
RL
LL
ON
TURN ON
TURN OFF
OFF
VCE
VB

TL/F/5860-5

FIGURE 5. Inductive Load Transfer Characteristics Clamped by Diode

Figure 6 shows the switching transfer characteristics of a capacitive load which leads to secondary breakdown. This condition occurs due to high sustained currents, not breakdown voltage. In this example, the large capacitor prevented the output transistor from switching fast enough through the high current and high voltage region; in turn the power dissipation of the device was exceeded and the output transistor went into secondary breakdown.

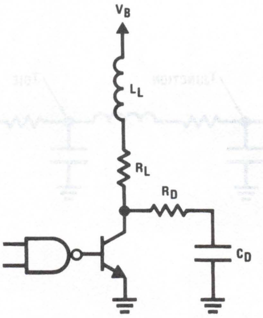

IC
TO SECONDARY BREAKDOWN
VB
RL
ON
TURN ON
TURN OFF
CL
OFF
VB
VCE

TL/F/5860-6

FIGURE 6. Capacitive Load Transfer Characteristics

Figure 7 shows another method of quenching the inductive voltage spike caused by the initial inductive current. This method dampens the switching response by the addition of R_D and C_D. The values of R_D and C_D are chosen to critically dampen the values of R_L and L_L; this will limit the output voltage to 2 × V_B.

$$\frac{L_L}{(R_L + R_D)0} \times \sqrt{\frac{1}{L_L C_D}} \leq 0.5$$


VB
LL
RL
RD
CD

TL/F/5860-7

FIGURE 7. Inductive Load Dampened by Capacitor

Figure 8 shows a method of reducing high sustaining currents in a capacitive load. R_D in series with the capacitor (C_L) will limit the switching transistor without affecting final amplitude of the output voltage, since the IR drop across R_D will be zero after the capacitor is charged.

As an additional warning, beware of parasitic reactance. If the driver's load is located some distance from the driver (as an example: on the inclosure panel or through a connecting cable) there will be additional inductance and capacitance which may cause ringing on the driver output which will exceed LVCEO or transient current that exceeds the sustaining current of the driver. A 300 mA current through a small inductor can cause a good size transient voltage, as compared with 20 mA transient current observed with TTL gates. For no other reason than to reduce the noise associated with these transients, it is good practice to dampen the driver's output.

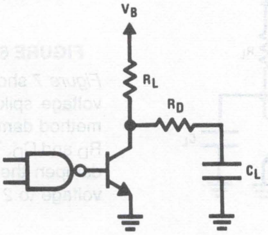
In conclusion, transient voltage associated with inductive loads can damage the peripheral driver, and transient currents associated with capacitive loads can also damage the driver. In some instances the device may not exhibit failure with the first switching cycle, but its conditions from ON to OFF will worsen after many cycles. In some cases the device will recover after the power has been turned off, but its long term reliability may have been degraded.

POWER DISSIPATION

Power Dissipation is limited by the IC Package Thermal Reactance and the external thermal reactance of the environment (PC board, heat sink, circulating air, etc.). Also, the power dissipation is limited by the maximum allowable junction temperature of the device. There are two contributions to the power: the internal bias currents and voltage of the device, and the power on the output of the device due to the Driver Load.

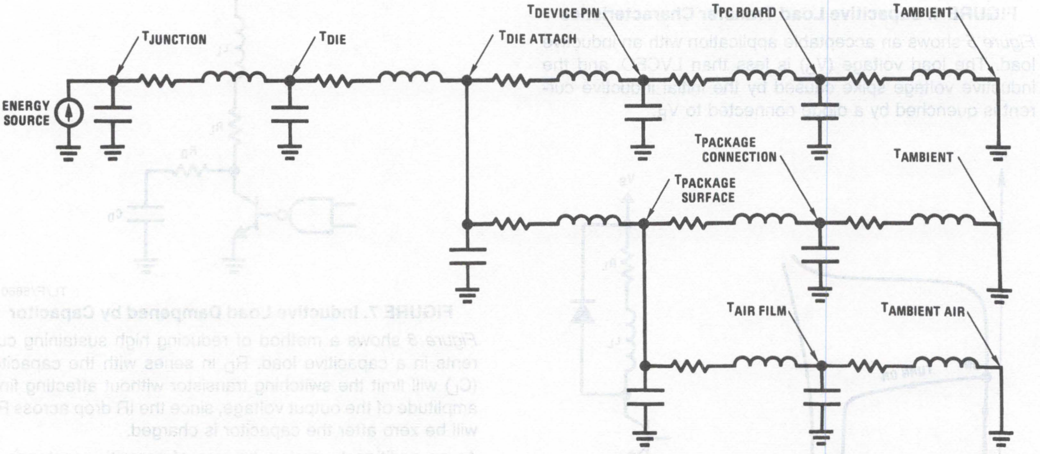
POWER LIMITATIONS OF PACKAGE

Figure 9 shows the equivalent circuit of a typical power device in its application. Power is shown equivalent to electrical current, thermal resistance is shown equivalent to electrical resistance, the electrical reactance C and L are equivalent to the capacity to store heat, and the propagation delay through the medium. There are two mediums of heat transfer: conduction through mass and radiant convection. Convection is insignificant compared with conduction and isn't shown in the thermal resistance circuits. From the point power is generated (device junction) there are three possible paths to the ultimate heat sink: 1) through the device leads; 2) through the device surface by mechanical connection; and 3) through the device surface to ambient air. In all cases, the thermal paths are like delay lines and have a corresponding propagation delay. The thermal resistance is proportional to the length divided by the cross sectional area of the material. The Thermal Inductance is proportional to the length of the material (copper, molding compound, etc.) and inversely proportional to the cross sectional area. The thermal capacity is proportional to the volume of the material.



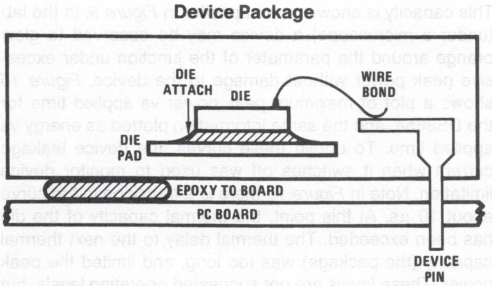
TL/F/5860-8

FIGURE 8. Capacitive Load with Current Limiting Resistor



TL/F/5860-9

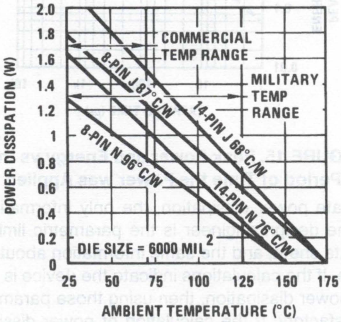
FIGURE 9. Thermal Reactance from Junction to Ambient



TL/F/5860-10

FIGURE 10. Components of Thermal Reactance for a Typical IC Package

National Semiconductor specifies the thermal resistance from device junction through the device leads soldered in a small PC board, measured in one cubic foot of still air. *Figure 11* shows the maximum package power rating for an 8 pin Molded, an 8 pin Ceramic, 14 pin Molded and a 14 pin Ceramic package. The slope of the line corresponds to thermal resistance ($\phi_{JA} = \Delta P/\Delta T$).

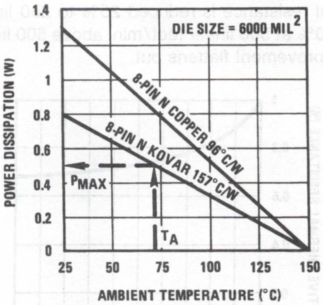


TL/F/5860-11

FIGURE 11. Maximum Package Power Rating

The maximum allowable junction temperature for ceramic packages is 175°C; operation above this temperature will reduce the reliability and life of the device below an acceptable level. At a temperature of 500°C the aluminum metallization paths on the die start to melt. The maximum allowable junction temperature for a molded device is 150°C, operations above this may cause the difference in thermal expansion between the molding compound and package lead frame to sheer off the wire bonds from the die to the package lead. The industry standard for a molded device is 150°C, but National further recommends operation below 135°C if the device in its application will encounter a lot of thermal cycling (such as powered on and off over its life).

The way to determine the maximum allowable power dissipation from *Figure 11*, is to project a line from the maximum ambient temperature (T_A) of the application vertically (shown dotted in *Figure 12*), until the line intercepts the diagonal line of the package type, and then project a line (shown dotted) horizontally until the line intercepts the Power Dissipation Axis (P_{MAX}).



TL/F/5860-12

FIGURE 12. Maximum Package Rating Copper vs Kovar Lead Frame Packages

Figure 11 shows that 14 pin packages have less thermal resistance than 8 pin packages; which should be expected since it has more pins to conduct heat and has more surface area. Something that may not be expected is that the Thermal Resistance of the molded devices is comparable to the ceramic devices. The reason for the lower thermal resistance of the molded devices is the Copper lead frame, which is a better thermal conductor than the Kovar lead frame of the ceramic package. Almost all the peripheral drivers made by National Semiconductor are constructed with Copper lead frames (refer to ϕ_{JA} on the specific devices data sheet). The difference between the thermal resistance of Copper and Kovar in a molded package is shown in *Figure 12*.

Another variance in thermal resistance is the size of the IC die. If the contact area to the lead frame is greater, then the thermal resistance from the Die to the Lead Frame is reduced. This is shown in *Figure 13*. The thermal resistance shown in *Figure 11* corresponds to die that are 6000 mil² in area.

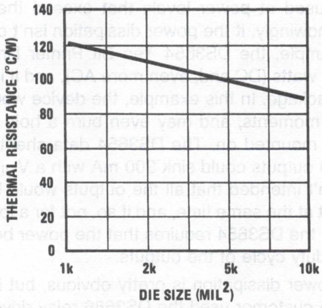


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FIGURE 13. Thermal Resistance vs Die Size

In most applications the prime medium for heat conduction is through the device leads to the PC board, but the thermal resistance can be significantly improved by cooling air driven across the surface of the package. The conduction to air is limited by a stagnant film of air at the surface of the package. The film acts as an additional thermal resistance. The thickness of the film is proportional to its resistance. The thickness of the film is reduced by the velocity of the air across the package as shown in *Figure 14*. In most cases, the thermal resistance is reduced 25% to 250 linear feet/min, and 30% at 500 linear feet/min, above 500 linear feet/min the improvement flattens out.

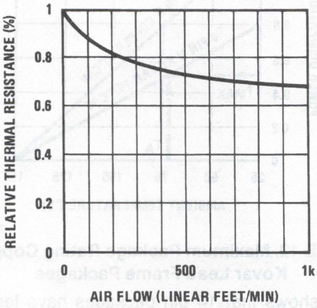

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FIGURE 14. Thermal Resistance vs Air Velocity

The thermal resistance can also be improved by connecting the package to the PC board copper or by attaching metal wings to the package. The improvement by these means is outside the control of the IC manufacturer, but is available from the manufacturer of the heat sink device. If the IC is mounted in a socket rather than soldered to a PC board, the thermal resistance through the device leads will worsen. In most cases, the thermal resistance is increased by 20%; again this is a variable subject to the specific socket type.

The maximum package rating shown in this note corresponds to a 90% confidence level that the package will have thermal resistance equal to or less than the value shown. The thermal resistance varies ±5% about the mean due to variables in assembly and package material.

CALCULATIONS OF POWER DISSIPATION

Most IC devices (such as T^2L) operate at power levels well below the device package rating, but peripheral drivers can easily be used at power levels that exceed the package rating unknowingly, if the power dissipation isn't calculated. As an example, the DS3654 Ten Bit Printer Driver could dissipate 3 watts (DC and, even more AC), and it is only in a 0.8 watt package. In this example, the device would be destroyed in moments, and may even burn a hole in the PC board it is mounted on. The DS3654 data sheet indicated that the 10 outputs could sink 300 mA with a V_{OL} of 1 volt, but it wasn't intended that all the outputs would be sinking this current at the same time, and if so, not for a long period. The use of the DS3654 requires that the power be calculated vs the duty cycle of the outputs.

The DC power dissipation is pretty obvious, but in another example, a customer used the DS3686 relay driver to drive 6.5h inductive load. The DS3687 has an internal clamp network to quench the inductive back swing at 60V. At 5 Hz the device dissipates 2 watts, with transient peaks up to 11 watts. After 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3687 was intended for telephone relay, which in most applications switches 20 times a day.

Peripheral driver will dissipate peak power levels that greatly exceed the average DC power. This is due to the capacity of the die and package to consume the transient energy while still maintaining the junction temperature at a safe level. This capacity is shown as a capacitor in *Figure 9*. In the lab (under a microscope) a device may be observed to glow orange around the parameter of the junction under excessive peak power without damage to the device. *Figure 15* shows a plot of maximum peak power vs applied time for the DS3654, and the same information plotted as energy vs applied time. To obtain these curves, the device leakage current when it switches off was used to monitor device limitation. Note in *Figure 15* there is a transition in the curve about 10 µs. At this point, the thermal capacity of the die has been exceeded. The thermal delay to the next thermal capacity (the package) was too long, and limited the peak power. These levels are not suggested operating levels, but an example of a Peripheral Driver to handle peak transient power.

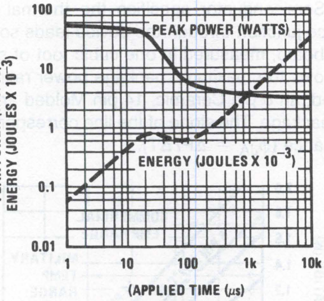

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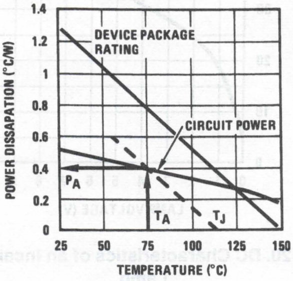
FIGURE 15. Peak Power and Energy vs the Period of Time the Power was Applied

To calculate power dissipation, the only information available to the design engineer is the parametric limits in the device data sheet, and the same information about the load reactance. If the calculations indicate the device is within its limits of power dissipation, then using those parametric limits is satisfactory. If the calculation of power dissipation is marginal, the parametric limits used in the calculations might be worst case at low temperature instead of high temperature due to a positive temperature coefficient (T_C) of resistance. IC resistors and resistors associated with the load generally have a positive T_C. On the other hand, diodes and transistor emitter base voltages have a negative T_C; which may in some circuits negate the effect of the resistors T_C. Peripheral output transistors have a positive T_C associated with V_{OL}; while output Darlington transistors have a negative T_C at low currents and may be flat at high currents. *Figure 16* shows an example of power dissipation vs temperature; note that the power dissipation at the application's maximum temperature (T_A) was less than the power dissipation at lower temperatures. Since maximum junction temperature is the concern of the calculation, then maximum ambient temperature power should be used. The junction temperature may be determined by projecting a line (shown dotted in *Figure 16*), with a slope proportional to ϕ_{JA} back to the horizontal axis (shown as T_J). If the point is below the curve then T_J will be less than 150°C. T_J must not exceed the maximum junction temperature for that package type. In this example, T_J is less than 150°C as required by a molded package. To calculate the power vs temperature, it is necessary to characterize the device parameters vs temperature. Unfortunately, this information is not always provided by IC manufacturers in the device data sheets. A method to calculate I_{CC} vs temperature is to measure a device, then normalize the measurements vs the typical value for I_{CC} in the data sheet, then worst case the measurements by adding 30%. Thirty percent is normally the worst-case resistor tolerance that IC devices are manufactured to.



TL/F/5860–16

FIGURE 16. IC Power Dissipation vs Temperature

CALCULATION OF OUTPUT POWER WITH AN INDUCTIVE LOAD

For this example, the device output circuit is similar to the DS3654 (10-Bit Printer Solenoid Driver) and the DS3686 and DS3687 (Telephone Relay Driver) as shown in *Figure 17*. Special features of the circuit type are the Darlington output transistors Q1 and Q2 and the zener diode from the collector of Q2 to the base of Q2. The Darlington output requires very little drive from the logic gate driving it and in turn dissipates less power when the output is turned ON and OFF, than a single saturating transistor output would. The zener diode (D_Z) quenches the inductive backswing when the output is turned OFF.

Device and Load Characteristics Used for Power Calculation

V_{OL}	Output Voltage ON	1.5V
V_C	Output Clamp Voltage	65V
V_B	Load Voltage	30V
R_L	Load Resistance	120Ω
L_L	Load Inductance	5h
T_{ON}	Period ON	100 ms
T_{OFF}	Period OFF	100 ms
T	Total Period	200 ms

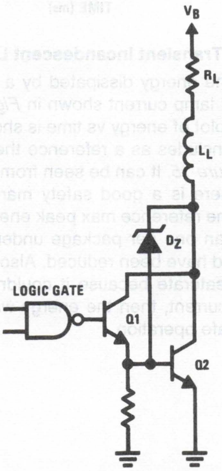


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FIGURE 17. Peripheral Driver with Inductive Load

Refer to *Figure 18* voltage and current waveforms corresponding to the power dissipation calculated for this example of an inductive load.

P_{ON} = Average power dissipation in device output when device is ON during total period (T)

$$\tau = \frac{L_L}{R_L} = \frac{5h}{120\Omega} = 41.7\text{ ms}$$

$$I_L = \frac{V_B - V_{OL}}{R_L} = \frac{30 - 1.5}{120} = 237.5\text{ mA}$$

$$I_P = I_L\,(1 - e^{-T_{ON}/\tau})$$

$$I_P = 237.5\text{ mA}\,(1 - e^{-100\text{ ms}/41.7\text{ ms}})$$

$$I_P = 215.9\text{ mA}$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \int_{\circ}^{T_{ON}} \frac{e^{-t/\tau}\,dt}{T_{ON}}\right]$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \frac{\tau}{T_{ON}}(1 - e^{-T_{ON}/\tau})\right]$$

$$P_{ON} = 1.5 \times 237.5\text{ mA} \times \frac{100}{200}\left[1 - \frac{41.7}{100}(1 - e^{-100/41.7})\right]$$

$$P_{ON} = 110.6\text{ mW}$$

P_{OFF} = Average power dissipation in device output when device is OFF during total period (T)

$$I_R = \frac{V_C - V_B}{R_L} = \frac{65 - 30}{120\Omega} = 291.7\text{ mA}$$

$$t_x = \tau\,\ell n\left(\frac{I_P + I_R}{I_R}\right)$$

$$t_x = 41.7\text{ ms}\;\ell n\left(\frac{215.9 + 291.7}{291.7}\right) = 23.1\text{ ms}$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R)\int_{\circ}^{t_x} \frac{e^{-t/\tau}\,dt}{t_x} - I_R\right]$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R) \times s\frac{\tau}{t_x}(1 - e^{-t_x/\tau}) - I_R\right]$$

$$P_{OFF} = 65 \times \frac{23.1}{200}\left[(215.9\text{ mA} + 291.7\text{ mA})\frac{41.7}{23.1}(1 - e^{-23.1/41.7}) - 291.7\text{ mA}\right]$$

$$P_{OFF} = 736\text{ mW}$$

P_O = Average power dissipation in device output

$$P_O = P_{ON} + P_{OFF} = 110.6 + 736 = 846.6\text{ mW}$$

In the above example, driving a 120Ω inductive load at 5 Hz, the power dissipation exceeded a more simple calculation of power dissipation, which would have been:

$$P_O = \frac{V_{OL}\,(V_B - V_{OL})}{R_L} \times \frac{T_{ON}}{T}$$

$$P_O = \frac{1.5\,(30 - 1.5)}{120} \times \frac{100\text{ ms}}{200\text{ ms}} = 182.5\text{ mW}$$

An error 460% would have occurred by not including the reactive load. The total power dissipation must also include other outputs (if the device has more than one output), and the power dissipation due to the device power supply currents. This is an example where the load will most likely exceed the device package rating. If the load is fixed, the power can be reduced by changing the period (T) and duty rate (T_{ON}/T_{OFF}).

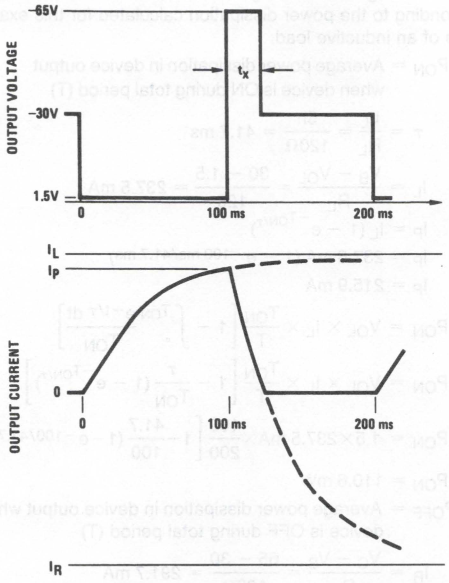

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FIGURE 18. Voltage and Current Waveforms Corresponding to Inductive Load

CALCULATION OF OUTPUT POWER WITH AN INCANDESCENT LAMP

An incandescent lamp is equivalent to a reactive load. The reactance is related to the period of time required to heat the lamp and the filaments positive temperature coefficient of resistance. *Figure 19* shows the transient response for a typical lamp used on instrument panels, and the equivalent electrical model for the lamp. Much like IC packages the lamp has a thermal circuit and its associated propagation delay. This lamp filament has an 8 ms time constant, and a longer 250 ms time constant from the lamp body to ambient. The DC characteristics are shown in *Figure 20*. Note the knee in the characteristics at 2 volts; this is where power starts to be dissipated in the form of light. This subject is important, since more peripheral drivers are damaged by lamps than any other load.

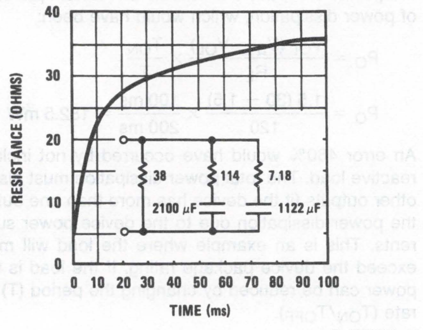

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FIGURE 19. Transient Response of an Incandescent Lamp

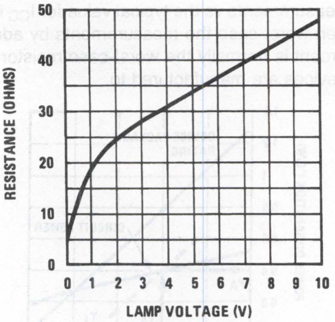

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FIGURE 20. DC Characteristics of an Incandescent Lamp

Figure 21 shows the transient response of a driver similar to a DS75451 driving the lamp characterized in *Figures 19* and *20*. The equivalent load doesn't include the reactance of the lamp base to ambient, which has a 250 ms time constant, since 10 ms to an IC is equivalent to DC. The peak transient current was 1 amp, settling to 200 ms, with an 8 ms time constant. Observe the peak current is clamped at 1 amp, by the sinking ability of the driver; otherwise the peak current may have been 1.2 amps. The DS75451 is only rated at 300 mA, but it is reasonable to assume it could sink 1 amp because of the designed force β required for switching response and worst case operating temperature.

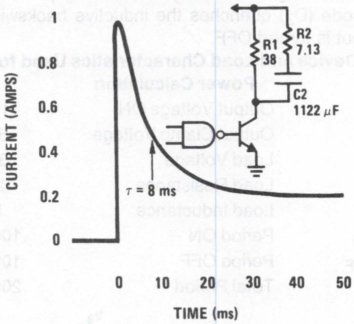

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FIGURE 21. Transient Incandescent Lamp Current

Calculation of the energy dissipated by a peripheral driver for the transient lamp current shown in *Figure 21* is shown above, and the plot of energy vs time is shown in *Figure 22*. *Figure 22* also includes as a reference the maximum peak energy from *Figure 15*. It can be seen from *Figure 22* that in this example there is a good safety margin between the lamp load and the reference max peak energy. If there were more drivers than one per package under the same load, the margin would have been reduced. Also, if the peripheral driver couldn't saturate because it couldn't sink the peak transient lamp current, then the energy would also reduce the margin of safe operation.

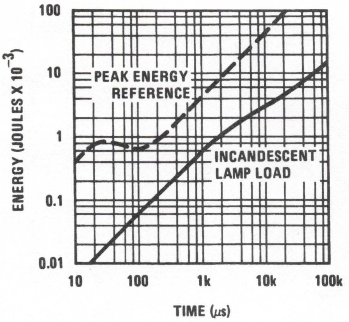

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FIGURE 22. Energy vs Time for a Peripheral Driver with an Incandescent Lamp Load

CALCULATION OF ENERGY IN AN INCANDESCENT LAMP

$$\text{Energy} = \int_{\circ}^{t} V_{OL} (I_{R1} + I_{R2})\, dt$$

$$i_{R1} = \frac{V_B - V_{OL}}{R1} = I_{R1}$$

$$i_{R2} = \left(\frac{V_B - V_{OL}}{R2}\right) e^{-t/\tau}$$

$$= I_{R2}\, e^{-t/\tau} \quad \tau = R2C2$$

$$\text{Energy} = \int_{\circ}^{t} V_{OL} (I_{R1} + I_{R2}\, e^{-t/\tau})\, dt$$

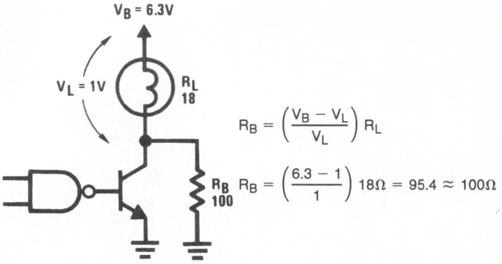
$$= V_{OL} [I_{R1} t + I_{R2} \tau (i - e^{-t/\tau})]$$

Given: $V_{OL} = 0.6V$

$I_{R1} = 0.2$ Amps

$I_{R1} + I_{R2} = 1$ Amp

A common technique used to reduce the 10 to 1 peak to DC transient lamp current is to bias the lamp partially ON, so the lamp filament is warm. This can be accomplished as shown in *Figure 23*. From *Figure 20* it can be seen that the lamp resistance at 0V is 5.7Ω, but at 1V the resistance is 18Ω. At 1V the lamp dosen't start to emit light. Using a lamp resistance of 100Ω and lamp voltage of 1V, R_B was calculated to be approximately 100Ω. This circuit will reduce the peak lamp current from 1 amp to 316 mA.



$$R_B = \left(\frac{V_B - V_L}{V_L}\right) R_L$$

$$R_B = \left(\frac{6.3 - 1}{1}\right) 18\Omega = 95.4 \approx 100\Omega$$

TL/F/5860-23

FIGURE 23. Circuit Used to Reduce Peak Transient Lamp Current

PERIPHERAL DRIVER SECTION

National Semiconductor has a wide selection of peripheral drivers as shown in this section's guide. The DS75451, DS75461, DS3631 and the DS3611 series have the same selection of logic function in an 8-pin package. The DS75461 is a high voltage selection of the DS75451 and may switch slower. The DS3611 and DS3631 are very high voltage circuits and were intended for slow relay applications. The DS3680, DS3686, and DS3687 were intended for 56V telephone relay applications. The DS3654 contains a 10-bit shift register followed by ten 250 mA clamped drivers. The DS3654 was intended for printer solenoid applications.

High current and high voltage peripheral drivers find many applications associated with digital systems, and it is the intention of the application note to insure that reliability and service life of peripheral drivers equal or exceed the performance of the other logic gates made by National.

For additional information, please contact the Interface Marketing Department at National or one of the many field application engineers world-wide.

Section 4
Display Drivers

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National Semiconductor

Display Drivers

MOS/LSI DISPLAY DRIVERS

National's comprehensive family of display drivers provides direct interface to all of the common display technologies—light-emitting diode (LED), liquid crystal display (LCD), and vacuum fluorescent (VF).

FUNCTION SIMILAR FAMILY

Each driver utilizes a simple serial-data input channel, on-chip shift register, latches and buffer/driver outputs. The serial input channel allows direct interface to most microprocessors, including COPS™, NSC800™, 8080 series, and TMS1000 series. Besides a serial-data input, each driver requires a clock input. Some offer a latch (data) input and/or data output for easy cascade interconnect of additional drivers.

Once loaded, the shift register data can be transferred to the on-chip latches, which then output to the buffer/driver and respective display. This buffer/driver is where each provides the unique driver interface desired by the particular display technology—LED, LCD, or VF.

THE MM58241 SERIES—VF

Each of the products in the MM58241 series provides high-voltage (several up to 60V) drive of VF displays. All are ideal for direct or multiplexed interface to large complex VF panel arrays or 5 × 7 (or larger) dot-matrix character strings. Each of the drivers are cascadable for further expansion. Application note AN-371 provides further details and other application information.

THE MM5450 SERIES—LED

National's MM5450 series of LED display drivers rounds out this comprehensive product family. This popular series offers direct drive of LED displays by providing up to 25 mA of current drive per LED segment.

CMOS/LSI

Many of the products in the display driver family utilize CMOS technology and are further evidence of National's capabilities and commitment to CMOS/LSI—the technology of the '80s.

In addition, National offers a line of bipolar segment and digit drivers with a broad range of output sink and source currents.

Detailed features/functions of the 16-member display driver family are high-lighted in the following product guide.

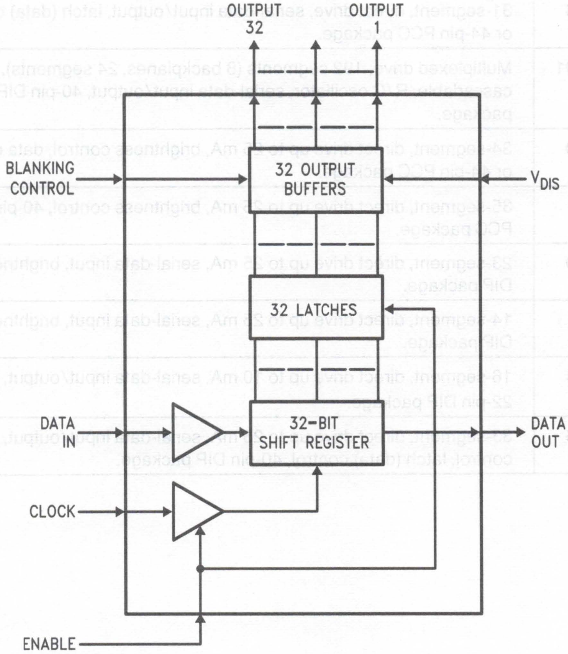

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FIGURE 1. Typical Block Diagram

National Semiconductor

LSI Display Driver Selection Guide

Display Technology	Product Number	Features	Page No.
Vacuum Fluorescent (VF)	MM58241	32-segment, direct/multiplexed drive to 60V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.	4-82
VF	MM58242	20-digit, direct/multiplexed drive to 60V, data enable, brightness control, cascadable, 28-pin DIP or PCC package.	4-87
VF	MM58248	35-segment, direct/multiplexed drive to 60V, pin-compatible to MM5448, 40-pin DIP or 44-pin PCC package.	4-92
VF	MM58341	32-segment, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.	4-97
VF	MM58342	20-digit, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 28-pin DIP or PCC package.	4-102
VF	MM58348	35-segment, direct/multiplexed drive to 35V, pin-compatible to MM5448, 40-pin DIP or 44-pin PCC package.	4-107
Liquid Crystal (LCD)	MM5452	32-segment, direct drive, serial-data input, data enable, on-chip backplane (B/P) oscillator, 40-pin DIP or 44-pin PCC package.	4-50
LCD	MM5453	33-segment, direct drive, serial-data input, B/P oscillator, 40-pin DIP or 44-pin PCC package.	4-50
LCD	MM5483	31-segment, direct drive, serial-data input/output, latch (data) control, 40-pin DIP or 44-pin PCC package.	4-65
LCD	MM58201	Multiplexed drive, 192 segments (8 backplanes, 24 segments), 192-bit RAM, cascadable, R/C oscillator, serial-data input/output, 40-pin DIP or 44-pin PCC package.	4-76
Light-Emitting Diode (LED)	MM5450	34-segment, direct drive up to 25 mA, brightness control, data enable, 40-pin DIP or 44-pin PCC package.	4-44
LED	MM5451	35-segment, direct drive up to 25 mA, brightness control, 40-pin DIP or 44-pin PCC package.	4-44
LED	MM5480	23-segment, direct drive up to 25 mA, serial-data input, brightness control, 28-pin DIP package.	4-57
LED	MM5481	14-segment, direct drive up to 25 mA, serial-data input, brightness control, 20-pin DIP package.	4-61
LED	MM5484	16-segment, direct drive up to 10 mA, serial-data input/output, cascadable, 22-pin DIP package.	4-68
LED	MM5486	33-segment, direct drive up to 25 mA, serial-data input/output, brightness control, latch (data) control, 40-pin DIP package.	4-71

National Semiconductor

Bipolar Display Driver Selection Guide

LED Display Segment Drivers

Device Number and Temperature Range		Drivers/ Package	I_O/Segment (mA)		V_{MAX} (V)		Comments	Page No.
0°C to +70°C	−55°C to +125°C		Sink* (Common Anode)	Source (Common Cathode)	Input	Supply		
DS75491		4	50	50	15	10		4-6
DS75493	DS55493	4		30	10	10	Programmable Constant Current	4-9
DS8654		8		50	36	36		4-14

*Digit drivers with output sink capability may be used to drive segments of "common anode" displays.

LED Display Digit Drivers

Device Number and Temperature Range		Drivers/ Package	I_O/Digit (mA)		V_{MAX} (V)		Comments	Page No.
0°C to +70°C	−55°C to +125°C		Sink (Common Anode)	Source (Common Cathode)	Input	Supply		
DS75491		4		50	10	10		4-6
DS75494	DS55494	6	150		10	10	Enable Control	4-12
DS75492		6	250		10	10		4-6
DS8870		6	350		10	10	DS75492 Pinout, Darlington Output	4-24
DS8863		8	500		15	10		4-21
DS8963			500		23	18		4-21
DS8654				50	36	36		4-14
DS8874			50		10	10	Serial Shift Register Input	4-26
DS8973			100		10	10	3-Cell Operation—Low Battery Indicator	4-39
DS3654		10	400		9.5	45	Serial Input	3-17

Gas Discharge Display Drivers

Device Number and Temperature Range		Device Type	Drivers/ Package	Comments	Page No.
0°C to +70°C	−55°C to +125°C				
DS8880	DS7880	Cathode Drivers	7	BCD to 7-Segment	4-28
DS8884A			7	BCD to 7-Segment with Comma and DP	4-36

Vacuum Fluorescent Display Drivers

Device Number and Temperature Range		Device Type	Drivers/ Package	Comments	Page No.
0°C to +70°C	−55°C to +125°C				
DS8654		Ground Driver (segments)	8	7-Segment plus DP	4-14
DS8654		Anode Driver (digit)	8		4-14

National Semiconductor

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

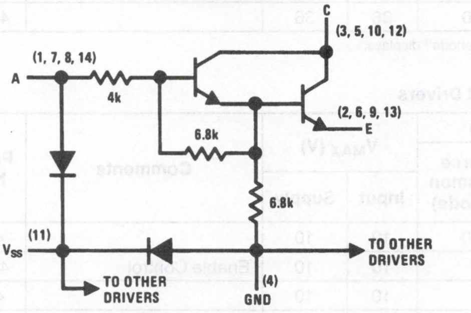
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LEDs in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

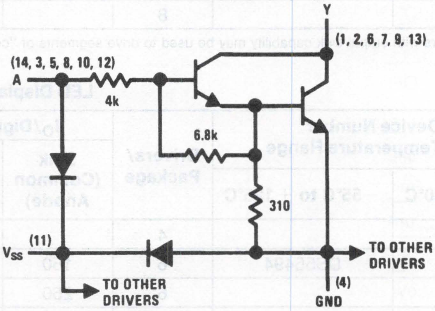
Schematic and Connection Diagrams

DS75491 (each driver)


C
(3, 5, 10, 12)
(1, 7, 8, 14)
A
4k
(2, 6, 9, 13)
E
6.8k
6.8k
(11)
V_{SS}
TO OTHER DRIVERS
TO OTHER DRIVERS
(4)
GND

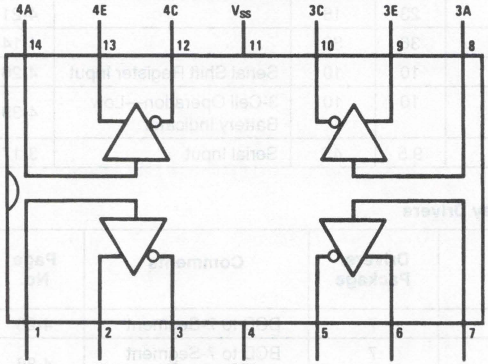
TL/F/5830–1

DS75492 (each driver)


Y
(1, 2, 6, 7, 9, 13)
(14, 3, 5, 8, 10, 12)
A
4k
6.8k
310
(11)
V_{SS}
TO OTHER DRIVERS
TO OTHER DRIVERS
(4)
GND

TL/F/5830–2

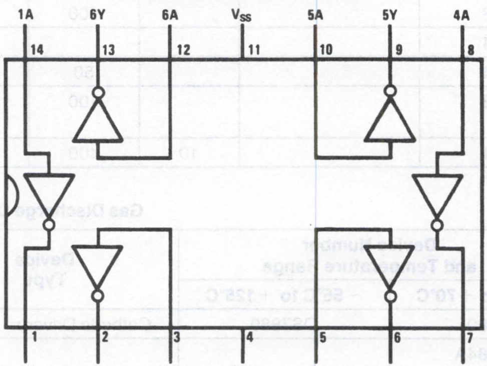
DS75491 Dual-In-Line Package


4A
4E
4C
V_{SS}
3C
3E
3A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1E
1C
GND
2C
2E
2A

TL/F/5830–3

Top View

DS75492 Dual-In-Line Package


1A
6Y
6A
V_{SS}
5A
5Y
4A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
2Y
2A
GND
3A
3Y
4Y

TL/F/5830–4

Top View

Order Number DS75491J, DS75492J, DS75491N or DS75492N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	DS75491	DS75492
Input Voltage Range (Note 4)	$-5V$ to V_{SS}	
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal with Respect to any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA

	DS75491	DS75492
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temp. (Soldering, 10 sec)	300°C	300°C
Maximum Power Dissipation at 25°C		
Cavity Package	1308 mW*	1364 mW†
Molded Package	1207 mW*	1280 mW†

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

†Derate cavity package 9.09 mW/°C; derate molded package 10.24 mW/°C above 25°C.

Electrical Characteristics $V_{SS} = 10V$ (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS75491							
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, $V_E = 5V$, $I_C = 50$ mA	$T_A = 25°C$		0.9	1.2	V
			$T_A = 0–70°C$			1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	$V_C = 10V$, $V_E = 0V$	$I_{IN} = 40\ \mu A$			100	µA
			$V_{IN} = 0.7V$			100	µA
I_I	Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $V_E = 0V$, $I_C = 20$ mA			2.2	3.3	mA
I_E	Emitter Reverse Current	$V_{IN} = 0V$, $V_E = 5V$, $I_C = 0$ mA				100	µA
I_{SS}	Current Into V_{SS} Terminal					1	mA
DS75492							
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, $I_{OUT} = 250$ mA	$T_A = 25°C$		0.9	1.2	V
			$T_A = 0–70°C$			1.5	V
I_{OH}	High Level Output Current	$V_{OH} = 10V$	$I_{IN} = 40\ \mu A$			200	µA
			$V_{IN} = 0.5V$			200	µA
I_I	Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $I_{OL} = 20$ mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics $V_{SS} = 7.5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS75491						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	$V_{IH} = 4.5V$, $V_E = 0V$, $R_L = 200\Omega$, $C_L = 15$ pF		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)			20		ns
DS75492						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{IH} = 7.5V$, $R_L = 39\Omega$, $C_L = 15$ pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

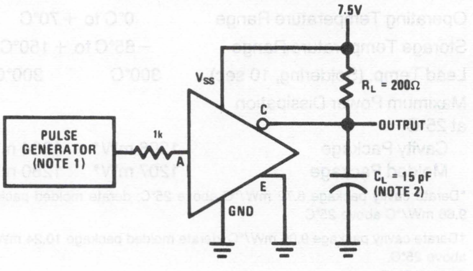
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

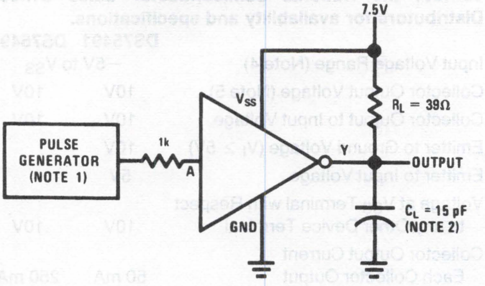
AC Test Circuits and Switching Time Waveforms

DS75491

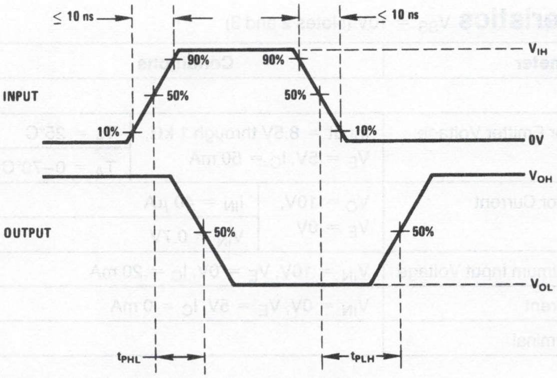

7.5V
V_{SS}
$R_L = 200\Omega$
C
OUTPUT
PULSE GENERATOR (NOTE 1)
1k
A
E
GND
$C_L = 15$ pF (NOTE 2)

TL/F/5830-5

DS75492


7.5V
V_{SS}
$R_L = 39\Omega$
PULSE GENERATOR (NOTE 1)
1k
A
Y
OUTPUT
GND
$C_L = 15$ pF (NOTE 2)

TL/F/5830-6


≤ 10 ns
≤ 10 ns
V_{IH}
90%
90%
INPUT
50%
50%
10%
10%
0V
V_{OH}
OUTPUT
50%
50%
V_{OL}
t_{PHL}
t_{PLH}

TL/F/5830-7

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 100 kHz, $t_W = 1\ \mu s$.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS55493/DS75493 Quad LED Segment Driver

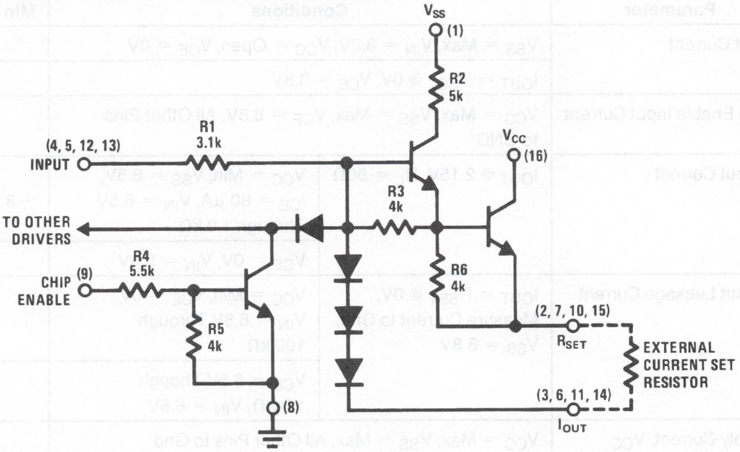
General Description

The DS55493/DS75493 is a quad LED segment driver. It is designed to interface between MOS IC's and LED's. An external resistor is required for each segment to drive the output current which is approximately equal to $0.7V/R_L$ and is relatively constant, independent of supply variations. Blanking can be achieved by taking the chip enable (CE) to a logical "1" level.

Features

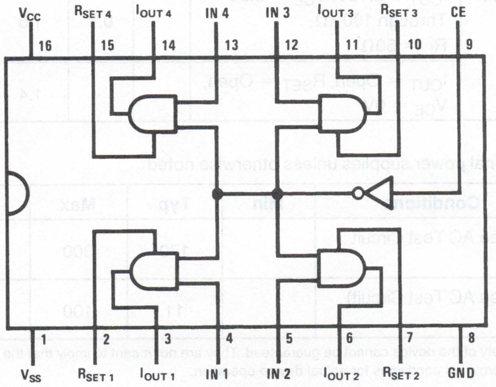
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Output current regulation
- Quad high gain circuits

Schematic and Connection Diagrams


V_SS
(1)
R2
5k
R1
3.1k
(4, 5, 12, 13)
INPUT
V_CC
(16)
R3
4k
TO OTHER DRIVERS
R6
4k
R4
5.5k
(9)
CHIP ENABLE
R5
4k
(2, 7, 10, 15)
R_SET
EXTERNAL CURRENT SET RESISTOR
(3, 6, 11, 14)
I_OUT
(8)

TL/F/7561–1

Dual-In-Line Package


V_CC
R_SET 4
I_OUT 4
IN 4
IN 3
I_OUT 3
R_SET 3
CE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
V_SS
R_SET 1
I_OUT 1
IN 1
IN 2
I_OUT 2
R_SET 2
GND

TL/F/7561–2

Order Number DS55493J, DS75493J or DS75493N
See NS Package Number J16A or N16A

Truth Table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	−65°C to +150°C
Output Current (I_{OUT})	−25 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.14 mW/°C above 25°C; derate molded package 10.24 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature T_A			
DS75493	0	+70	°C
DS55493	−55	+125	°C

Electrical Characteristics ($V_{SS} \geq V_{CC}$) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IN}	Input Current	V_{SS} = Max, V_{IN} = 8.8V, V_{CC} = Open, V_{CE} = 0V				3.2	mA
		I_{OUT} = R_{SET} @ 0V, V_{CE} = 8.8V				3.6	mA
I_{CE}	Chip Enable Input Current	V_{CC} = Max, V_{SS} = Max, V_{CE} = 8.8V, All Other Pins to GND				2.1	mA
I_{OUT}	Output Current	I_{OUT} @ 2.15V, R_L = 50Ω	V_{CC} = Min, V_{SS} = 6.5V, I_{CE} = 80 μA, V_{IN} = 6.5V Through 1.0 kΩ	−8	−13		mA
			V_{CE} = 0V, V_{IN} = 8.8V		−16	−20	mA
I_{OL}	Output Leakage Current	I_{OUT} = R_{SET} @ 0V, Measure Current to Gnd, V_{SS} = 8.8V	V_{CC} = Min, V_{CE} = 0V V_{IN} = 8.8V Through 100 kΩ			−200	μA
			V_{CE} = 6.5V Though 1.0 kΩ, V_{IN} = 8.8V			−100	μA
I_{CC}	Supply Current, V_{CC}	V_{CC} = Max, V_{SS} = Max, All Other Pins to Gnd				40	μA
I_{SS}	Supply Current	V_{CC} = 0V, All Other Pins to Gnd				40	μA
		V_{CC} = Min, V_{SS} = 8.8V	I_{OUT} @ 2.15V, V_{CE} = 8.8V Through 100 kΩ, R_L = 50Ω		0.5	1.5	mA
			I_{OUT} = Open, R_{SET} = Open, V_{CE} = 0V			1.4	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

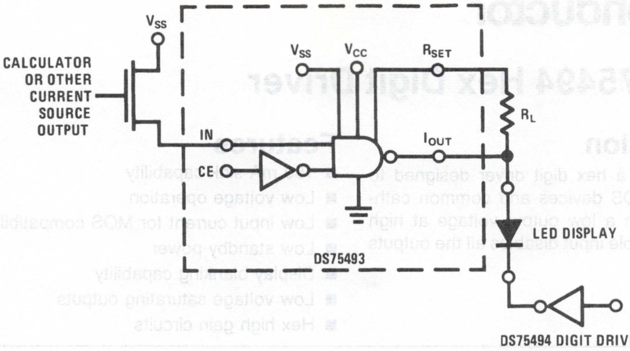
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd(OFF)}$	Propagation Delay to a Logical "0" From Input to Output	(See AC Test Circuit		170	300	ns
$t_{pd(ON)}$	Propagation Delay to a Logical "1" From Input to Output	(See AC Test Circuit)		11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75493 and across the −55°C to +125°C range for the DS55493.

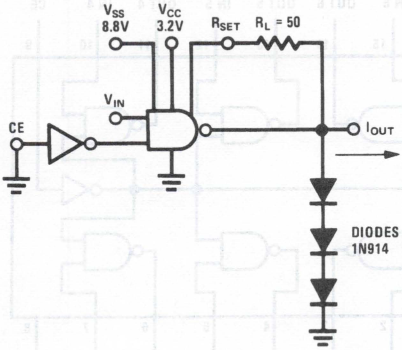
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications


V_{SS}
CALCULATOR OR OTHER CURRENT SOURCE OUTPUT
V_{SS}
V_{CC}
R_{SET}
R_L
IN
I_{OUT}
CE
LED DISPLAY
DS75493
DS75494 DIGIT DRIVER

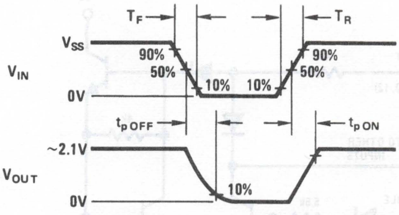
TL/F/7561–3

AC Test Circuit


V_{SS} 8.8V
V_{CC} 3.2V
R_{SET}
R_L = 50
V_{IN}
CE
I_{OUT}
DIODES 1N914

TL/F/7561–4

Switching Time Waveforms



TL/F/7561–5

National Semiconductor

DS55494/DS75494 Hex Digit Driver

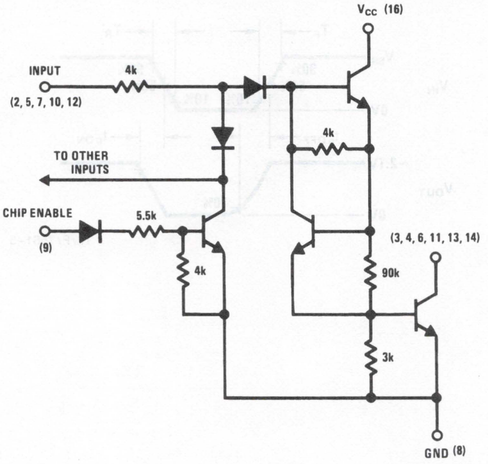
General Description

The DS55494/DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

Features

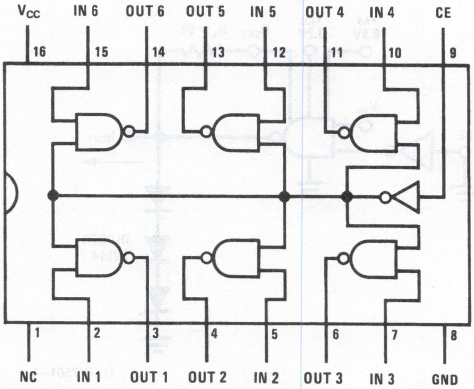
- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams


V_{CC} (16)
INPUT
4k
(2, 5, 7, 10, 12)
TO OTHER INPUTS
4k
CHIP ENABLE
5.5k
(9)
4k
(3, 4, 6, 11, 13, 14)
90k
3k
GND (8)

TL/F/5832–1

Dual-In-Line Package


V_{CC}
IN 6
OUT 6
OUT 5
IN 5
OUT 4
IN 4
CE
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
NC
IN 1
OUT 1
OUT 2
IN 2
OUT 3
IN 3
GND

TL/F/5832–2

Top View

Order Number DS55494J, DS75494J or DS75494N

See NS Package Number J16A or N16A

Truth Table

Enable	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering 4 seconds)	260°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C
DS55494	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

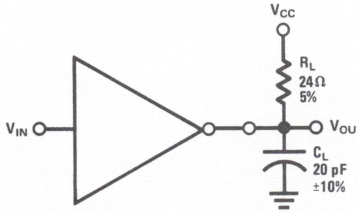
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V, V_{CE} = 8.8V through 100k			2.0	mA
		V_{CC} = Min, V_{IN} = 8.8V, V_{CE} = 8.8V			2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V			−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V, V_{IN} = 8.8V through 100k, V_{CE} = 0V			400	μA
		V_{CC} = Max, V_{OH} = 8.8V, V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k			400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k, DS75494		0.25	0.35	V
		V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k, DS55494		0.25	0.4	V
I_{CC}	Supply Currents	V_{CC} = Max, One Driver "ON", V_{IN} = 8.8V, DS75474			8.0	mA
		V_{CC} = Max, One Driver "ON", V_{IN} = 8.8V, DS55494			10.0	mA
		V_{CC} = Max, All Other Pins to GND, V_{CE} = 6.5V through 1.0k			100	μA
		V_{CC} = Max, All Other Pins to GND, V_{IN} = 8.8V through 100k			100	μA
		V_{CC} = Max, All Other Pins to GND			40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits		0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits		13	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

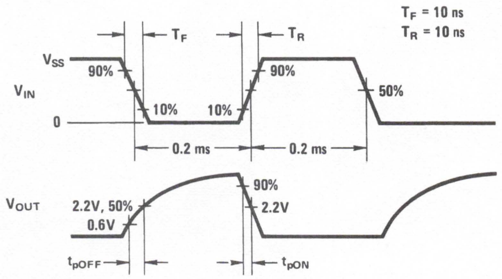
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494 and across the −55°C to +125°C range for the DS55494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



TL/F/5832-3



TL/F/5832-4

National Semiconductor

DS8654 8-Output Display Driver (LED, VF, Thermal Printer)

General Description

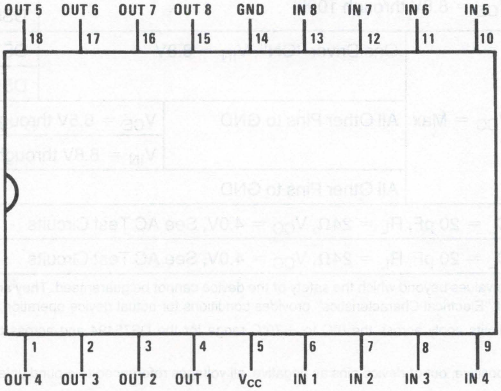
DS8654 is an 8-digit driver with emitter/follower outputs. It can source up to 50 mA at a low impedance, and operates with a constant internal drive current over a wide range of power supply—from 4.5V to 33V. The DS8654 can be used to drive electrical or mechanical, multiplexed or unmultiplexed display systems. It can be used as a segment driver for common cathode displays with external current limiting resistors or can drive incandescent or fluorescent displays directly, both digits (anodes) and segments (grids). It will be necessary to run the device at a lower duty cycle, to keep the maximum package dc power dissipation less than 600 mW while operating all 8 outputs at high supply voltage and large source current. The inputs are MOS compatible and eliminate the need for level shifting since inputs are referenced to the most negative supply of system.

System Description

The DS8654 is specifically designed to operate a thermal printing head for calculator or other uses. In this application the same segment in each digit is selected at the same time, reducing the overall time for a complete print cycle. The DS8654 is an 8-digit driver. With a 15-digit print head, two of the DS8654 are required.

Connection Diagram

Dual-In-Line Package



TL/F/5833-1

Top View

Order Number DS8654N
See NS Package Number N18A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36V
Input Voltage	36V
Output Voltage	$V_{CC} - 36V$
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1563 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 12.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	33	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

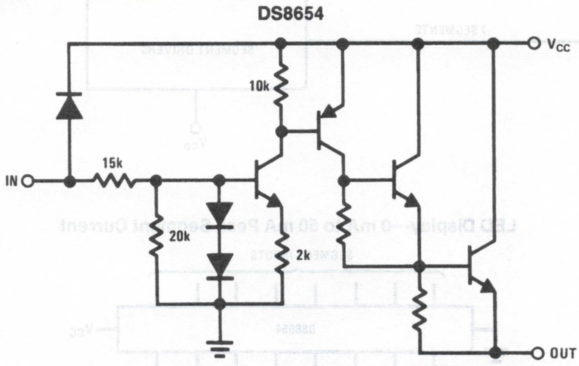
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		390	500	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V		13	40	μA
I_{OFF}	"Off" State Leakage Current	$V_{OUT} = V_{CC} - 33V$		0.01	−100	μA
V_{ON}	"On" State Output Voltage	V_{CC} = Max, I_{IN} = 500 μA, I_{OH} = −50 mA		$V_{CC} - 1.8$	$V_{CC} - 2.5$	V
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, $V_{IN} = V_{OUT}$ = GND		0.01	1.0	mA
$I_{CC(ON)}$	Supply Current (All Outputs "ON")	V_{CC} = Max, V_{IN} = 6.5V, I_{OUT} = 0 mA		7.5	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8654. All typicals are given for V_{CC} = 30V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

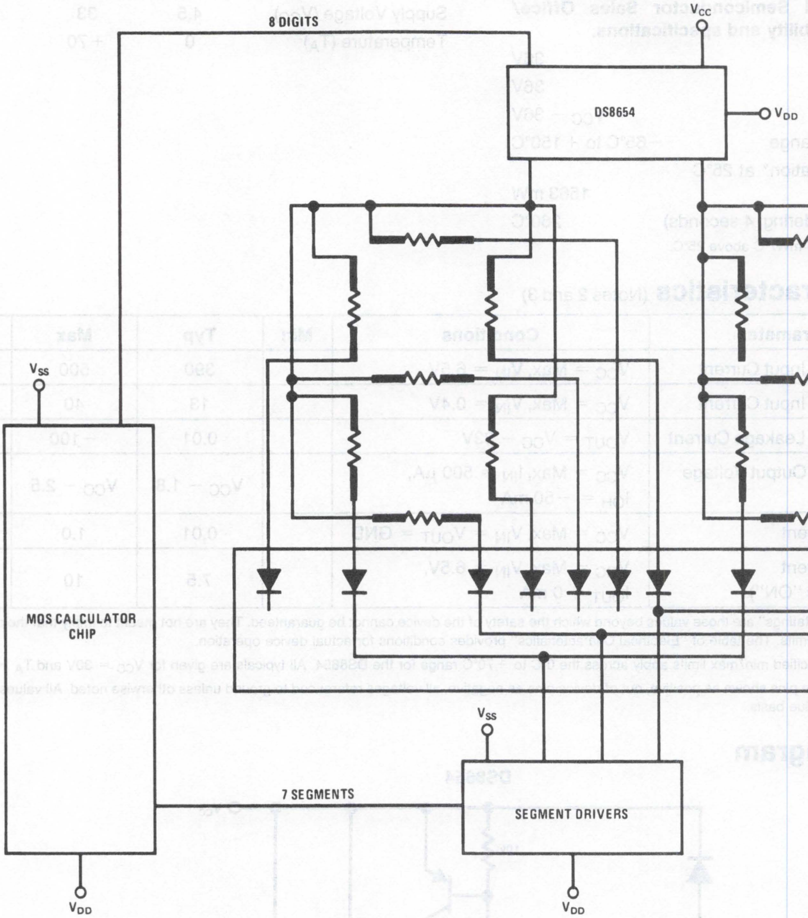
Schematic Diagram



TL/F/5833-2

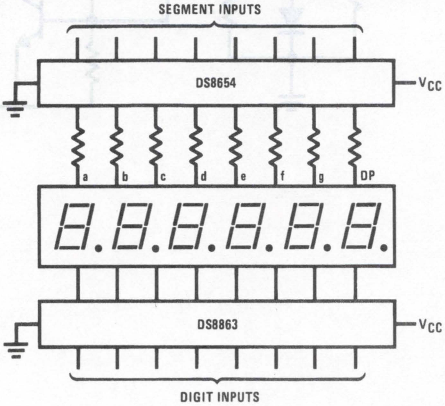
Typical Applications

Thermal Printer


8 DIGITS
V_{CC}
DS8654
V_{DD}
V_{SS}
MOS CALCULATOR CHIP
DS8656
V_{SS}
7 SEGMENTS
SEGMENT DRIVERS
V_{DD}
V_{DD}

TL/F/5833-3

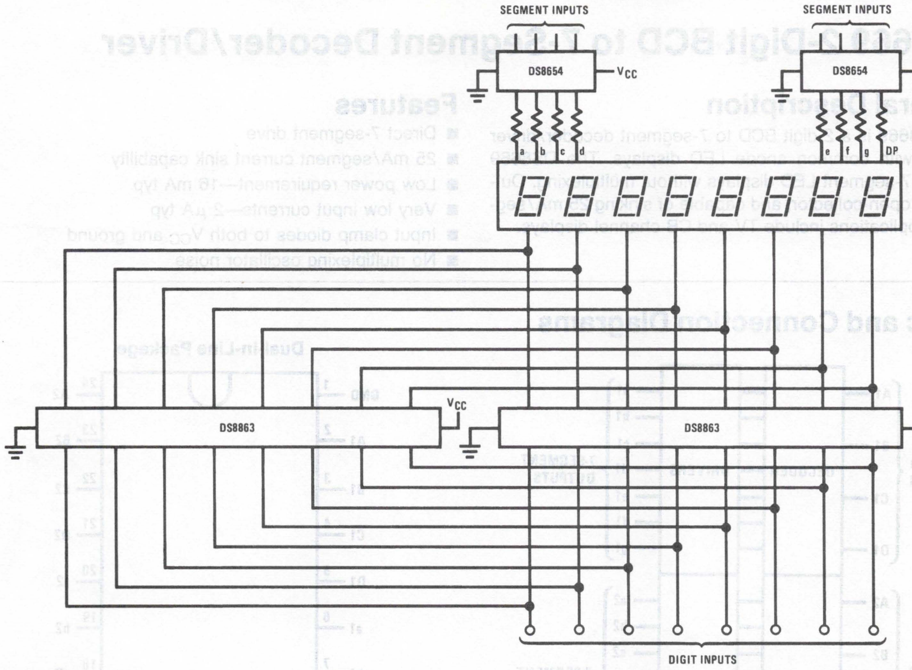
LED Display—0 mA to 50 mA Peak Segment Current


SEGMENT INPUTS
DS8654
V_{CC}
a
b
c
d
e
f
g
DP
DS8863
V_{CC}
DIGIT INPUTS

TL/F/5833-4

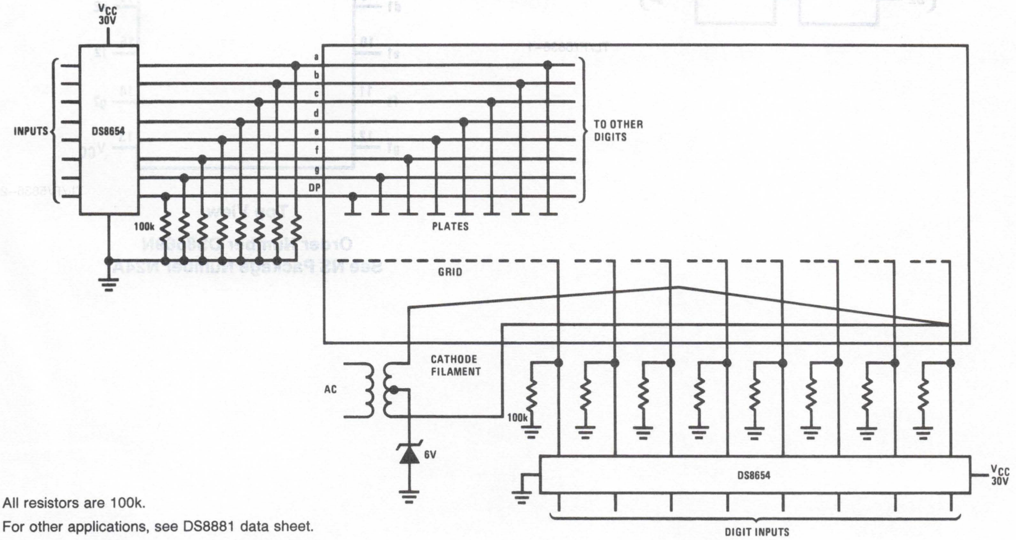
Typical Applications (Continued)

LED Display—50 mA to 100 mA Peak Segment Current


SEGMENT INPUTS
DS8654
V_{CC}
a
b
c
d
SEGMENT INPUTS
DS8654
V_{CC}
e
f
g
DP
DS8863
V_{CC}
DS8863
V_{CC}
DIGIT INPUTS

TL/F/5833-5

VF Display


V_{CC} 30V
INPUTS
DS8654
a
b
c
d
e
f
g
DP
TO OTHER DIGITS
PLATES
100k
GRID
CATHODE FILAMENT
AC
6V
100k
DS8654
V_{CC} 30V
DIGIT INPUTS

All resistors are 100k.

For other applications, see DS8881 data sheet.

TL/F/5833-6

National Semiconductor

DS8669 2-Digit BCD to 7-Segment Decoder/Driver

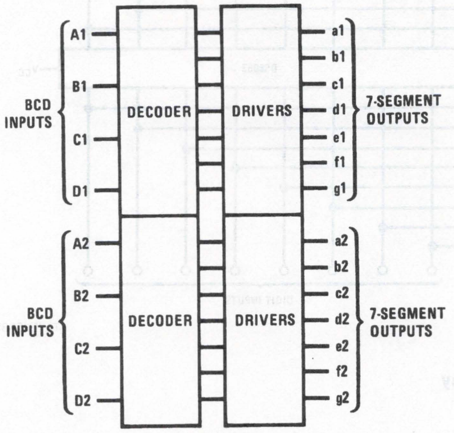
General Description

The DS8669 is a 2-digit BCD to 7-segment decoder/driver for use with common anode LED displays. The DS8669 drives 2 7-segment LED displays without multiplexing. Outputs are open-collector, and capable of sinking 25 mA/segment. Applications include TV and CB channel displays.

Features

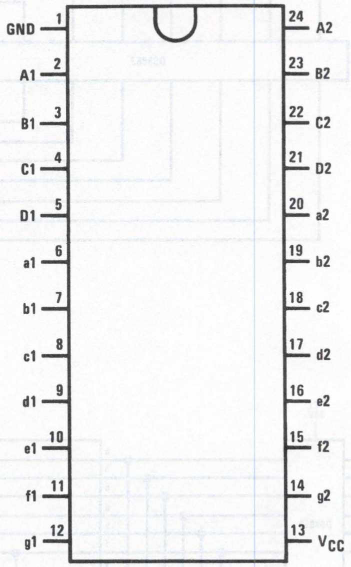
- Direct 7-segment drive
- 25 mA/segment current sink capability
- Low power requirement—16 mA typ
- Very low input currents—2 μA typ
- Input clamp diodes to both V_{CC} and ground
- No multiplexing oscillator noise

Logic and Connection Diagrams


A1
B1
C1
D1
BCD INPUTS
DECODER
DRIVERS
a1
b1
c1
d1
e1
f1
g1
7-SEGMENT OUTPUTS
A2
B2
C2
D2
BCD INPUTS
DECODER
DRIVERS
a2
b2
c2
d2
e2
f2
g2
7-SEGMENT OUTPUTS

TL/F/5836–1

Dual-In-Line Package


GND 1
A1 2
B1 3
C1 4
D1 5
a1 6
b1 7
c1 8
d1 9
e1 10
f1 11
g1 12
24 A2
23 B2
22 C2
21 D2
20 a2
19 b2
18 c2
17 d2
16 e2
15 f2
14 g2
13 VCC

TL/F/5836–2

Top View

Order Number DS8669N
See NS Package Number N24A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Current	20 mA
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	6.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics V_{CC} = 5.25V, (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min	2.0		V_{CC} + 0.6	V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min	−0.3		0.8	V
I_O	Logical "1" Output Leakage Current	V_{CC} = Max, V_{OUT} = 10V			50	µA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 25 mA, V_{CC} = Min		0.4	0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = V_{CC} = Max		2.0	10	µA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V, V_{CC} = Max		−0.1	−10	µA
I_{CC}	Supply Current	All Outputs Low, V_{CC} = Max		16	25	mA
V_{IC}	Input Clamp Voltage	I_{IN} = 10 mA			V_{CC} + 1.5V	V
		I_{IN} = −10 mA			−1.5V	V
t_{pd0}	Propagation Delay to a Logical "0" from Any Input to Any Output	R_L = 400Ω C_L = 50 pF T_A = 25°C			10	µs
t_{pd1}	Propagation Delay to a Logical "1" from Any Input to Any Output				10	µs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8669. All typicals are given for V_{CC} = 5.25V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Table

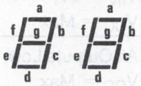
INPUT LEVELS				SEGMENT OUTPUTS															
D_N	C_N	B_N	A_N	a1	b1	c1	d1	e1	f1	g1	a2	b2	c2	d2	e2	f2	g2	DISPLAY 1	DISPLAY 2
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	2	2
0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	3	3
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0	4	4
0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	0	5	5
0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	6	6
0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	7	7
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	8
1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	9	9
1	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	C	H
1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	A	J
1	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	1	P	L
1	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	E	F
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	–	–
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	(Blank)	(Blank)

"0" = Segment ON

"1" = Segment OFF

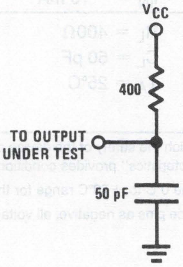
TL/F/5836-3

Display Segment Notation


a
f
g
b
e
c
d
a
f
g
b
e
c
d

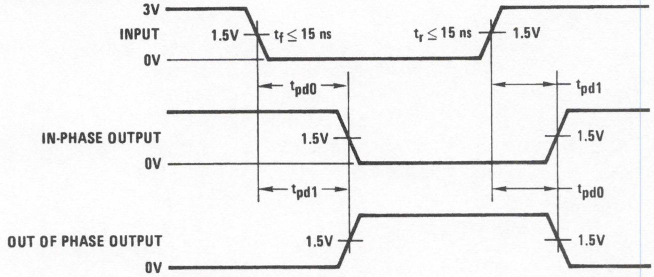
TL/F/5836-4

AC Test Circuit


V_{CC}
400
TO OUTPUT UNDER TEST
50 pF

TL/F/5836-5

Switching Time Waveforms


3V
INPUT
0V
1.5V
$t_f \leq 15$ ns
$t_r \leq 15$ ns
1.5V
t_{pd0}
t_{pd1}
IN-PHASE OUTPUT
0V
1.5V
1.5V
t_{pd1}
t_{pd0}
OUT OF PHASE OUTPUT
0V
1.5V
1.5V

TL/F/5836-6

National Semiconductor

DS8863/DS8963 MOS-to-LED 8-Digit Driver

General Description

The DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

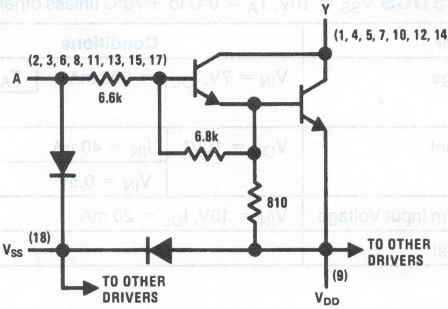
The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

Features

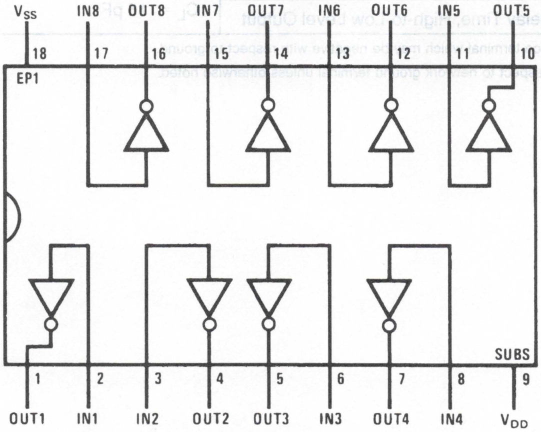
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

Schematic and Connection Diagrams


Y
(1, 4, 5, 7, 10, 12, 14, 16)
(2, 3, 6, 8, 11, 13, 15, 17)
A
6.6k
6.8k
810
(18)
V_{SS}
TO OTHER DRIVERS
TO OTHER DRIVERS
(9)
V_{DD}

TL/F/5839-1

Dual-In-Line Package


V_{SS}
IN8
OUT8
IN7
OUT7
IN6
OUT6
IN5
OUT5
18
17
16
15
14
13
12
11
10
EP1
SUBS
1
2
3
4
5
6
7
8
9
OUT1
IN1
IN2
OUT2
OUT3
IN3
OUT4
IN4
V_{DD}

TL/F/5839-2

Top View

Order Number DS8863N or DS8963N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	DS8863	DS8963
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	18V
Collector (Output)-to-Input Voltage	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)		
Emitter-to-Input Voltage		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	18V

	DS8863	DS8963
Collector (Output) Current		
Each Collector (Output)	500 mA	500 mA
All Collectors (Output)	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	
Maximum Power Dissipation at 25°C Molded Package	1563 mW†	1563 mW†
Lead Temperature (Soldering, 4 sec.)	260°C	260°C

†Derate molded package 12.5 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage	V_{IN} = 7V, I_{OUT} = 500 mA	T_A = 25°C			1.5	V
						1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V*	I_{IN} = 40 µA			250	µA
			V_{IN} = 0.5V			250	µA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA				2	mA
I_{SS}	Current into V_{SS} Terminal					1	mA

*18V for the DS8963

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

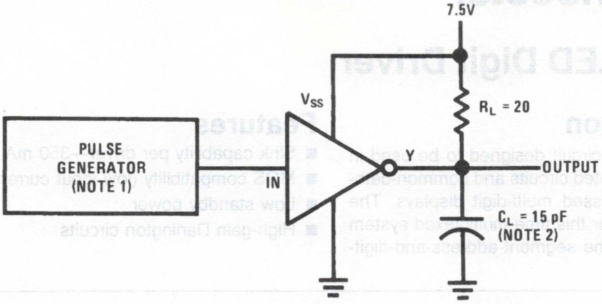
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 8V, R_L = 20Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.

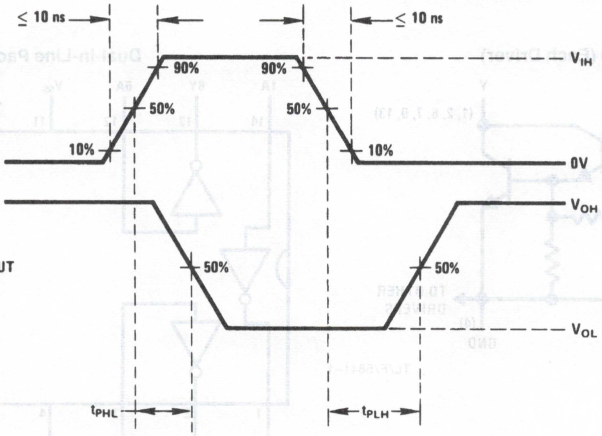
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

AC Test Circuits and Waveforms

DS8863


7.5V
V_{SS}
R_L = 20
PULSE GENERATOR (NOTE 1)
IN
Y
OUTPUT
C_L = 15 pF (NOTE 2)

TL/F/5839-3


≤ 10 ns
≤ 10 ns
90%
90%
50%
50%
10%
10%
INPUT
V_{IH}
0V
V_{OH}
OUTPUT
50%
50%
V_{OL}
t_{PHL}
t_{PLH}

TL/F/5839-4

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS8870 Hex LED Digit Driver

General Description

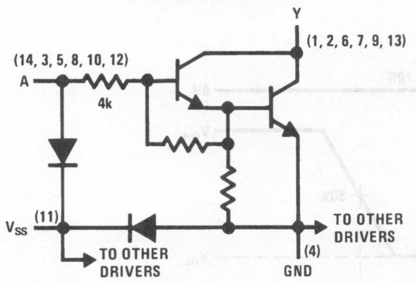
The DS8870 is an interface circuit designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- Sink capability per driver—350 mA
- MOS compatibility (low input current)
- Low standby power
- High-gain Darlington circuits

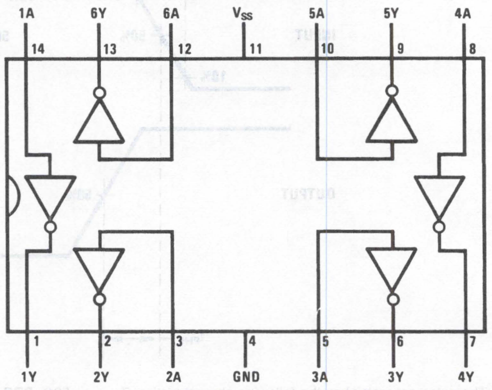
Schematic and Connection Diagrams

DS8870 (Each Driver)


Y
(1, 2, 6, 7, 9, 13)
(14, 3, 5, 8, 10, 12)
A
4k
V_{SS} (11)
TO OTHER DRIVERS
TO OTHER DRIVERS
(4)
GND

TL/F/5841-1

Dual-In-Line Package


1A
6Y
6A
V_{SS}
5A
5Y
4A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
2Y
2A
GND
3A
3Y
4Y

TL/F/5841-2

Order Number DS8870J or DS8870N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage Range (Note 4)	$-5V$ to V_{SS}
Collector Output Voltage	10V
Collector Output to Input Voltage	10V
Voltage at V_{SS} Terminal with Respect to Any Other Device Terminal	10V
Collector Output Current	
Each Collector Output	350 mA
All Collector Outputs	600 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0° to +70°C
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Electrical Characteristics $V_{SS} = 10V$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage	Input = 6.5V through kΩ, $I_{OUT} = 350$ mA, $T_A = 25°C$		1.2	1.4	V
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, $I_{OUT} = 350$ mA			1.6	V
I_{OH}	High Level Output Current	$V_{OH} = 10V$, $I_{IN} = 40\ \mu A$			200	μA
I_{OH}	High Level Output Current	$V_{OH} = 10V$, $V_{IN} = 0.5V$			200	μA
I_I	Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $I_{OL} = 20\ \mu A$		2.2	3.3	mA
I_{SS}	Current into V_{SS} Terminal				1	mA

Switching Characteristics $V_{SS} = 7.5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{IH} = 7.5V$, $R_L = 39\Omega$, $C_L = 15$ pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$V_{IH} = 7.5V$, $R_L = 39\Omega$, $C_L = 15$ pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

National Semiconductor

DS8874 9-Digit Shift Input LED Driver

General Description

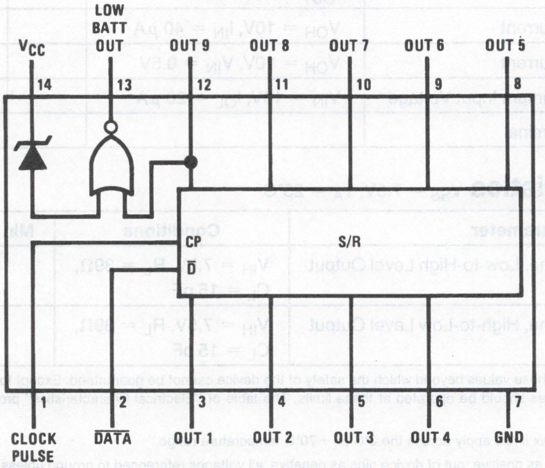
The DS8874 is a 9-digit LED driver which incorporates a shift register input decoding circuit and a low battery indicator. Outputs will sink 110 mA at less than 0.5V drop when sequentially selected. When the V_{CC} supply falls below 6.5V typical, segment current will be furnished at digit 9 time to indicate a low battery condition. Pin 13 is generally connected to the decimal point segment on the display so that when a low battery condition exists, the left-most decimal point lights up.

Features

- 110 mA digit sink
- Low battery indicator
- Minimum number of connections
- MOS compatible inputs

Connection Diagram

Dual-In-Line Package



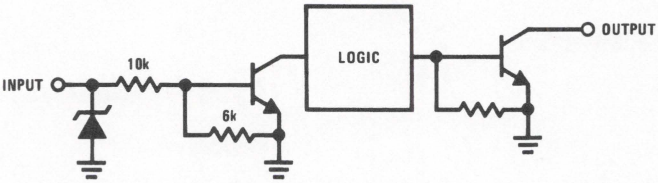
LOW BATT OUT
V_{CC}
OUT 9
OUT 8
OUT 7
OUT 6
OUT 5
14
13
12
11
10
9
8
CP
D
S/R
1
2
3
4
5
6
7
CLOCK PULSE
DATA
OUT 1
OUT 2
OUT 3
OUT 4
GND

TL/F/5843-1

Top View

Order Number DS8874N
See NS Package Number N14A

Equivalent Schematic



INPUT
10k
6k
LOGIC
OUTPUT

TL/F/5843-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	3V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1280 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded package 10.24 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	6.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

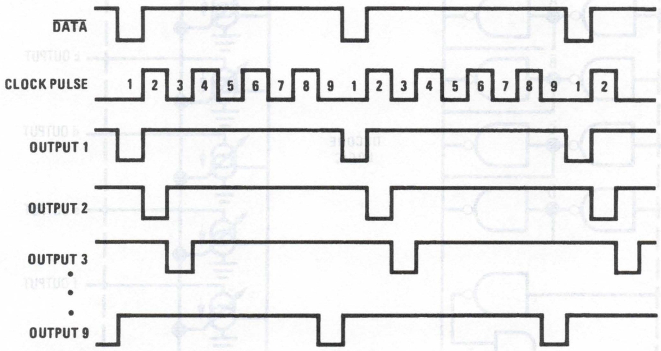
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 3V		0.25	0.4	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.8V		0.05	0.1	mA
V_{CCL}	Decimal Point "ON"	V_{dp} = 2.3V, I_{dp} = −4 mA, O9 = V_{OL}			6.0	V
V_{CCH}	Decimal Point "OFF"	V_{dp} = 1V, I_{dp} = −10 μA, O9 = V_{OL}	7.0			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, Output Not Selected			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, Output Selected, I_{O1} = 80 mA		0.45	1	V
		V_{CC} = Max, Output Selected, I_{O1} = 110 mA		0.6	1.5	V
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Timing Diagram (Upper Level More Positive)



TL/F/5843-4

National Semiconductor

DS7880/DS8880 High Voltage 7-Segment Decoder/Driver

General Description

The DS7880/DS8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the decoder switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

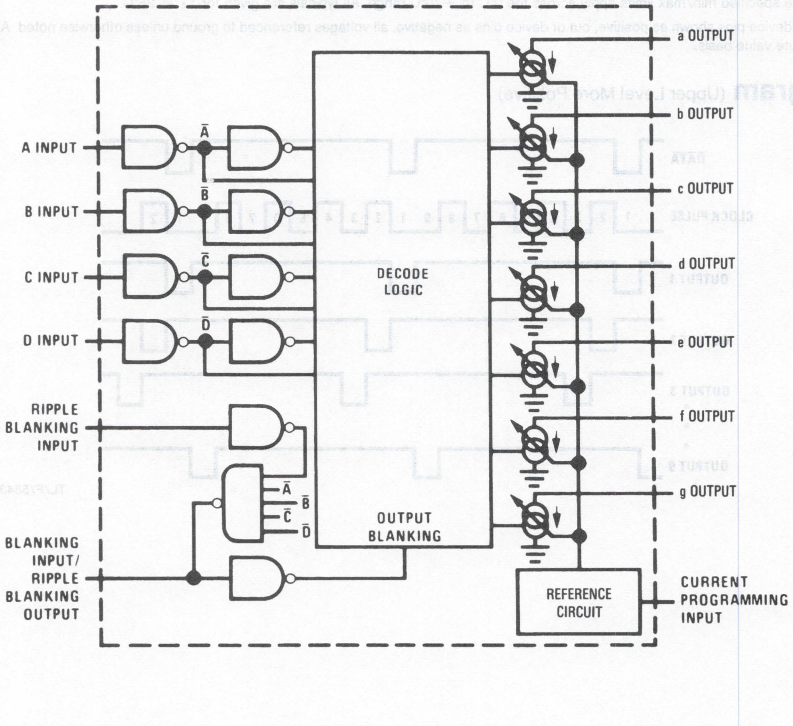
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

Features

- Current sink outputs
- Adjustable output current—0.2 to 1.5 mA
- High output breakdown voltage—110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

Logic Diagram


A INPUT
B INPUT
C INPUT
D INPUT
RIPPLE BLANKING INPUT
BLANKING INPUT/ RIPPLE BLANKING OUTPUT
A̅
B̅
C̅
D̅
DECODE LOGIC
OUTPUT BLANKING
a OUTPUT
b OUTPUT
c OUTPUT
d OUTPUT
e OUTPUT
f OUTPUT
g OUTPUT
REFERENCE CIRCUIT
CURRENT PROGRAMMING INPUT

TL/F/5845–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.06 mW/°C above 25°C; derate molded package 11.81 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7880	4.5	5.5	V
DS8880	4.75	5.25	V
Temperature (T_A)			
DS7880	−55	+125	°C
DS8880	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200 µA, RBO		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 8 mA, RBO			0.13	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI	V_{IN} = 2.4V		2	15	µA
			V_{IN} = 5.5V		4	400	µA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI		−300	−600	µA
			BI		−1.2	−2.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max, R_p = 2.2k, All Inputs = 0V			27	43	mA
V_{CD}	Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C, I_{IN} = 12 mA			−0.9	−1.5	V
I_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, $I_{OUT}b$ = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Outut c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
I_b ON	Output b "ON" Current	V_{CC} = 5V, $V_{OUT}b$ = 50V, All Other Outputs ≥ 5V, T_A = 25°C	R_p = 18.1k	0.15	0.20	0.25	mA
			R_p = 7.03k	0.45	0.50	0.55	mA
			R_p = 3.40k	0.90	1.00	1.10	mA
			R_p = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, R_p = 1k±5%, $I_{OUT}b$ = 2 mA, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, BI = 0V, R_p = 2.2k			0.003	3	µA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250 µA, BI = 0V, R_p = 2.2k		80	110		V
t_{pd}	Propagation Delays BCD Input to Segment Output	V_{CC} = 5V, T_A = 25°C			0.4	10	µs
	BI to Segment Output				0.4	10	µs
	RBI to Segment Output				0.7	10	µs
	RBI to RBO				0.4	10	µs

Note 1: "Absolute Maximum Rating" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7880 and across the 0°C to +70°C range for the DS8880. All typical values are for T_A = 25°C and V_{CC} = 5V.

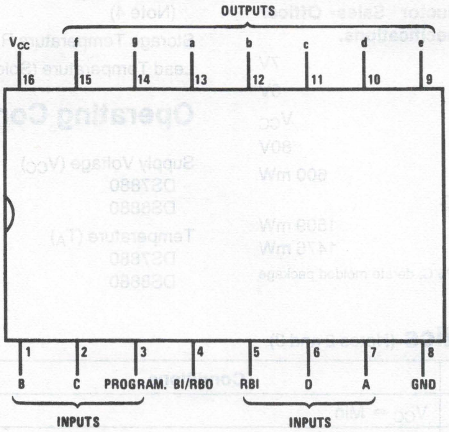
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Connection Diagram

Dual-In-Line Package


OUTPUTS
VCC
g
a
b
c
d
e
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
B
C
PROGRAM.
BI/RBO
RBI
D
A
GND
INPUTS
INPUTS

TL/F/5845-2

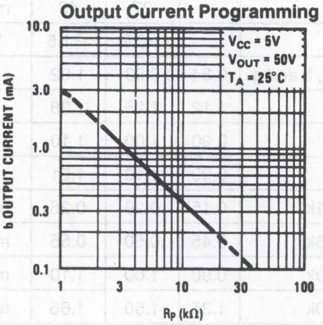
Top View

Order Number DS7880J, DS8880J or DS8880N

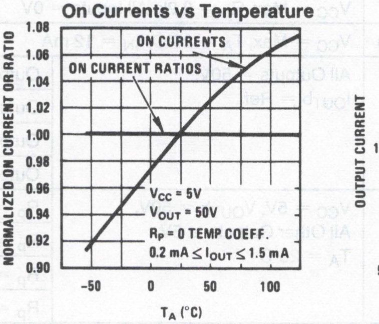
See NS Package Number J16A or N16A

Typical Performance Characteristics

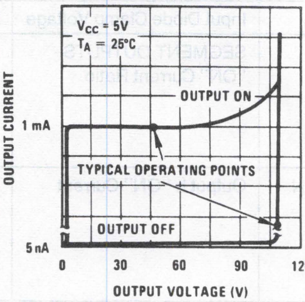
Output Current Programming



On Currents vs Temperature

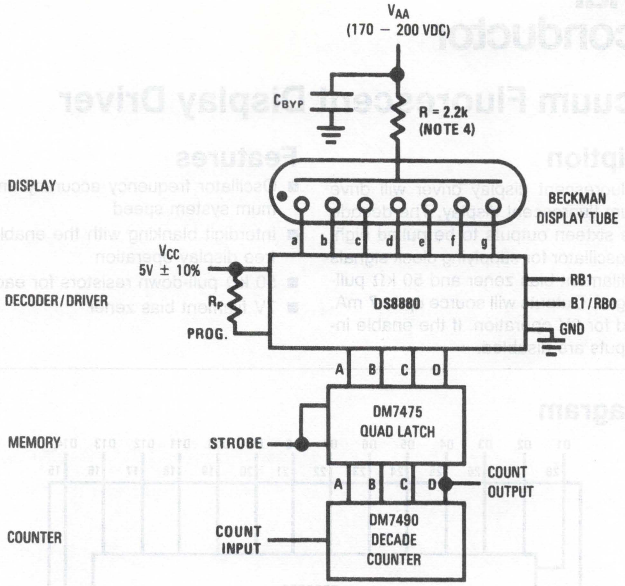


Output Characteristic



TL/F/5845-3

Typical Application


V_{AA} (170 – 200 VDC)
C_{BYP}
R = 2.2k (NOTE 4)
DISPLAY
BECKMAN DISPLAY TUBE
a
b
c
d
e
f
g
V_{CC} 5V ± 10%
R_P
PROG.
DECODER/DRIVER
DS8880
RB1
B1/RBO
GND
A
B
C
D
DM7475 QUAD LATCH
MEMORY
STROBE
A
B
C
D
COUNT OUTPUT
DM7490 DECADE COUNTER
COUNTER
COUNT INPUT

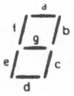
TL/F/5845-4

Truth Table

DECIMAL OR FUNCTION	RBI†	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI*	X	X	X	X	X	0*	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

*BI/RBO used as input only

†X = Don't care



SEGMENT IDENTIFICATION

TL/F/5845-5

National Semiconductor

DS8881 Vacuum Fluorescent Display Driver

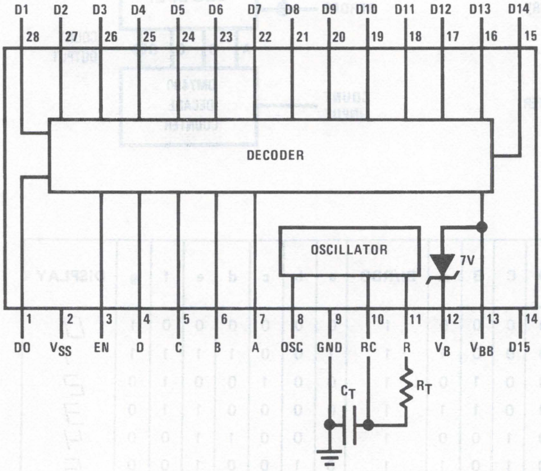
General Description

The DS8881 vacuum fluorescent display driver will drive 16-digit grids of a vacuum fluorescent display. The decode inputs select one of the sixteen outputs to be pulled high. The device contains an oscillator for supplying clock signals to the MOS circuit, the filament bias zener and 50 kΩ pull-down resistors for each grid. Outputs will source up to 7 mA. The DS8881 is designed for 9V operation. If the enable input is pulled low, all outputs are disabled.

Features

- Oscillator frequency accuracy and stability allows maximum system speed
- Interdigit blanking with the enable input provides ghost-free display operation
- 50 kΩ pull-down resistors for each grid
- 7V filament bias zener

Connection Diagram


D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
DECODER
OSCILLATOR
7V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
DO
V_{SS}
EN
D
C
B
A
OSC
GND
RC
R
V_B
V_{BB}
D15
C_T
R_T

TL/F/5846-1

Top View

Order Number DS8881N
See NS Package Number N28B

Truth Table All outputs now shown high are off (low)

Inputs					Digit Outputs															
E_N	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	L	L	L	L	H															
H	L	L	L	H		H														
H	L	L	H	L			H													
H	L	L	H	H				H												
H	L	H	L	L					H											
H	L	H	L	H						H										
H	L	H	H	L							H									
H	L	H	H	H								H								
H	H	L	L	L									H							
H	H	L	L	H										H						
H	H	L	H	L											H					
H	H	L	H	H												H				
H	H	H	L	L													H			
H	H	H	L	H														H		
H	H	H	H	L															H	
H	H	H	H	H																H
L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{SS}-V_{BB}$)	38V
Input Current	10 mA
Output Current	−20 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2168 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded package 17.35 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{SS}	5.0	9.5	V
V_{BB}	Gnd	−26	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{SS} = Max	Enable	I_{IN} = 260 μA				5.1	V
			A, B, C, D	I_{IN} = 1400 μA				1.5	V
I_{IH}	Logical "1" Input Current	V_{SS} = Max	Enable A, B, C, D					260	μA
V_{IL}	Logical "0" Input Voltage	V_{SS} = Max	Enable					1.0	V
			A, B, C, D					0.3	V
I_{IL}	Logical "0" Input Current	V_{SS} = Max	Enable	V_{IN} = 0V				−1.0	μA
			A, B, C, D	$V_{IN} = V_{IL(MAX)}$		25			μA
V_{OH}	Logical "1" Output Voltage	Digit Output, I_{OH} = −7 mA				V_{SS} − 2.5			V
I_{OH}	Logical "1" Output Current	V_{SS} = Max, Osc. Output, V_{RC} = 0.6V, V_{OH} = 10V						50	μA
I_{OS}	Output Short-Circuit Current	V_{SS} = Min, Pin R, V_{RC} = 0.6V, V_R = 0V				−150		−450	μA
R_{OUT}	Output Pull-Down Resistor	V_{SS} = Min, Digit Output				30	50	85	kΩ
V_{OL}	Logical "0" Output Voltage	V_{SS} = Min	Osc	V_{RC} = 1.6V	I_{OL} = 6 mA			0.5	V
			Pin R		I_{OL} = 60 μA			0.2	V
		V_{SS} = Max	Digit Output	V_{ENABLE} = 1V	I_{OL} = 10 μA			V_{BB} + 1.4	V
I_{SS}	Supply Current	V_{SS} = 9.5V, I_{OH} = 0		V_{ENABLE} = 5.1V			9.0	12.5	mA
				V_{ENABLE} = 1V			5.0	9.0	mA
I_{BB}	Supply Current	V_{SS} = 9.5V, I_B = 0, V_{BB} = −26V, I_{IN} = 300 μA (Note 4)		V_{ENABLE} = 1V			−0.8	−1.5	mA
				V_{ENABLE} = 5.1V			−3.0	−5.0	mA
V_B	Filament Bias Voltage	I_B = 10 mA				V_{BB} + 6.4	V_{BB} + 6.9	V_{BB} + 7.4	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

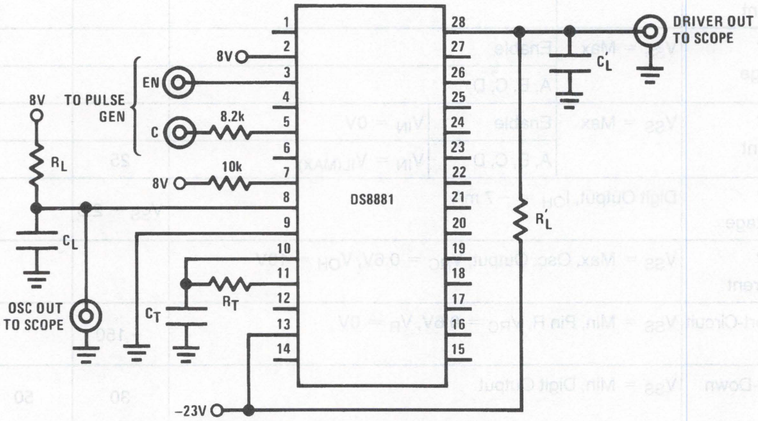
Note 3: All currents into device pins shown as positive, out of device pins as negative, and all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Approximately 50% of input current on pins 4, 5, 6, 7 is shunted to V_{BB}. If minimum I_{BB} is desired, then I_{IN} should be minimized by using resistors in series with the inputs.

Switching Characteristics $T_A = 25°C$ unless otherwise specified

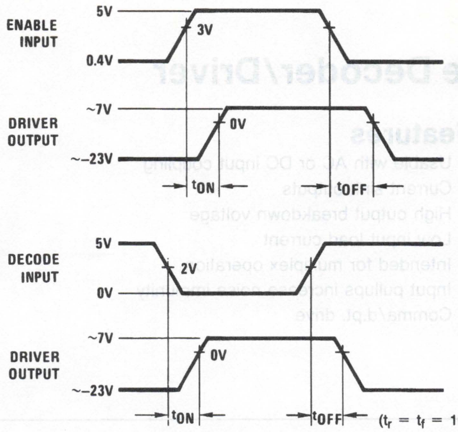
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Enable Input to Digit Output	$R_L = 4.7\ k\Omega$, $C_L = 50\ pF$, $V_{BB} = -23V$, $V_{SS} = 8V$			1	μs
t_{pd0}	Propagation Delay to a Logical "0" A, B, C, D to Digit Output				1	μs
t_{pd1}	Propagation Delay to a Logical "1" from Enable Input to Digit Output				300	ns
t_{pd1}	Propagation Delay to a Logical "1" from A, B, C, D to Digit Output				500	ns
t_{FALL}	Oscillator Output Transition Time from 1 to 0	$V_{SS} = 9.5V$, $R_L = 6k$ to V_{SS}, $C_L = 25\ pF$			50	ns
f_{OSC}	Oscillator Frequency	$7V < V_{SS} < 9.5V$, $R_T = 27\ k\Omega \pm 2\%$, $R_L = 1.3k$, $C_T = 100\ pF$, $\pm 5\%$, $C_L = 50\ pF$	320	360	400	kHz
dc	Oscillator Duty Cycle		46	56	66	%

AC Test Circuit


DRIVER OUT
TO SCOPE
C_L
8V
EN
TO PULSE
GEN
8V
R_L
8.2k
C
10k
8V
DS8881
R_L'
C_L
R_T
C_T
OSC OUT
TO SCOPE
−23V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15

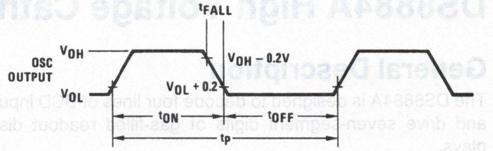
TL/F/5846-2

Switching Time Waveforms



(t_r = t_f = 10 ns from 10% to 90% of input)

TL/F/5846-3

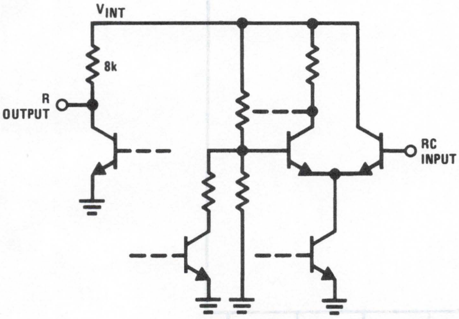


TL/F/5846-4

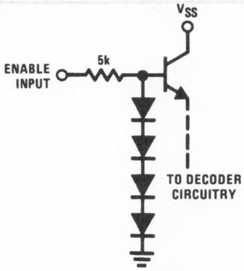
$$\text{Duty Cycle} = \frac{t_{ON}}{t_p}$$

$$\text{Frequency} = \frac{1}{t_p}$$

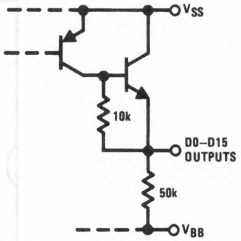
Input-Output Schematics


V_{INT}
8k
R OUTPUT
RC INPUT

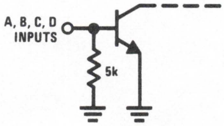
TL/F/5846-5


V_{SS}
ENABLE INPUT
5k
TO DECODER CIRCUITRY

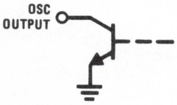
TL/F/5846-6


V_{SS}
10k
D0–D15 OUTPUTS
50k
V_{BB}

TL/F/5846-7


A, B, C, D INPUTS
5k

TL/F/5846-8



TL/F/5846-9

National Semiconductor

DS8884A High Voltage Cathode Decoder/Driver

General Description

The DS8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays.

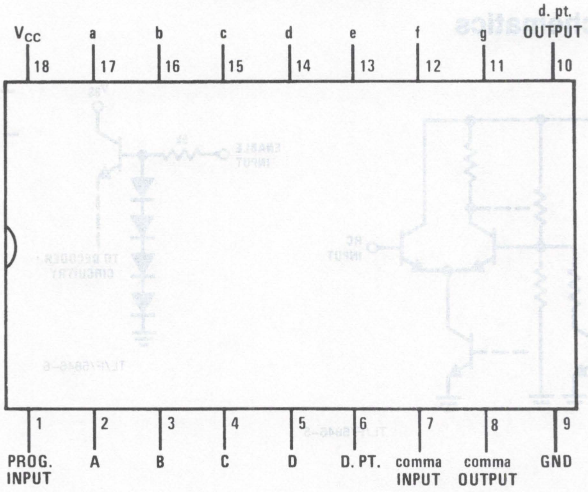
All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 mA to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve. Unused outputs must be tied to V_{CC}.

Features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation
- Input pullups increase noise immunity
- Comma/d.pt. drive

Connection Diagram

Dual-In-Line Package



TL/F/5847-2

Top View

Order Number DS8884AN
See NS Package Number N18A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}	7V
Input Voltage (Note 4)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 5)	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1714 mW

*Derate molded package 13.71 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Logical "1" Input Voltage	$V_{CC} = 4.75V$		2.0		V
V_{IL}	Logical "0" Input Voltage	$V_{CC} = 4.75V$			1.0	V
I_{IH}	Logical "1" Input Current	$V_{CC} = 5.25V, V_{IN} = 2.4V$			15	μA
I_{IL}	Logical "0" Input Current	$V_{CC} = 5.25V, V_{IN} = 0.4V$			−250	μA
I_{CC}	Power Supply Current	$V_{CC} = 5.25V, R_P = 2.8k$, All Inputs = 5V			40	mA
V_{I+}	Positive Input Clamp Voltage	$V_{CC} = 4.75V, I_{IN} = 1$ mA		5.0		V
V_{I-}	Negative Input Clamp Voltage	$V_{CC} = 5V, I_{IN} = -12$ mA, $T_A = 25°C$			−1.5	V
ΔI_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref., All Outputs		0.9	1.1	
$I_{b\ ON}$	Output b "ON" Current	$V_{CC} = 5V, V_{OUT}$ b = 50V, $T_A = 25°C$	$R_P = 18.1k$	0.15	0.25	mA
			$R_P = 7.03k$	0.45	0.55	mA
			$R_P = 3.40k$	0.90	1.10	mA
			$R_P = 2.80k$	1.08	1.32	mA
I_{CEX}	Output Leakage Current	$V_{OUT} = 75V$			5	μA
V_{BR}	Output Breakdown Voltage	$I_{OUT} = 250$ μA		80		V
t_{pd}	Propagation Delay of Any Input to Segment Output	$V_{CC} = 5V, T_A = 25°C$			10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

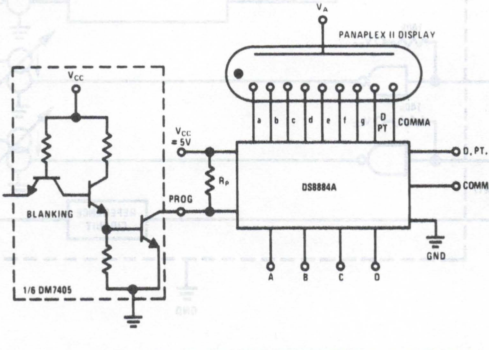
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8884A. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This limit can be higher for a current limiting voltage source.

Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

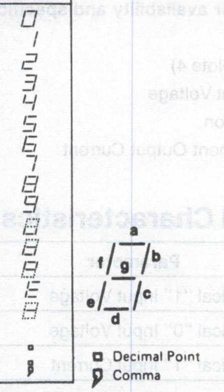
Typical Application



TL/F/5847-4

Truth Table

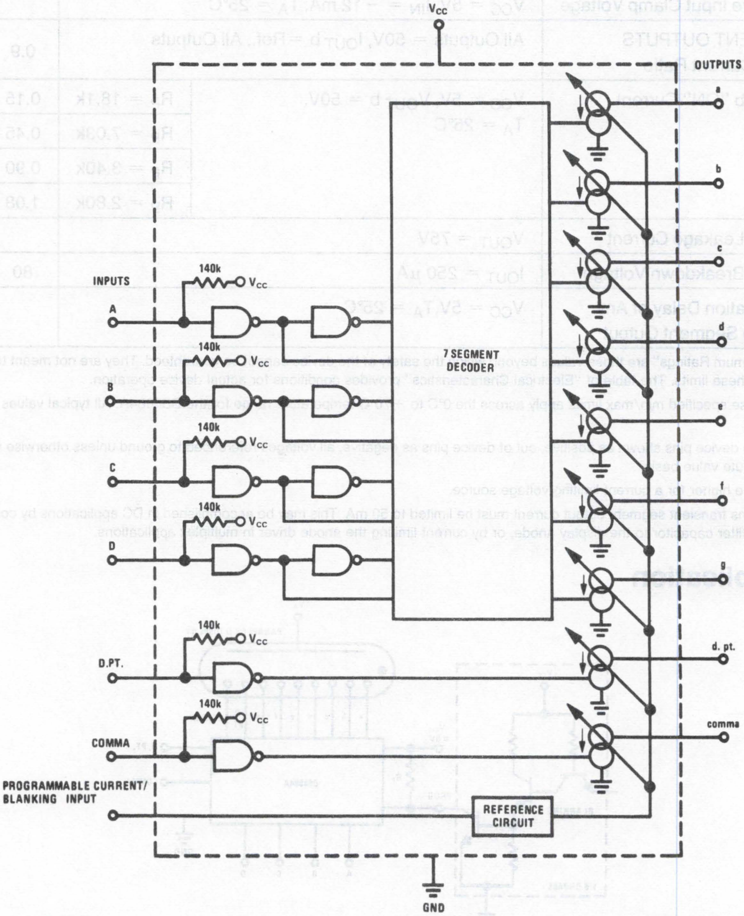
FUNCTION	D.PT.	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	1	1	0	0	1	1	1	1	
2	1	1	0	0	1	0	0	0	1	0	0	1	0	
3	1	1	0	0	1	1	0	0	0	0	1	1	0	
4	1	1	0	1	0	0	1	0	0	1	1	0	0	
5	1	1	0	1	0	1	0	1	0	0	1	0	0	
6	1	1	0	1	1	0	0	1	0	0	0	0	0	
7	1	1	0	1	1	1	0	0	0	1	1	1	1	
8	1	1	1	0	0	0	0	0	0	0	0	0	0	
9	1	1	1	0	0	1	0	0	0	0	1	0	0	
10	1	1	1	0	1	0	1	1	0	0	0	1	1	
11	1	1	1	0	1	1	1	1	0	0	0	1	0	
12	1	1	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	1	1	0	1	0	1	1	0	0	0	0	
14	1	1	1	1	1	0	1	1	1	1	1	1	0	
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D.PT.	0	1	X	X	X	X	X	X	X	X	X	X	X	
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	


a
b
c
d
e
f
g
Decimal Point
Comma

TL/F/5847-3

*Decimal point and comma can be displayed with or without any numeral.

Logic Diagram


V_{CC}
OUTPUTS
a
b
c
d
e
f
g
d. pt.
comma
INPUTS
A
B
C
D
140k
V_{CC}
7 SEGMENT DECODER
D.PT.
COMMA
PROGRAMMABLE CURRENT/ BLANKING INPUT
REFERENCE CIRCUIT
GND

TL/F/5847-1

National Semiconductor

DS8973 9-Digit LED Driver

General Description

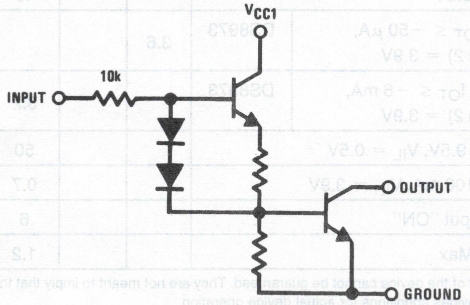
The DS8973 is a 9-digit driver designed to operate from 3-cell battery supplies. Each driver will sink 100 mA to less than 0.7V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a DC-to-DC converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 is designed for the more efficient operating mode.

Features

- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Straight through pin out for easy board layout

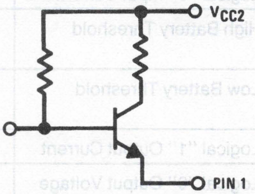
Equivalent Circuit Diagrams

Typical Driver Circuit


V_{CC1}
10k
INPUT
OUTPUT
GROUND

TL/F/5851-1

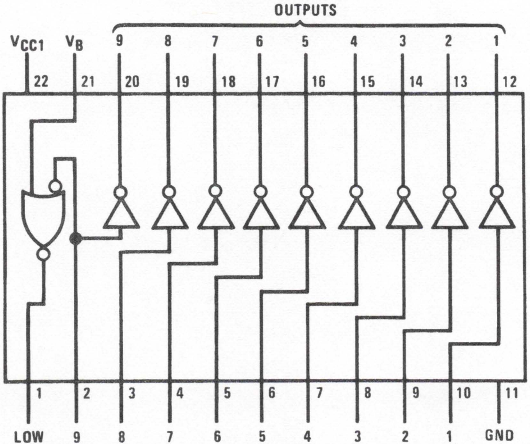
Typical D.P. Out Circuit



TL/F/5851-2

Connection Diagram

Dual-In-Line Package


OUTPUTS
V_{CC1}
V_B
9
8
7
6
5
4
3
2
1
22
21
20
19
18
17
16
15
14
13
12
1
2
3
4
5
6
7
8
9
10
11
LOW VOLT IND
9
8
7
6
5
4
3
2
1
GND
INPUTS

TL/F/5851-3

Top View

Order Number DS8973N
See NS Package Number N22A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1673 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 13.39 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_B)	3.0	5.5	V
Supply Voltage (V_{CC1})	3.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	µA
V_{BH}	High Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50\ \mu A$, T_A = 25°C, V_{IH} (Pin 2) = 3.9V	DS8973	3.6			V
V_{BL}	Low Battery Threshold	V_{OT} (Pin 1) = 2.1V, $I_{OT} \leq -6$ mA, T_A = 25°C, V_{IH} (Pin 2) = 3.9V	DS8973			3.2	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	µA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.7	V
I_{CC1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_B	Pin 21 (High Battery Supply)	V_{CC} = Max, V_B = Max				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Driving 7-Segment Gas Discharge Display Tubes with National Semiconductor Drivers

National Semiconductor
Application Note 84

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays* and Burroughs Panaplex II, is greatly simplified by two monolithic integrated circuits from National Semiconductor. They are: DS8880 high voltage cathode decoder/driver and DS8884A high voltage cathode decoder/driver.

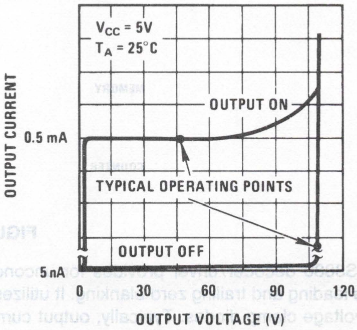
In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, these circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National circuits can drive the displays directly.

Sperry Information Display* and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200 μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3 μA to 5 μA.

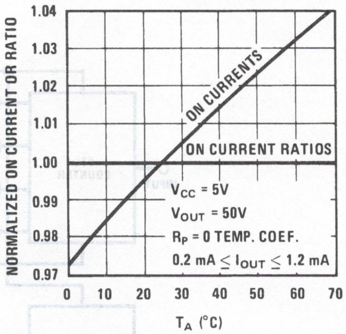
Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3 μA to 5 μA.

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output "on" voltage ranging from 5V to 50V (see *Figure 1*). The following is a brief description of the circuits now offered by National:



TL/F/5871–1

(a) Cathode Driver Output Characteristic



TL/F/5871–2

(b) On Currents vs Temperature

FIGURE 1

DS8880 HIGH VOLTAGE CATHODE DECODER/DRIVER

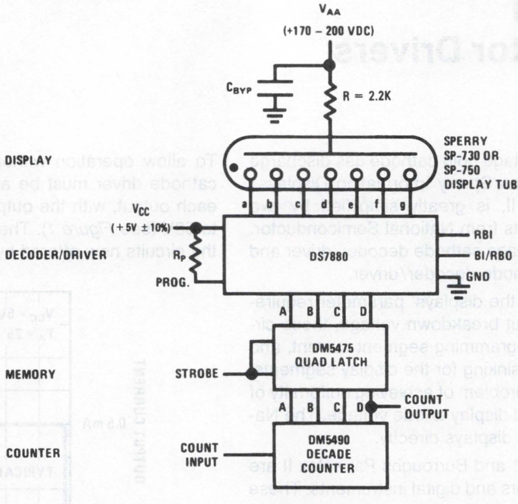
The DS8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

---

*Now called Beckman Displays

APPLICATION

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components *(Figure 2)*. The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.



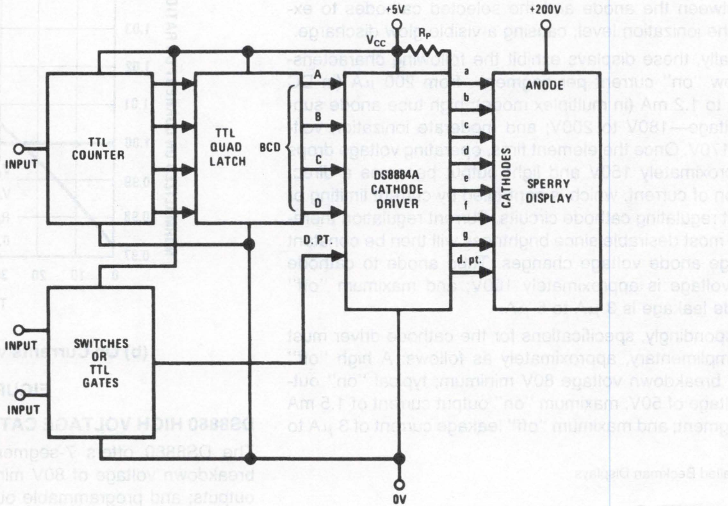
V_{AA}
(+170 – 200 VDC)
C_{BYP}
R = 2.2K
DISPLAY
SPERRY
SP-730 OR
SP-750
DISPLAY TUBE
a b c d e f g
V_{CC}
(+5V ±10%)
R_P
DECODER/DRIVER
PROG.
DS7880
RBI
BI/RBO
GND
A B C D
DM5475
QUAD LATCH
MEMORY
STROBE
A B C D
COUNT
OUTPUT
DM5490
DECADE
COUNTER
COUNTER
COUNT
INPUT

TL/F/5871–3

FIGURE 2. DC Operation From TTL

The DS8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DS7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DS8880 in molded DIP over the industrial range of 0°C to +70°C.



+5V
+200V
V_{CC}
R_P
INPUT
TTL
COUNTER
TTL
QUAD
LATCH
BCD
A
B
C
D
D. PT
DS8884A
CATHODE
DRIVER
ANODE
b
c
e
f
g
d. pt
CATHODES
SPERRY
DISPLAY
INPUT
SWITCHES
OR
TTL
GATES
INPUT
0V

TL/F/5871–4

FIGURE 3. Interfacing Directly With TTL Output

DS8884A HIGH VOLTAGE CATHODE DECODER/DRIVER

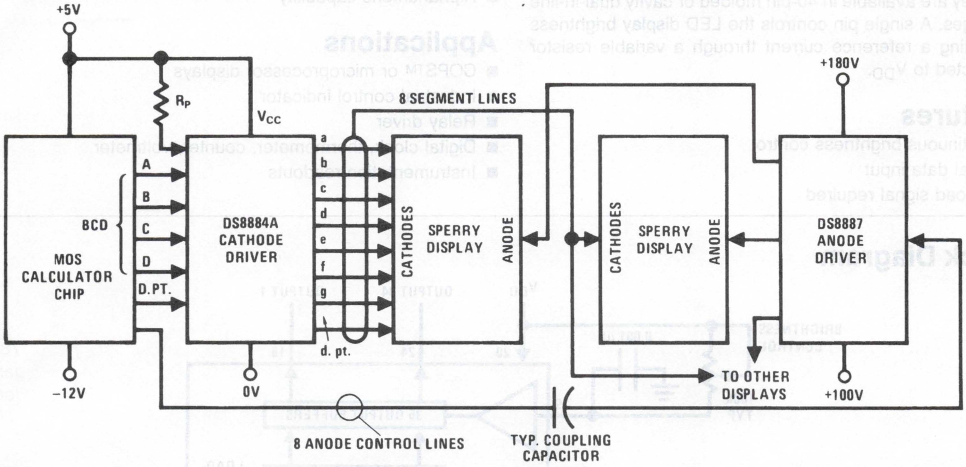
The DS8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

APPLICATION

DS8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL *(Figure 3)* or MOS outputs *(Figure 4)*, or AC-coupled to TTL or MOS outputs *(Figure 5)* using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

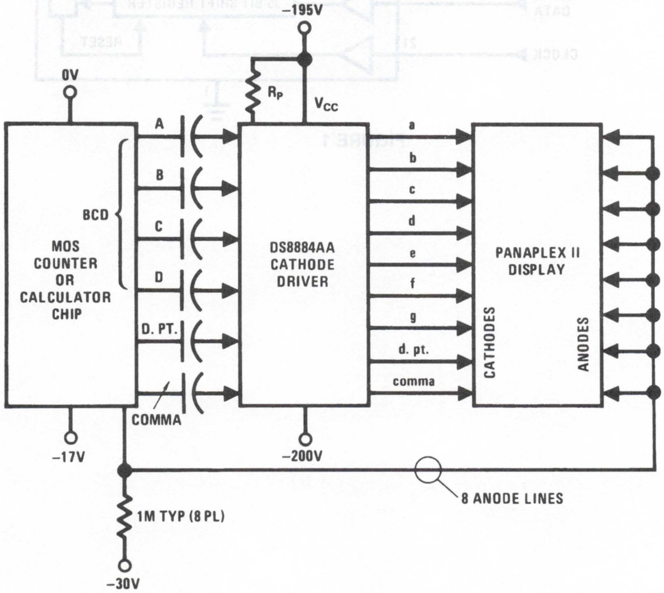
Other advantages of the DS8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DS8884A is guaranteed over the 0°C to +70°C operating temperature range.


+5V
R_P
V_{CC}
8 SEGMENT LINES
+180V
A
B
C
D
D.PT.
BCD
MOS
CALCULATOR
CHIP
DS8884A
CATHODE
DRIVER
a
b
c
d
e
f
g
d. pt.
CATHODES
SPERRY
DISPLAY
ANODE
CATHODES
SPERRY
DISPLAY
ANODE
DS8887
ANODE
DRIVER
−12V
0V
TO OTHER
DISPLAYS
+100V
8 ANODE CONTROL LINES
TYP. COUPLING
CAPACITOR

TL/F/5871-5

FIGURE 4. BCD Data Interfacing Directly With MOS Output


−195V
0V
R_P
V_{CC}
A
B
C
D
D. PT.
COMMA
BCD
MOS
COUNTER
OR
CALCULATOR
CHIP
DS8884AA
CATHODE
DRIVER
a
b
c
d
e
f
g
d. pt.
comma
PANAPLEX II
DISPLAY
CATHODES
ANODES
−17V
−200V
8 ANODE LINES
1M TYP (8 PL)
−30V

TL/F/5871-6

Note: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transistions.

FIGURE 5. Cathode BCD Data AC Coupled From MOS-Output

National Semiconductor

MM5450/MM5451 LED Display Drivers

General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

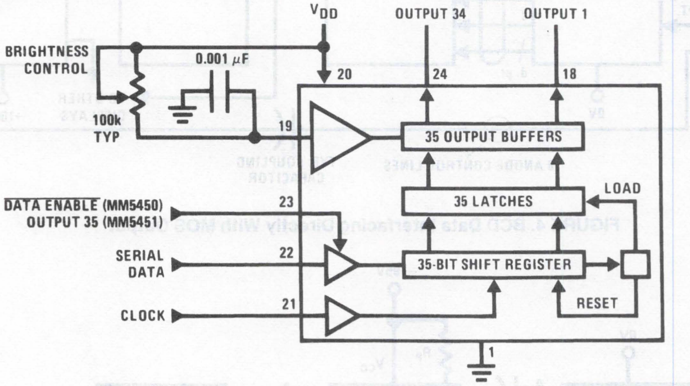
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram


V_{DD}
OUTPUT 34
OUTPUT 1
BRIGHTNESS CONTROL
0.001 μF
20
24
18
100k TYP
19
35 OUTPUT BUFFERS
LOAD
DATA ENABLE (MM5450)
OUTPUT 35 (MM5451)
23
35 LATCHES
SERIAL DATA
22
35-BIT SHIFT REGISTER
CLOCK
21
RESET
1

TL/F/6136-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	560 mW at +85°C 1W at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 4.5V to 11.0V, V_{SS} = 0V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			7	mA
Input Voltages					
Logical "0" Level (V_L)	±10 µA Input Bias	−0.3		0.8	V
Logical "1" Level (V_H)	4.75V ≤ V_{DD} ≤ 5.25V	2.2		V_{DD}	V
	V_{DD} > 5.25V	V_{DD} − 2V		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	V_{OUT} = 3.0V			10	µA
Segment ON	V_{OUT} = 1V (Note 3)	0		15	mA
	Brightness Input = 0 µA	0		10	µA
	Brightness Input = 100 µA	2.0	2.7	4	mA
	Brightness Input = 750 µA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current 750 µA	3.0		4.3	V
Output Matching (Note 1)				±20	%
Clock Input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hole Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See *Figures 5, 6,* and *7* for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

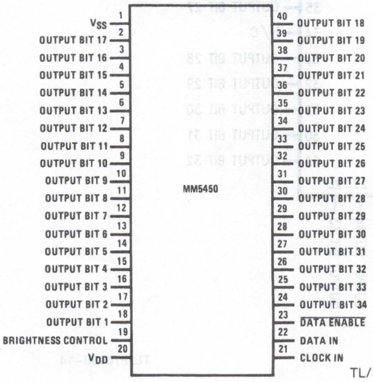
Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package

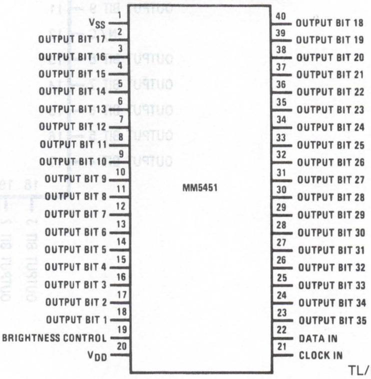

VSS 1
OUTPUT BIT 17 2
OUTPUT BIT 16 3
OUTPUT BIT 15 4
OUTPUT BIT 14 5
OUTPUT BIT 13 6
OUTPUT BIT 12 7
OUTPUT BIT 11 8
OUTPUT BIT 10 9
OUTPUT BIT 9 10
OUTPUT BIT 8 11
OUTPUT BIT 7 12
OUTPUT BIT 6 13
OUTPUT BIT 5 14
OUTPUT BIT 4 15
OUTPUT BIT 3 16
OUTPUT BIT 2 17
OUTPUT BIT 1 18
BRIGHTNESS CONTROL 19
VDD 20
MM5450
40 OUTPUT BIT 18
39 OUTPUT BIT 19
38 OUTPUT BIT 20
37 OUTPUT BIT 21
36 OUTPUT BIT 22
35 OUTPUT BIT 23
34 OUTPUT BIT 24
33 OUTPUT BIT 25
32 OUTPUT BIT 26
31 OUTPUT BIT 27
30 OUTPUT BIT 28
29 OUTPUT BIT 29
28 OUTPUT BIT 30
27 OUTPUT BIT 31
26 OUTPUT BIT 32
25 OUTPUT BIT 33
24 OUTPUT BIT 34
23 DATA ENABLE
22 DATA IN
21 CLOCK IN

TL/F/6136–2

Top View

FIGURE 2a

Dual-In-Line Package


VSS 1
OUTPUT BIT 17 2
OUTPUT BIT 16 3
OUTPUT BIT 15 4
OUTPUT BIT 14 5
OUTPUT BIT 13 6
OUTPUT BIT 12 7
OUTPUT BIT 11 8
OUTPUT BIT 10 9
OUTPUT BIT 9 10
OUTPUT BIT 8 11
OUTPUT BIT 7 12
OUTPUT BIT 6 13
OUTPUT BIT 5 14
OUTPUT BIT 4 15
OUTPUT BIT 3 16
OUTPUT BIT 2 17
OUTPUT BIT 1 18
BRIGHTNESS CONTROL 19
VDD 20
MM5451
40 OUTPUT BIT 18
39 OUTPUT BIT 19
38 OUTPUT BIT 20
37 OUTPUT BIT 21
36 OUTPUT BIT 22
35 OUTPUT BIT 23
34 OUTPUT BIT 24
33 OUTPUT BIT 25
32 OUTPUT BIT 26
31 OUTPUT BIT 27
30 OUTPUT BIT 28
29 OUTPUT BIT 29
28 OUTPUT BIT 30
27 OUTPUT BIT 31
26 OUTPUT BIT 32
25 OUTPUT BIT 33
24 OUTPUT BIT 34
23 OUTPUT BIT 35
22 DATA IN
21 CLOCK IN

TL/F/6136–3

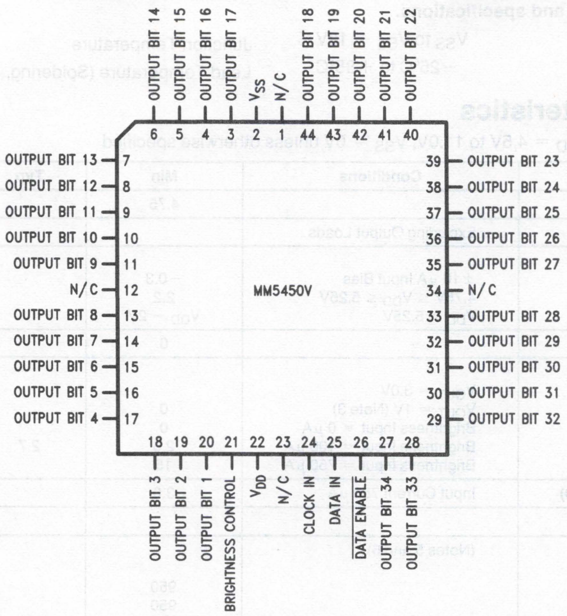
Top View

FIGURE 2b

Order Number MM5450N, MM5451N, MM5450V or MM5451V
See NS Package Number N40A or V44A

Connection Diagrams (Continued)

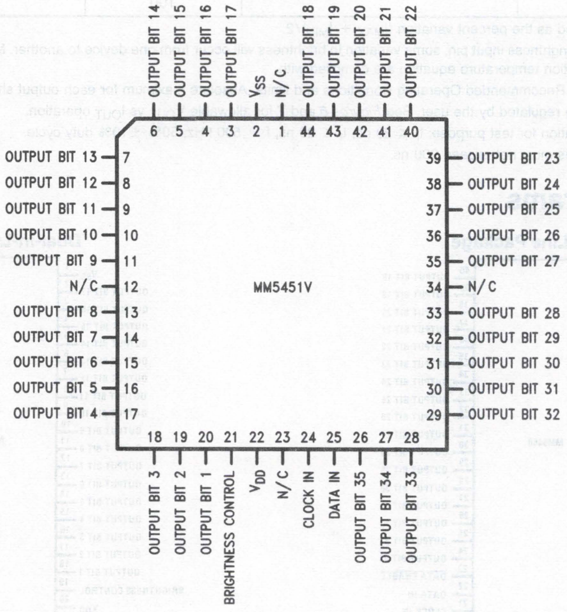
Plastic Chip Carrier


OUTPUT BIT 14
OUTPUT BIT 15
OUTPUT BIT 16
OUTPUT BIT 17
V_{SS}
N/C
OUTPUT BIT 18
OUTPUT BIT 19
OUTPUT BIT 20
OUTPUT BIT 21
OUTPUT BIT 22
6
5
4
3
2
1
44
43
42
41
40
OUTPUT BIT 13 7
OUTPUT BIT 12 8
OUTPUT BIT 11 9
OUTPUT BIT 10 10
OUTPUT BIT 9 11
N/C 12
OUTPUT BIT 8 13
OUTPUT BIT 7 14
OUTPUT BIT 6 15
OUTPUT BIT 5 16
OUTPUT BIT 4 17
MM5450V
39 OUTPUT BIT 23
38 OUTPUT BIT 24
37 OUTPUT BIT 25
36 OUTPUT BIT 26
35 OUTPUT BIT 27
34 N/C
33 OUTPUT BIT 28
32 OUTPUT BIT 29
31 OUTPUT BIT 30
30 OUTPUT BIT 31
29 OUTPUT BIT 32
18
19
20
21
22
23
24
25
26
27
28
OUTPUT BIT 3
OUTPUT BIT 2
OUTPUT BIT 1
BRIGHTNESS CONTROL
V_{DD}
N/C
CLOCK IN
DATA IN
$\overline{\text{DATA ENABLE}}$
OUTPUT BIT 34
OUTPUT BIT 33

TL/F/6136-13

Top View

Plastic Chip Carrier


OUTPUT BIT 14
OUTPUT BIT 15
OUTPUT BIT 16
OUTPUT BIT 17
V_{SS}
N/C
OUTPUT BIT 18
OUTPUT BIT 19
OUTPUT BIT 20
OUTPUT BIT 21
OUTPUT BIT 22
6
5
4
3
2
1
44
43
42
41
40
OUTPUT BIT 13 7
OUTPUT BIT 12 8
OUTPUT BIT 11 9
OUTPUT BIT 10 10
OUTPUT BIT 9 11
N/C 12
OUTPUT BIT 8 13
OUTPUT BIT 7 14
OUTPUT BIT 6 15
OUTPUT BIT 5 16
OUTPUT BIT 4 17
MM5451V
39 OUTPUT BIT 23
38 OUTPUT BIT 24
37 OUTPUT BIT 25
36 OUTPUT BIT 26
35 OUTPUT BIT 27
34 N/C
33 OUTPUT BIT 28
32 OUTPUT BIT 29
31 OUTPUT BIT 30
30 OUTPUT BIT 31
29 OUTPUT BIT 32
18
19
20
21
22
23
24
25
26
27
28
OUTPUT BIT 3
OUTPUT BIT 2
OUTPUT BIT 1
BRIGHTNESS CONTROL
V_{DD}
N/C
CLOCK IN
DATA IN
OUTPUT BIT 35
OUTPUT BIT 34
OUTPUT BIT 33

TL/F/6136-14

Top View

Functional Description

Both the MM5450 and the MM5451 are specifically designed to operate 4- or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in *Figure 1.* For the MM5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the MM5450. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 2 shows the pin-out of the MM5450 and MM5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(124^\circ\text{C/W}) + T_A$$

where:

T_j = junction temperature + 150°C max

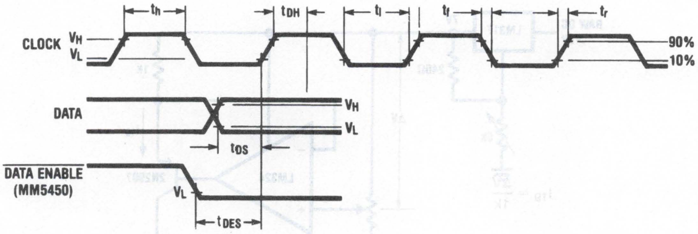
V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_A = ambient temperature

The above equation was used to plot *Figure 5, Figure 6* and *Figure 7.*



TL/F/6136-4

FIGURE 3

Functional Description (Continued)

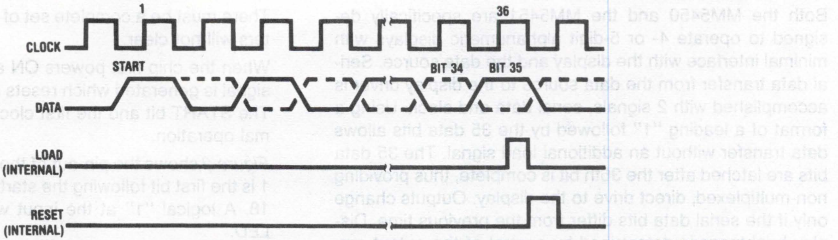

1
36
CLOCK
START
BIT 34
BIT 35
DATA
LOAD (INTERNAL)
RESET (INTERNAL)

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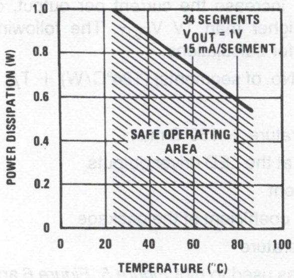
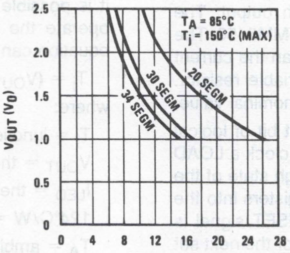
FIGURE 4. Input Data Format

Typical Performance Characteristics



TL/F/6136-6

FIGURE 5



TL/F/6136-7

FIGURE 6

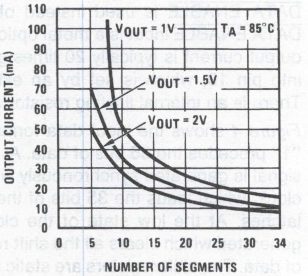


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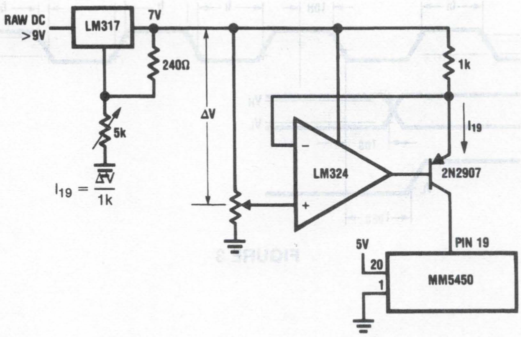
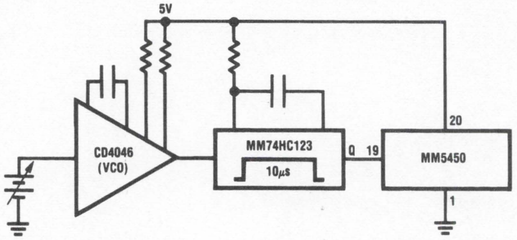
FIGURE 7

Typical Applications


RAW DC >9V
LM317
7V
240Ω
5k
$I_{19} = \frac{\Delta V}{1k}$
ΔV
1k
I_{19}
−
+
LM324
2N2907
5V
PIN 19
20
1
MM5450

TL/F/6136-9

FIGURE 8. Typical Application of Constant Current Brightness Control

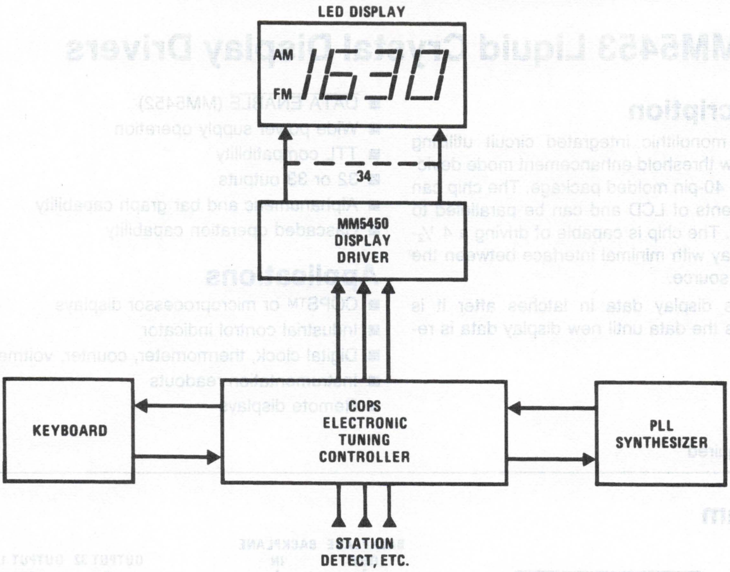

5V
CD4046 (VCO)
MM74HC123
10μs
Q
19
20
MM5450
1

TL/F/6136-10

FIGURE 9. Brightness Control Varying the Duty Cycle

Typical Applications (Continued)

Basic Electronically Tuned Radio System


LED DISPLAY
AM
FM
1630
34
MM5450
DISPLAY
DRIVER
KEYBOARD
COPS
ELECTRONIC
TUNING
CONTROLLER
PLL
SYNTHESIZER
STATION
DETECT, ETC.

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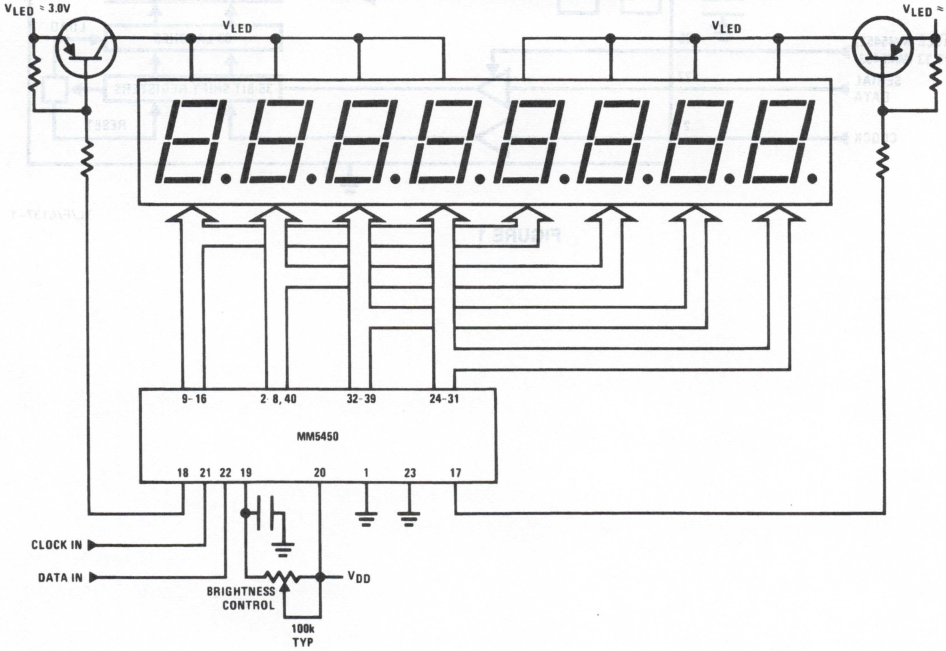
Duplexing 8 Digits with One MM5450


$V_{LED} \approx 3.0V$
V_{LED}
V_{LED}
$V_{LED} \approx 3.0V$
9-16
2-8, 40
32-39
24-31
MM5450
18
21
22
19
20
1
23
17
CLOCK IN
DATA IN
BRIGHTNESS
CONTROL
V_{DD}
100k
TYP

TL/F/6136-12

National Semiconductor

MM5452/MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 ½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

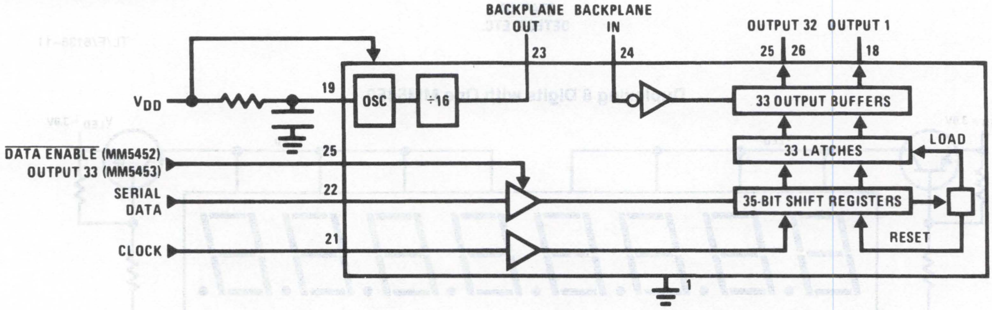
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram


BACKPLANE OUT
BACKPLANE IN
OUTPUT 32
OUTPUT 1
23
24
25
26
18
19
VDD
OSC
÷16
33 OUTPUT BUFFERS
33 LATCHES
LOAD
DATA ENABLE (MM5452)
OUTPUT 33 (MM5453)
25
SERIAL DATA
22
35-BIT SHIFT REGISTERS
RESET
CLOCK
21
1

TL/F/6137-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +70°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs				
	OSC = V_{SS}, BP IN @ 32 Hz			40	µA
	V_{DD} = 5V, Open Outputs, No Clock			10	µA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	$V_{DD} < 4.75$	−0.3		0.1 V_{DD}	V
	$V_{DD} \geq 4.75$	−0.3		0.8	V
Logical '1' Level	$V_{DD} > 5.25$	0.8 V_{DD}		V_{DD}	V
	$V_{DD} \leq 5.25$	2.0		V_{DD}	V
Output Current Levels					
Segments					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−20	µA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	20			µA
Backplane					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−320	µA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	320			µA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF (Note 1)			±50	mV
Clock Input Frequency, f_C	(Notes 2 and 3)			500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input Set-Up Time, t_{DES}		100			ns

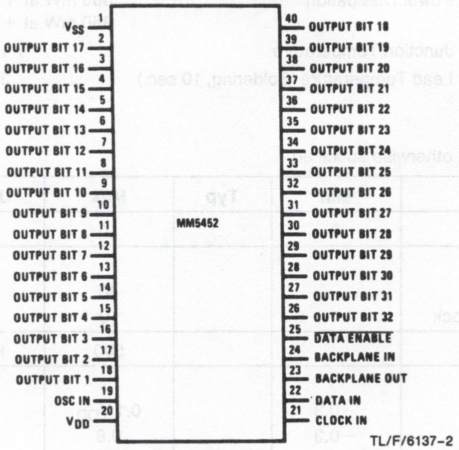
Note 1: This parameter is guaranteed (not 100% production tested) over operating temperature and supply voltage ranges. Not to be used in Q.A. testing.

Note 2: AC input waveform for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package



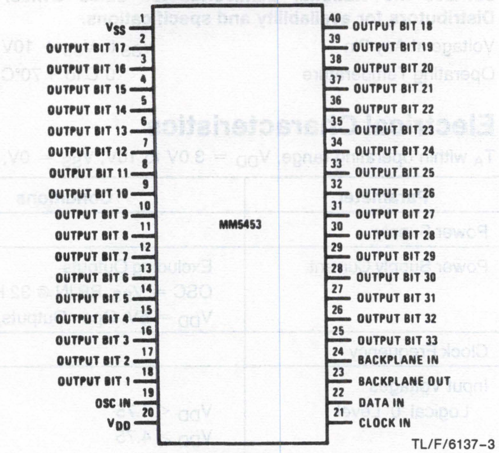
V_{SS} 1
OUTPUT BIT 17 2
OUTPUT BIT 16 3
OUTPUT BIT 15 4
OUTPUT BIT 14 5
OUTPUT BIT 13 6
OUTPUT BIT 12 7
OUTPUT BIT 11 8
OUTPUT BIT 10 9
OUTPUT BIT 9 10
OUTPUT BIT 8 11
OUTPUT BIT 7 12
OUTPUT BIT 6 13
OUTPUT BIT 5 14
OUTPUT BIT 4 15
OUTPUT BIT 3 16
OUTPUT BIT 2 17
OUTPUT BIT 1 18
OSC IN 19
V_{DD} 20
MM5452
40 OUTPUT BIT 18
39 OUTPUT BIT 19
38 OUTPUT BIT 20
37 OUTPUT BIT 21
36 OUTPUT BIT 22
35 OUTPUT BIT 23
34 OUTPUT BIT 24
33 OUTPUT BIT 25
32 OUTPUT BIT 26
31 OUTPUT BIT 27
30 OUTPUT BIT 28
29 OUTPUT BIT 29
28 OUTPUT BIT 30
27 OUTPUT BIT 31
26 OUTPUT BIT 32
25 $\overline{\text{DATA ENABLE}}$
24 BACKPLANE IN
23 BACKPLANE OUT
22 DATA IN
21 CLOCK IN

TL/F/6137-2

Top View

FIGURE 2a

Dual-In-Line Package



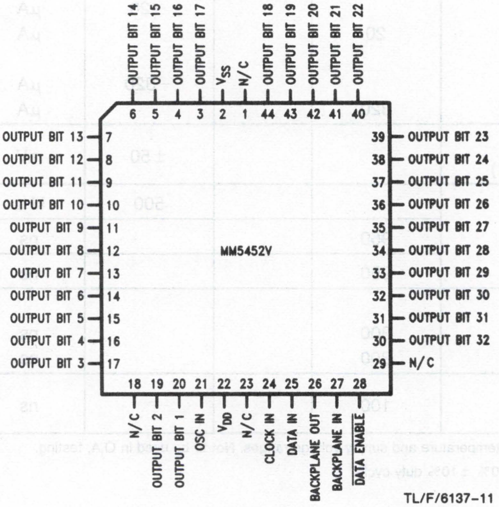
V_{SS} 1
OUTPUT BIT 17 2
OUTPUT BIT 16 3
OUTPUT BIT 15 4
OUTPUT BIT 14 5
OUTPUT BIT 13 6
OUTPUT BIT 12 7
OUTPUT BIT 11 8
OUTPUT BIT 10 9
OUTPUT BIT 9 10
OUTPUT BIT 8 11
OUTPUT BIT 7 12
OUTPUT BIT 6 13
OUTPUT BIT 5 14
OUTPUT BIT 4 15
OUTPUT BIT 3 16
OUTPUT BIT 2 17
OUTPUT BIT 1 18
OSC IN 19
V_{DD} 20
MM5453
40 OUTPUT BIT 18
39 OUTPUT BIT 19
38 OUTPUT BIT 20
37 OUTPUT BIT 21
36 OUTPUT BIT 22
35 OUTPUT BIT 23
34 OUTPUT BIT 24
33 OUTPUT BIT 25
32 OUTPUT BIT 26
31 OUTPUT BIT 27
30 OUTPUT BIT 28
29 OUTPUT BIT 29
28 OUTPUT BIT 30
27 OUTPUT BIT 31
26 OUTPUT BIT 32
25 OUTPUT BIT 33
24 BACKPLANE IN
23 BACKPLANE OUT
22 DATA IN
21 CLOCK IN

TL/F/6137-3

Top View

FIGURE 2b

Plastic Chip Carrier

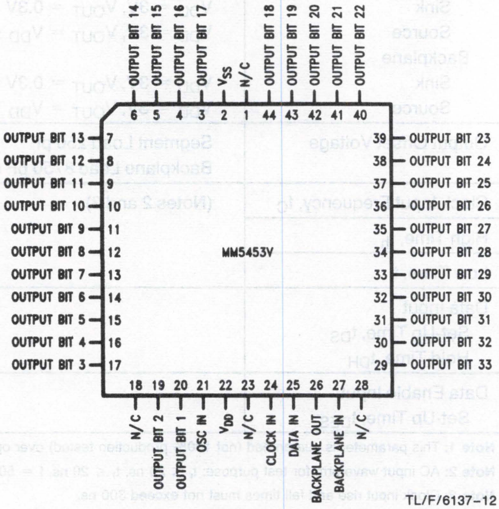


OUTPUT BIT 14 6
OUTPUT BIT 15 5
OUTPUT BIT 16 4
OUTPUT BIT 17 3
V_{SS} 2
N/C 1
OUTPUT BIT 18 44
OUTPUT BIT 19 43
OUTPUT BIT 20 42
OUTPUT BIT 21 41
OUTPUT BIT 22 40
OUTPUT BIT 13 7
OUTPUT BIT 12 8
OUTPUT BIT 11 9
OUTPUT BIT 10 10
OUTPUT BIT 9 11
OUTPUT BIT 8 12
OUTPUT BIT 7 13
OUTPUT BIT 6 14
OUTPUT BIT 5 15
OUTPUT BIT 4 16
OUTPUT BIT 3 17
MM5452V
39 OUTPUT BIT 23
38 OUTPUT BIT 24
37 OUTPUT BIT 25
36 OUTPUT BIT 26
35 OUTPUT BIT 27
34 OUTPUT BIT 28
33 OUTPUT BIT 29
32 OUTPUT BIT 30
31 OUTPUT BIT 31
30 OUTPUT BIT 32
29 N/C
18 N/C
19 OUTPUT BIT 2
20 OUTPUT BIT 1
21 OSC IN
22 V_{DD}
23 N/C
24 CLOCK IN
25 DATA IN
26 BACKPLANE OUT
27 BACKPLANE IN
28 $\overline{\text{DATA ENABLE}}$

TL/F/6137-11

Top View

Plastic Chip Carrier



OUTPUT BIT 14 6
OUTPUT BIT 15 5
OUTPUT BIT 16 4
OUTPUT BIT 17 3
V_{SS} 2
N/C 1
OUTPUT BIT 18 44
OUTPUT BIT 19 43
OUTPUT BIT 20 42
OUTPUT BIT 21 41
OUTPUT BIT 22 40
OUTPUT BIT 13 7
OUTPUT BIT 12 8
OUTPUT BIT 11 9
OUTPUT BIT 10 10
OUTPUT BIT 9 11
OUTPUT BIT 8 12
OUTPUT BIT 7 13
OUTPUT BIT 6 14
OUTPUT BIT 5 15
OUTPUT BIT 4 16
OUTPUT BIT 3 17
MM5453V
39 OUTPUT BIT 23
38 OUTPUT BIT 24
37 OUTPUT BIT 25
36 OUTPUT BIT 26
35 OUTPUT BIT 27
34 OUTPUT BIT 28
33 OUTPUT BIT 29
32 OUTPUT BIT 30
31 OUTPUT BIT 31
30 OUTPUT BIT 32
29 OUTPUT BIT 33
18 N/C
19 OUTPUT BIT 2
20 OUTPUT BIT 1
21 OSC IN
22 V_{DD}
23 N/C
24 CLOCK IN
25 DATA IN
26 BACKPLANE OUT
27 BACKPLANE IN
28 N/C

TL/F/6137-12

Top View

Order Number MM5452N, MM5453N,
MM5452V or MM5453V
See NS Package Number N40A or V44A

Functional Description

The MM5452 is specifically designed to operate 4 ½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1.* For the MM5452 a $\overline{\text{DATA ENABLE}}$ is used instead of the 33rd output. If the $\overline{\text{DATA ENABLE}}$ signal is not required, the 33rd output can be brought out. This is the MM5453 device.

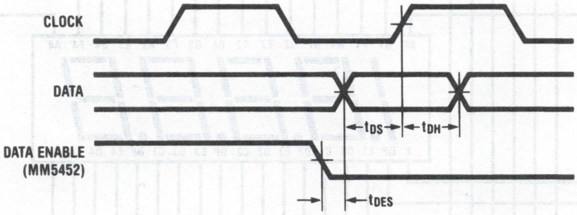
Functional Description (Continued)

Figure 4 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

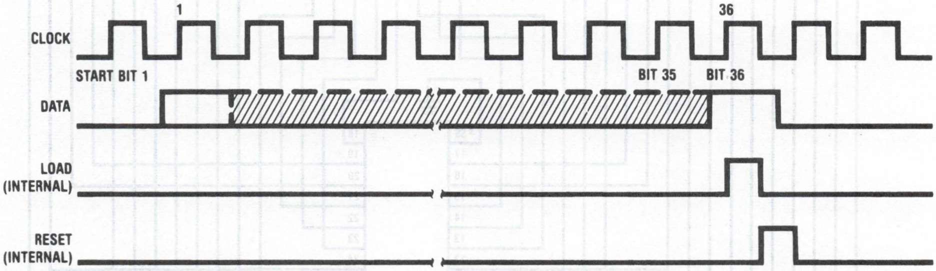
Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$.


CLOCK
DATA
DATA ENABLE
(MM5452)
t_{DS}
t_{DH}
t_{DES}

TL/F/6137-4

FIGURE 3

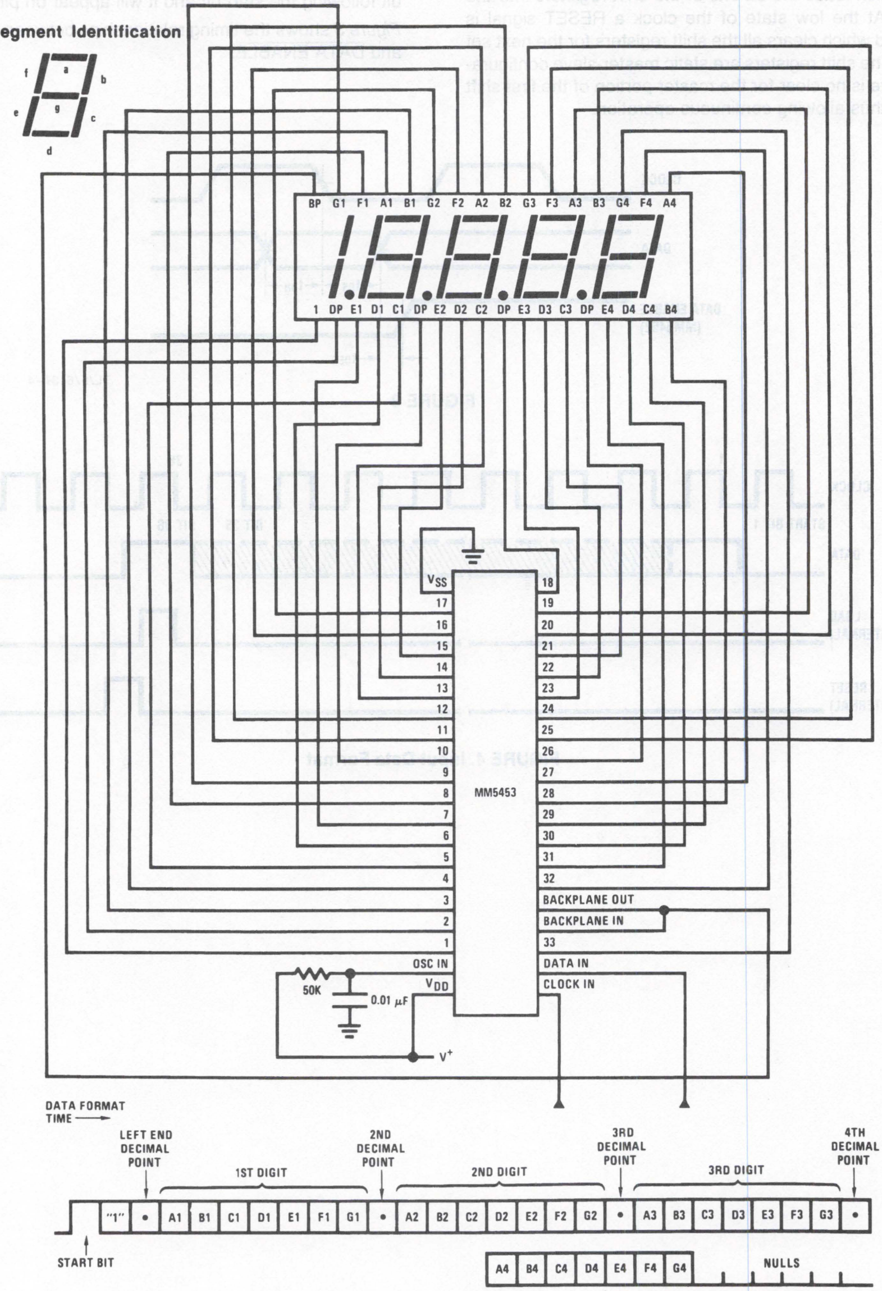

1
36
CLOCK
START BIT 1
BIT 35
BIT 36
DATA
LOAD
(INTERNAL)
RESET
(INTERNAL)

TL/F/6137-5

FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.

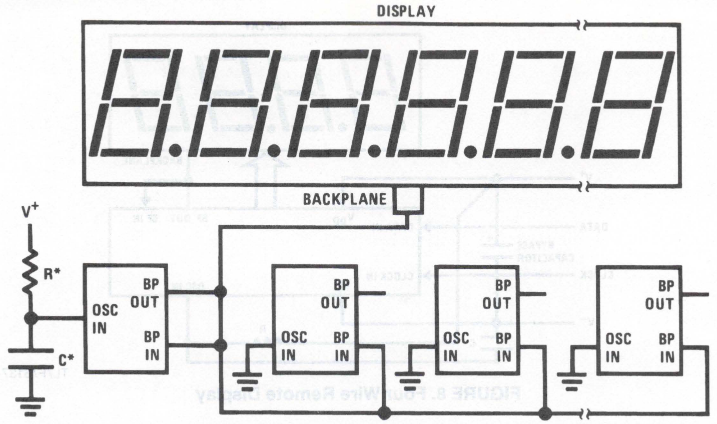

Segment Identification
a
b
c
d
e
f
g
BP G1 F1 A1 B1 G2 F2 A2 B2 G3 F3 A3 B3 G4 F4 A4
1 DP E1 D1 C1 DP E2 D2 C2 DP E3 D3 C3 DP E4 D4 C4 B4
VSS
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
OSC IN
VDD
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
BACKPLANE OUT
BACKPLANE IN
33
DATA IN
CLOCK IN
MM5453
50K
0.01 μF
V+
DATA FORMAT
TIME
LEFT END DECIMAL POINT
2ND DECIMAL POINT
3RD DECIMAL POINT
4TH DECIMAL POINT
1ST DIGIT
2ND DIGIT
3RD DIGIT
"1" • A1 B1 C1 D1 E1 F1 G1 • A2 B2 C2 D2 E2 F2 G2 • A3 B3 C3 D3 E3 F3 G3 •
START BIT
A4 B4 C4 D4 E4 F4 G4
NULLS

TL/F/6137-6

Consult LCD manufacturer's data sheet for specific pinouts.

FIGURE 5. Typical 4½-Digit Display Application

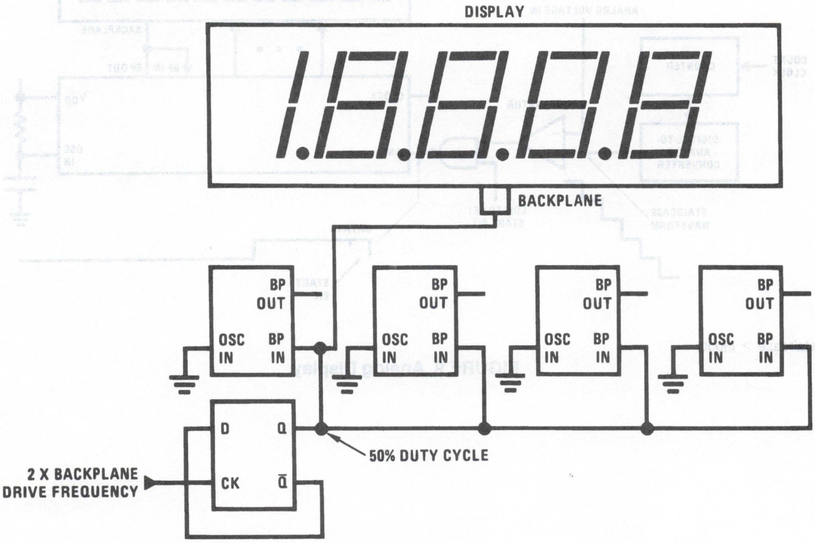
Functional Description (Continued)


DISPLAY
BACKPLANE
V+
R*
C*
OSC IN
BP OUT
BP IN
OSC IN
BP IN
BP OUT
OSC IN
BP IN
BP OUT
OSC IN
BP IN
BP OUT

TL/F/6137-7

*The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91 × 10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs


DISPLAY
BACKPLANE
BP OUT
OSC IN
BP IN
BP OUT
OSC IN
BP IN
BP OUT
OSC IN
BP IN
BP OUT
OSC IN
BP IN
D
Q
CK
Q̄
50% DUTY CYCLE
2 X BACKPLANE DRIVE FREQUENCY

TL/F/6137-8

FIGURE 7. External Backplane Clock

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

USING AN EXTERNAL CLOCK

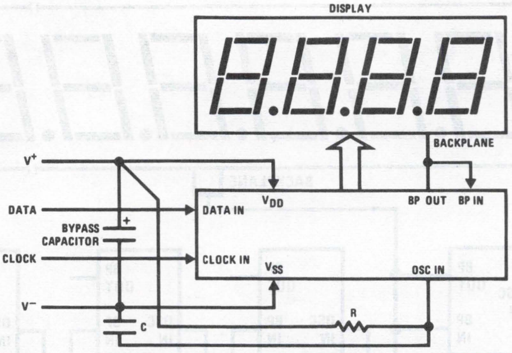
The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7,* a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

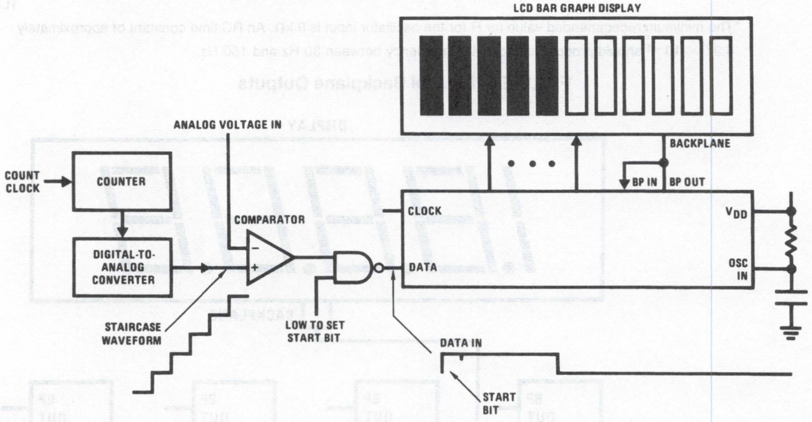
With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

Functional Description (Continued)


DISPLAY
BACKPLANE
V+
DATA
BYPASS CAPACITOR
CLOCK
V−
C
DATA IN
CLOCK IN
VDD
VSS
BP OUT
BP IN
OSC IN
R

TL/F/6137-9

FIGURE 8. Four Wire Remote Display


LCD BAR GRAPH DISPLAY
ANALOG VOLTAGE IN
COUNT CLOCK
COUNTER
DIGITAL-TO-ANALOG CONVERTER
COMPARATOR
−
+
STAIRCASE WAVEFORM
LOW TO SET START BIT
CLOCK
DATA
BACKPLANE
BP IN
BP OUT
VDD
OSC IN
DATA IN
START BIT

TL/F/6137-10

Data is high until staircase > input

FIGURE 9. Analog Display

National Semiconductor

MM5480 LED Display Driver

General Description

The MM5480 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5451 die packaged in a 28-pin package making it ideal for a 3½ digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

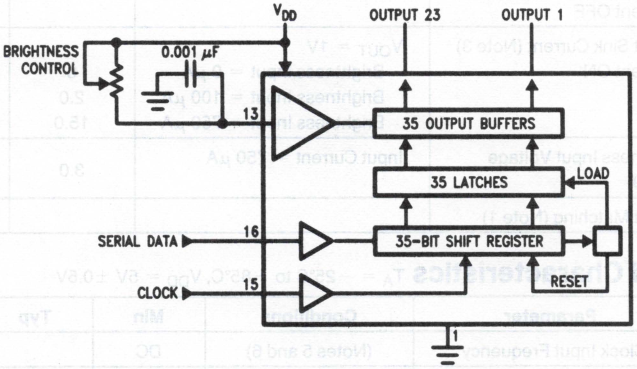
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 3½ digit displays

Applications

- COPS™ microcontrollers or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram



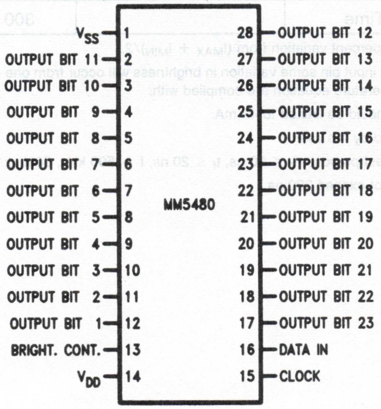
V_DD
OUTPUT 23
OUTPUT 1
BRIGHTNESS CONTROL
0.001 μF
13
35 OUTPUT BUFFERS
35 LATCHES
LOAD
SERIAL DATA
16
35-BIT SHIFT REGISTER
15
CLOCK
RESET
1

TL/F/6138-1

FIGURE 1

Connection Diagram

Dual-In-Line Package



V_SS 1
OUTPUT BIT 11 2
OUTPUT BIT 10 3
OUTPUT BIT 9 4
OUTPUT BIT 8 5
OUTPUT BIT 7 6
OUTPUT BIT 6 7
OUTPUT BIT 5 8
OUTPUT BIT 4 9
OUTPUT BIT 3 10
OUTPUT BIT 2 11
OUTPUT BIT 1 12
BRIGHT. CONT. 13
V_DD 14
28 OUTPUT BIT 12
27 OUTPUT BIT 13
26 OUTPUT BIT 14
25 OUTPUT BIT 15
24 OUTPUT BIT 16
23 OUTPUT BIT 17
22 OUTPUT BIT 18
21 OUTPUT BIT 19
20 OUTPUT BIT 20
19 OUTPUT BIT 21
18 OUTPUT BIT 22
17 OUTPUT BIT 23
16 DATA IN
15 CLOCK
MM5480

Order Number MM5480N
See NS Package Number N28B

TL/F/6138-2

Top View
FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Storage Temperature	−65°C to +150°C
Power Dissipation	490 mW at +85°C 940 mW at +25°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltage Logical "0" Level	±10 µA Input Bias	−0.3		0.8	V
V_{IH}	Input Voltage Logical "1" Level	4.75V ≤ V_{DD} ≤ 5.25V	2.2		V_{DD}	V
		V_{DD} > 5.25V	V_{DD} − 2		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	V_{OUT} = 3.0V			10.0	µA
I_{OL}	Output Sink Current (Note 3) Segment ON	V_{OUT} = 1V				
		Brightness Input = 0 µA	0		10.0	µA
		Brightness Input = 100 µA	2.0	2.7	4.0	mA
		Brightness Input = 750 µA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 µA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics T_A = −25°C to +85°C, V_{DD} = 5V ±0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
t_{DS}	Data Input Set-Up Time		300			ns
t_{DH}	Data Input Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation from $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5480 is specifically designed to operate 3½-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF ceramic or mica disc capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are 'Don't Cares'.

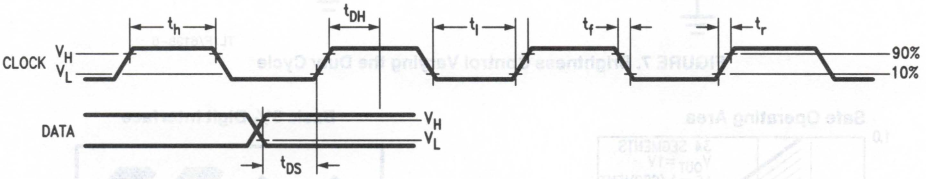
Figure 3 shows the timing relationships between data and clock. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(132°\text{C/W}) + T_A$$

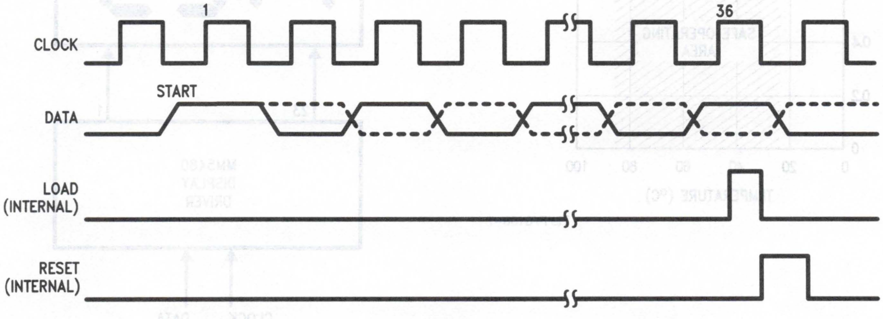
where:

T_j = junction temperature +150°C max.
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
132°C/W = thermal coefficient of the package
T_A = ambient temperature



TL/F/6138-3

FIGURE 3



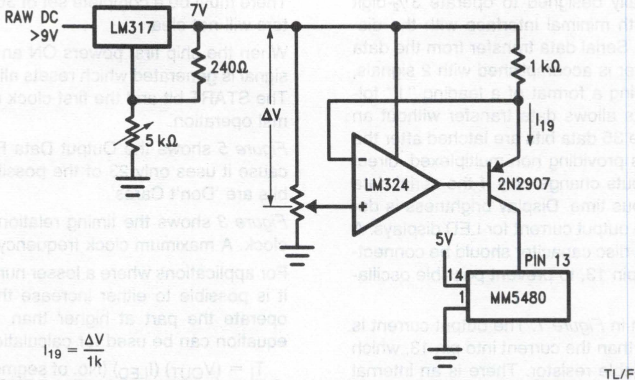
TL/F/6138-4

FIGURE 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	5451
START	X	1	2	3	4	5	6	7	X	X	X	8	9	10	11	X	X	X	X	12	13	14	15	16	17	X	18	X	X	19	20	21	22	23	X	5480

FIGURE 5. Output Data Format

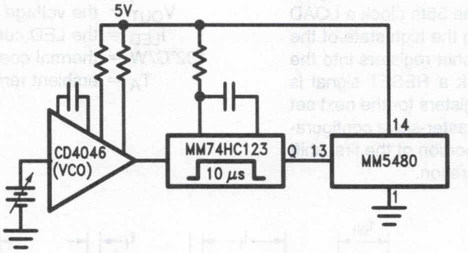
Functional Description (Continued)


RAW DC
>9V
LM317
7V
240Ω
ΔV
5 kΩ
1 kΩ
I_{19}
LM324
2N2907
5V
PIN 13
14
1
MM5480

$$I_{19} = \frac{\Delta V}{1k}$$

TL/F/6138-5

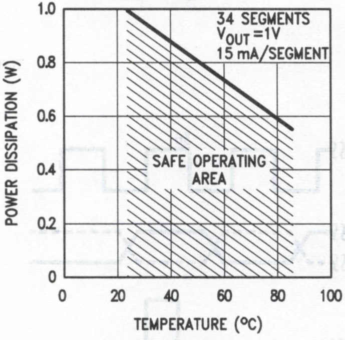
FIGURE 6. Typical Application of Constant Current Brightness Control


5V
CD4046
(VCO)
MM74HC123
10 μs
Q
13
14
MM5480
1

TL/F/6138-6

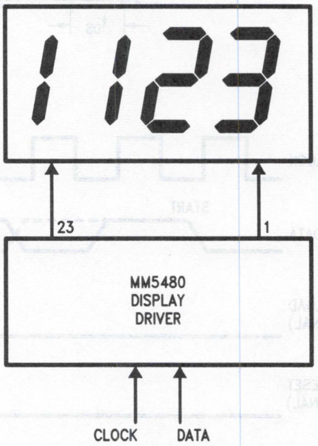
FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



TL/F/6138-7

Basic 3½-Digit Interface


1123
23
1
MM5480
DISPLAY
DRIVER
CLOCK
DATA

TL/F/6138-8

National Semiconductor

MM5481 LED Display Driver

General Description

The 5481 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5450 die packaged in a 20-pin package making it ideal for a 2 digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

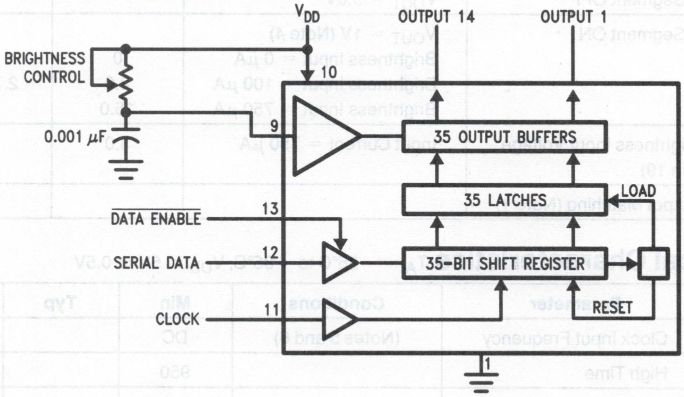
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Data enable
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 2 digit LED driver

Applications

- COPS or microprocessor displays
- Industrial control indicator
- Relay driver
- Instrumentation readouts

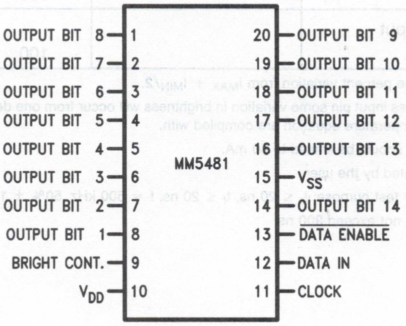
Block and Connection Diagrams



V_{DD}
OUTPUT 14
OUTPUT 1
BRIGHTNESS CONTROL
10
9
0.001 μF
35 OUTPUT BUFFERS
35 LATCHES
LOAD
$\overline{\text{DATA ENABLE}}$
13
SERIAL DATA
12
35-BIT SHIFT REGISTER
CLOCK
11
RESET
1
TL/F/6139-1

FIGURE 1

Dual-In-Line Package



OUTPUT BIT 8 — 1
OUTPUT BIT 7 — 2
OUTPUT BIT 6 — 3
OUTPUT BIT 5 — 4
OUTPUT BIT 4 — 5
OUTPUT BIT 3 — 6
OUTPUT BIT 2 — 7
OUTPUT BIT 1 — 8
BRIGHT CONT. — 9
V_{DD} — 10
20 — OUTPUT BIT 9
19 — OUTPUT BIT 10
18 — OUTPUT BIT 11
17 — OUTPUT BIT 12
16 — OUTPUT BIT 13
15 — V_{SS}
14 — OUTPUT BIT 14
13 — $\overline{\text{DATA ENABLE}}$
12 — DATA IN
11 — CLOCK
MM5481
TL/F/6139-2

Top View
FIGURE 2

Order Number MM5481N
See NS Package Number N20A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Storage Temperature	−65°C to +150°C
Power Dissipation	450 mW at +85°C 860 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltages Logical "0" Level	±10 µA Input Bias	−0.3		0.8	V
V_{IH}	Logical "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD} − 2		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	V_{OUT} = 3.0V			10.0	µA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4)				
		Brightness Input = 0 µA	0		10.0	µA
		Brightness Input = 100 µA	2.0	2.7	4.0	mA
		Brightness Input = 750 µA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 µA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 5V ± 0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
t_{DES}	Data Enable Input Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are compiled with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5481 uses the MM5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interference to the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are a static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the MM5481. Because it uses only 14 of the possible 34 outputs, 20 of the bits are 'Don't Cares'. Note that only alternate groups of 4 outputs are used.

Figure 3 shows the timing relationships between data, clock, and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})(I_{LED})(\text{No. of segments})(145^\circ C/W) + T_A$$

where:

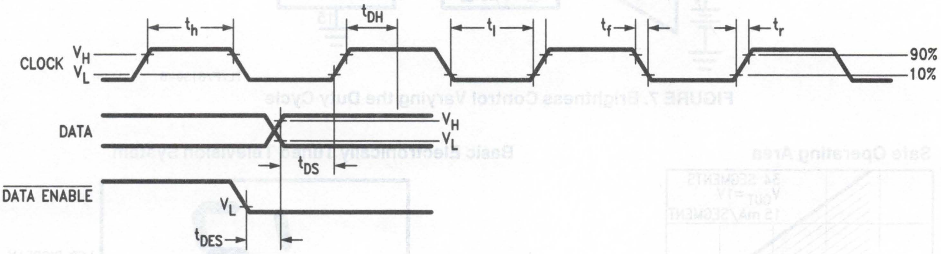
T_j = junction temperature + 150°C max.

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

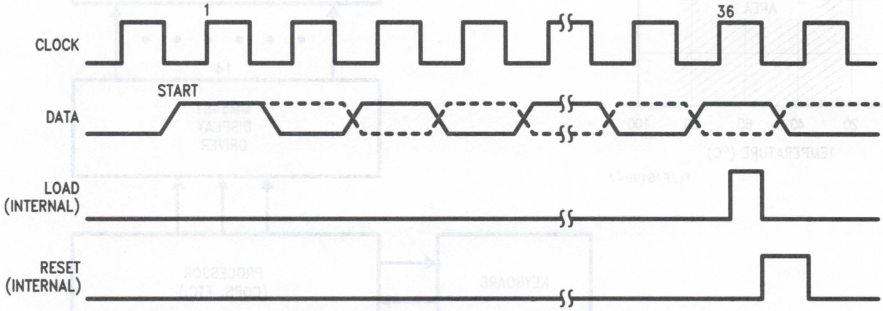
145°C/W = thermal coefficient of the package

T_A = ambient temperature



TL/F/6139-3

FIGURE 3. Timing



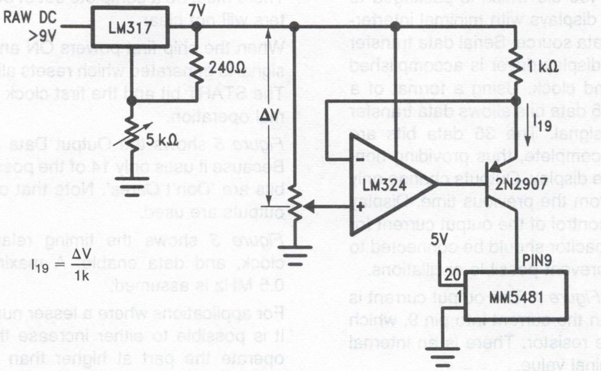
TL/F/6139-4

FIGURE 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	5450
START	X	X	X	X	1	2	3	4	X	X	X	X	5	6	7	8	X	X	X	X	9	10	11	12	X	X	X	X	13	14	X	X	X	X	5481

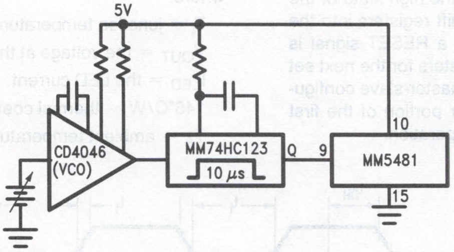
FIGURE 5. Output Data Format

Functional Description (Continued)


RAW DC
>9V
LM317
7V
240Ω
5 kΩ
ΔV
$I_{19} = \frac{\Delta V}{1k}$
1 kΩ
I_{19}
LM324
2N2907
−
+
5V
PIN9
20
MM5481

TL/F/6139–5

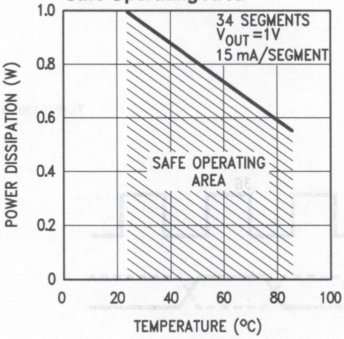
FIGURE 6. Typical Application of Constant Current Brightness Control


5V
CD4046
(VCO)
MM74HC123
10 μs
Q
9
10
MM5481
15

TL/F/6139–6

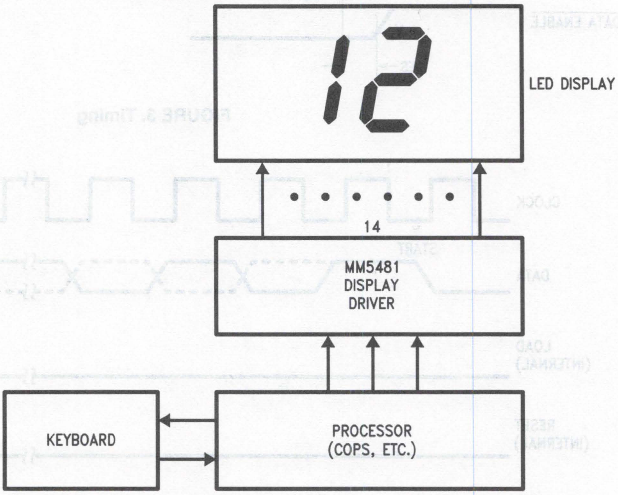
FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



TL/F/6139–7

Basic Electronically Tuned Television System


12
LED DISPLAY
14
MM5481
DISPLAY
DRIVER
KEYBOARD
PROCESSOR
(COPS, ETC.)

TL/F/6139–8

National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received

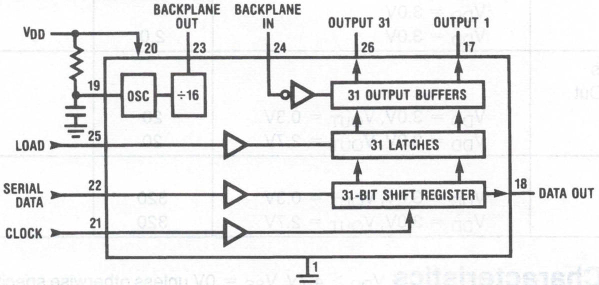
Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block and Connection Diagrams

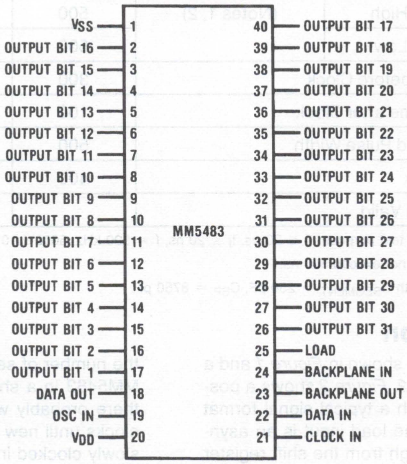


BACKPLANE OUT
BACKPLANE IN
OUTPUT 31
OUTPUT 1
V_{DD}
20
23
24
26
17
19
OSC
÷16
31 OUTPUT BUFFERS
31 LATCHES
LOAD
25
SERIAL DATA
22
31-BIT SHIFT REGISTER
18
DATA OUT
CLOCK
21
1

TL/F/6140–1

FIGURE 1

Dual-In-Line Package



V_{SS} 1
OUTPUT BIT 16 2
OUTPUT BIT 15 3
OUTPUT BIT 14 4
OUTPUT BIT 13 5
OUTPUT BIT 12 6
OUTPUT BIT 11 7
OUTPUT BIT 10 8
OUTPUT BIT 9 9
OUTPUT BIT 8 10
OUTPUT BIT 7 11
OUTPUT BIT 6 12
OUTPUT BIT 5 13
OUTPUT BIT 4 14
OUTPUT BIT 3 15
OUTPUT BIT 2 16
OUTPUT BIT 1 17
DATA OUT 18
OSC IN 19
V_{DD} 20
MM5483
40 OUTPUT BIT 17
39 OUTPUT BIT 18
38 OUTPUT BIT 19
37 OUTPUT BIT 20
36 OUTPUT BIT 21
35 OUTPUT BIT 22
34 OUTPUT BIT 23
33 OUTPUT BIT 24
32 OUTPUT BIT 25
31 OUTPUT BIT 26
30 OUTPUT BIT 27
29 OUTPUT BIT 28
28 OUTPUT BIT 29
27 OUTPUT BIT 30
26 OUTPUT BIT 31
25 LOAD
24 BACKPLANE IN
23 BACKPLANE OUT
22 DATA IN
21 CLOCK IN

Order Number MM5483N
See NS Package Number N40A

TL/F/6140–2

Top View

FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +85°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470 pF, Outputs Open				
	V_{DD} = 3.0V		9	15	µA
	V_{DD} = 5.0V		17	25	µA
	V_{DD} = 10.0V		35	45	µA
	OSC = 0V, Outputs Open, BPIN = 32 Hz, V_{DD} = 3.0V		1.5	2.5	µA
Input Voltage Levels	Load, Clock, Data				
Logic "0"	V_{DD} = 5.0V			0.9	V
Logic "1"	V_{DD} = 5.0V	2.4			V
Logic "0"	V_{DD} = 3.0V			0.4	V
Logic "1"	V_{DD} = 3.0V	2.0			V
Output Current Levels Segments and Data Out					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	20			µA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	20			µA
BP OUT					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	320			µA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	320			µA

AC Electrical Characteristics $V_{DD} \geq$ 4.7V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
f_C	Clock Frequency, V_{DD} = 3V				500	kHz
t_{CH}	Clock Period High	(Notes 1, 2)	500			ns
t_{CL}	Clock Period Low		500			ns
t_{DS}	Data Set-Up before Clock		300			ns
t_{DH}	Data Hold Time after Clock		100			ns
t_{LW}	Minimum Load Pulse Width		500			ns
t_{LTC}	Load to Clock		400			ns
t_{CDO}	Clock to Data Valid			400	750	ns

Note 1: AC input waveform specification for test purpose: $t_r \leq$ 20 ns, $t_f \leq$ 20 ns, f = 500 kHz, 50% ±10% duty cycle.

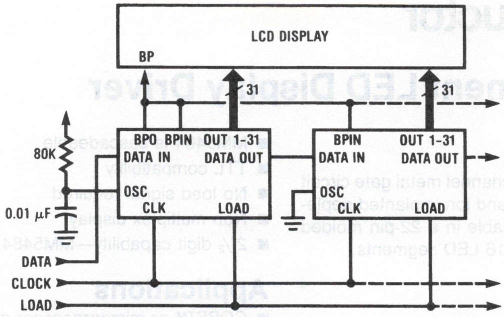
Note 2: Clock input rise and fall times must not exceed 300 ns.

Note 3: Output offset voltage is ±50 mV with $C_{SEGMENT}$ = 250 pF, C_{BP} = 8750 pF.

Functional Description

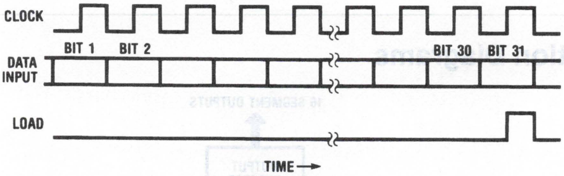
A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2*. *Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3*. Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5*. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6*. It should be noted that data out is not a TTL-compatible output.

Functional Description (Continued)


LCD DISPLAY
BP
31
31
BPO BPIN OUT 1-31
DATA IN DATA OUT
OSC
CLK LOAD
BPIN OUT 1-31
DATA IN DATA OUT
OSC
CLK LOAD
80K
0.01 μF
DATA
CLOCK
LOAD

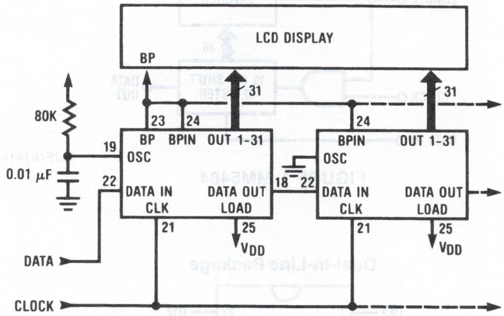
TL/F/6140-3

FIGURE 3. Three-Wire Control Mode


CLOCK
BIT 1
BIT 2
BIT 30
BIT 31
DATA INPUT
LOAD
TIME

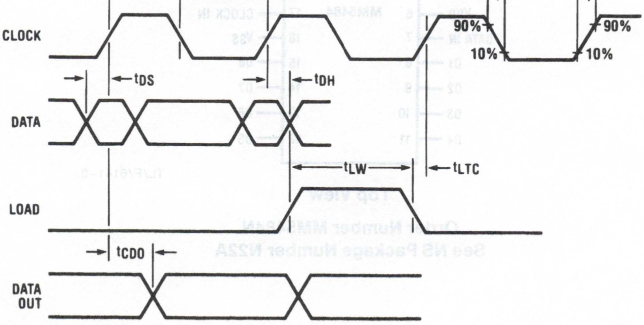
TL/F/6140-4

FIGURE 4. Data Format Diagram


LCD DISPLAY
BP
31
31
23
24
24
BP BPIN OUT 1-31
BPIN OUT 1-31
80K
19
OSC
OSC
0.01 μF
22
DATA IN DATA OUT
18
22
DATA IN DATA OUT
CLK LOAD
CLK LOAD
21
25
21
25
V_{DD}
V_{DD}
DATA
CLOCK

TL/F/6140-5

FIGURE 5. Two-Wire Control Mode


t_{CH}
t_{CL}
t_f
t_r
CLOCK
90%
10%
90%
10%
t_{DS}
t_{DH}
DATA
t_{LW}
t_{LTC}
LOAD
t_{CDO}
DATA OUT

TL/F/6140-6

FIGURE 6. Timing Diagram

National Semiconductor

MM5484 16-Segment LED Display Driver

General Description

The MM5484 is a low threshold N-channel metal gate circuit using low threshold enhancement and ion implanted depletion devices. The MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments.

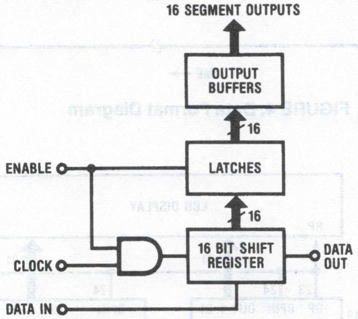
Features

- Serial data input
- Wide power supply operation
- 16 output, 15 mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

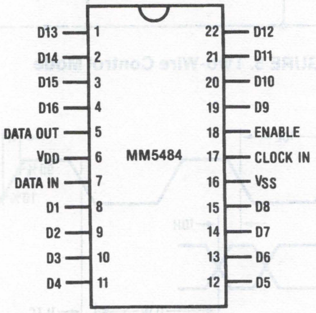
Block and Connection Diagrams


16 SEGMENT OUTPUTS
OUTPUT BUFFERS
16
ENABLE
LATCHES
16
16 BIT SHIFT REGISTER
CLOCK
DATA OUT
DATA IN

TL/F/6141-1

FIGURE 1. MM5484

Dual-In-Line Package


D13 1
D14 2
D15 3
D16 4
DATA OUT 5
VDD 6
DATA IN 7
D1 8
D2 9
D3 10
D4 11
22 D12
21 D11
20 D10
19 D9
18 ENABLE
17 CLOCK IN
16 VSS
15 D8
14 D7
13 D6
12 D5
MM5484

TL/F/6141-3

Top View

Order Number MM5484N
See NS Package Number N22A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at LED Outputs	V_{SS} − 0.5V to V_{SS} + 12V
Voltage at Other Pins	V_{SS} − 0.5V to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +150°C
Maximum Power Dissipation MM5484	500 mW
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		4.5		9	V
Supply Current			5	10	mA
Logic One Input High Level V_{IH}		2.4		V_{DD} + 0.5	V
Logic Zero Input Low Level V_{IL}		0		0.8	V
Input Current	High or Low Level			±1	μA
Input Capacitance				7.5	pF
OUTPUTS					
Data Output Voltage High Level V_{OH}	I_{OUT} = 0.1 mA	V_{DD} − 0.5			V
Low Level V_{OL}	I_{OUT} = −0.1 mA			0.5	V
Segment Off (Logic Zero on Input)	V_{OUT} = 12V R_{EXT} = 400Ω			50	μA
Output Current Segment On (Logic One on Input) Output Voltage	I_{OUT} = 15 mA V_{DD} ≥ 6V		0.5	1.0	V

AC Electrical Characteristics

(See *Figure 3.*) V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Frequency				0.5	MHz
t_h	High Time		0.95			μs
t_l	Low Time		0.95			μs
t_{S1}	Data Setup Time		0.5			μs
t_{H1}	Data Hold Time		0.5			μs
t_{S2}	Enable Setup Time		0.5			μs
t_{H2}	Enable Hold Time		0.5			μs
t_{pd}	Data Out Delay				0.5	μs

Note 1: Under no condition should the power dissipated by the segment driver exceed 50 mW nor the entire chip power dissipation exceed 500 mW.

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 500 ns.

Functional Description

The MM5484 is designed to drive LED displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, DATA IN, CLOCK and ENABLE. The signal ENABLE acts as an envelope and only while this signal is at a logic '1' do the circuits recognize the clock signal.

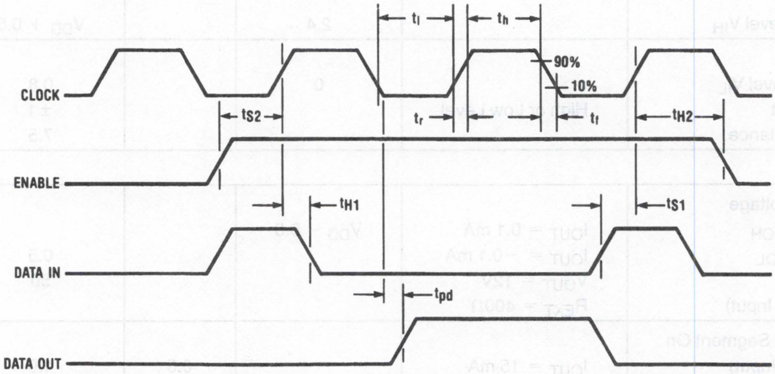
While ENABLE is high, data on the serial data input is transferred and shifted in the internal shift register on the rising clock edge, i.e. a logic '0' to logic '1' transition.

When the ENABLE signal goes to a low (logic zero state), the contents of the shift register is latched and the display will show the new data. While new data is being loaded into the SR the display will continue to show the old data.

For the MM5484, data is output from the serial DATA OUT pin on the falling edge of clock so cascading is made simple with race hazards eliminated.

When the chip first powers on, an internal power on reset signal is generated which resets the SR and latches to zero so that the display will be off.

Timing Diagram



TL/F/6141-5

FIGURE 3

National Semiconductor

MM5486 LED Display Driver

General Description

The MM5486 is a monolithic MOS integrated circuit utilizing N-channel metal-gate low-threshold, enhancement mode and ion-implanted depletion mode devices. It is available in a 40-pin molded dual-in-line package. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

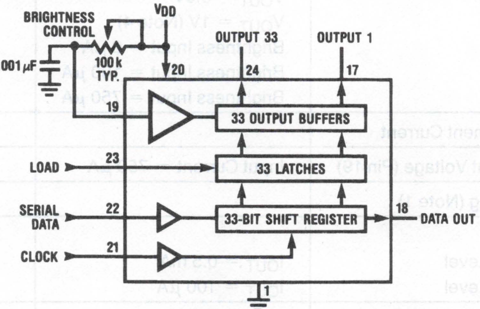
Features

- Continuous brightness control
- Serial data input/outut
- External load input
- Cascaded operation capability
- Wide power supply operation
- TTL compatibility
- 33 outputs, 15 mA sink capability
- Alphanumeric capability

Applications

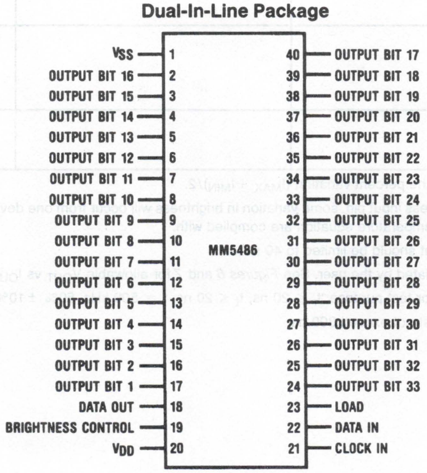
- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Reference MOS Brief #1

Block and Connection Diagrams


BRIGHTNESS CONTROL
VDD
0.001 µF
100k TYP.
20
19
OUTPUT 33
OUTPUT 1
24
17
33 OUTPUT BUFFERS
LOAD
23
33 LATCHES
SERIAL DATA
22
33-BIT SHIFT REGISTER
18
DATA OUT
CLOCK
21
1

TL/F/6142–1

FIGURE 1


Dual-In-Line Package
VSS 1
OUTPUT BIT 16 2
OUTPUT BIT 15 3
OUTPUT BIT 14 4
OUTPUT BIT 13 5
OUTPUT BIT 12 6
OUTPUT BIT 11 7
OUTPUT BIT 10 8
OUTPUT BIT 9 9
OUTPUT BIT 8 10
OUTPUT BIT 7 11
OUTPUT BIT 6 12
OUTPUT BIT 5 13
OUTPUT BIT 4 14
OUTPUT BIT 3 15
OUTPUT BIT 2 16
OUTPUT BIT 1 17
DATA OUT 18
BRIGHTNESS CONTROL 19
VDD 20
40 OUTPUT BIT 17
39 OUTPUT BIT 18
38 OUTPUT BIT 19
37 OUTPUT BIT 20
36 OUTPUT BIT 21
35 OUTPUT BIT 22
34 OUTPUT BIT 23
33 OUTPUT BIT 24
32 OUTPUT BIT 25
31 OUTPUT BIT 26
30 OUTPUT BIT 27
29 OUTPUT BIT 28
28 OUTPUT BIT 29
27 OUTPUT BIT 30
26 OUTPUT BIT 31
25 OUTPUT BIT 32
24 OUTPUT BIT 33
23 LOAD
22 DATA IN
21 CLOCK IN
MM5486

Order Number MM5486N
See NS Package Number N40A

TL/F/6142–2

Top View

FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	560 mW at +85°C 1W at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logic "0" Level	±10 µA Input Bias	−0.3		0.8	V
V_{IH}	Logic "1" Level	$4.75 \le V_{DD} \le 5.25$	2.2		V_{DD}	V
		$V_{DD} > 5.25$	$V_{DD}-2$		V_{DD}	V
I_{BR}	Brightness Input (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	V_{OUT} = 3.0V			10	µA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4)				
		Brightness Input = 0 µA	0		10	µA
		Brightness Input = 100 µA	2.0	2.7	4	mA
		Brightness Input = 750 µA	15		25	mA
I_O	Maximum Segment Current				40	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 µA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%
	Data Output					
V_{OL}	Logical "0" Level	I_{OUT} = 0.5 mA	V_{SS}		0.4	V
V_{OH}	Logical "1" Level	I_{OUT} = 100 µA	2.4		V_{DD}	V
	Clock Input	(Notes 5 and 6)				
f_C	Frequency				500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
	Data Enable Input					
t_{DES}	Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation ($I_{MAX} + I_{MIN}$)/2.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5486 is specifically designed to operate four-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock, and load. The data bits are latched by a positive-level load signal, thus providing non-multiplexed, direct drive to the display. When load is high, the data in the shift registers is displayed on the output drivers. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

A block diagram is shown in *Figure 1*.

Figure 4 shows the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED. The load signal latches the 33 bits of the shift register into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers.

When the chip first powers ON, an internal power ON reset signal is generated which resets all registers and latches. The leading clock returns the chip to its normal operation.

Figure 3 shows the timing relationship between data, clock and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations:

$$T_J = (V_{OUT})(I_{LED})(\text{No. of segments})(124°\text{C/W}) + T_A$$

where:

T_J = junction temperature +150°C max.

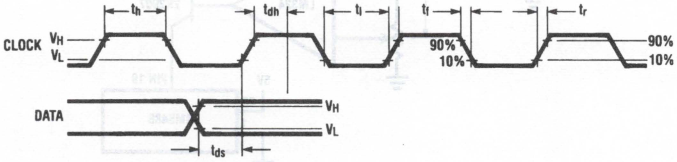
V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

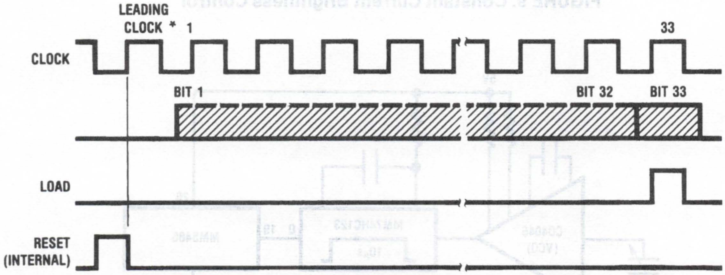
T_A = ambient temperature

The above equation was used to plot *Figure 6, Figure 7,* and *Figure 8*.



TL/F/6142-3

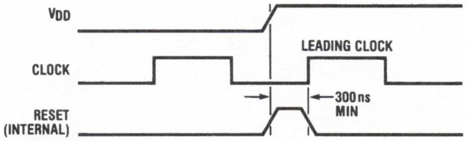
FIGURE 3



TL/F/6142-4

*This leading clock is necessary only after power ON.

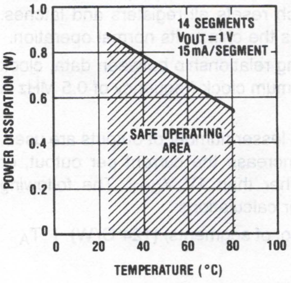
FIGURE 4. Input Data Format



TL/F/6142-5

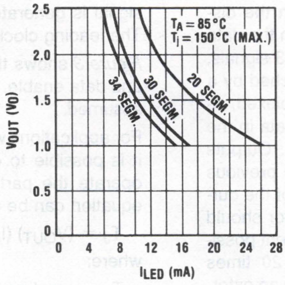
FIGURE 5

Typical Applications



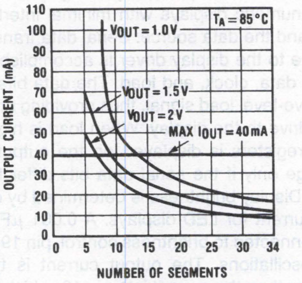
TL/F/6142-6

FIGURE 6



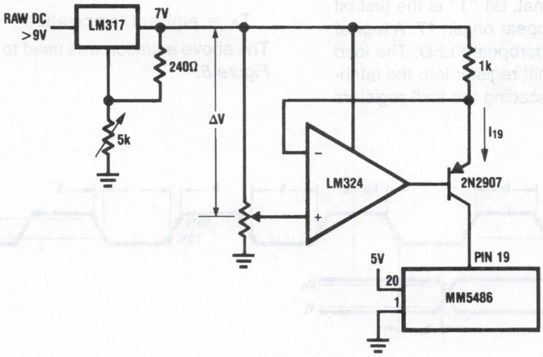
TL/F/6142-7

FIGURE 7



TL/F/6142-8

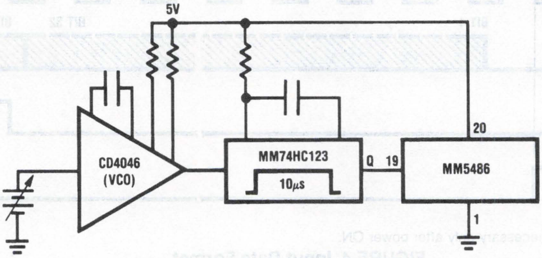
FIGURE 8


RAW DC
>9V
LM317
7V
240Ω
5k
ΔV
1k
I19
LM324
2N2907
PIN 19
5V
20
1
MM5486

TL/F/6142-9

$$I_{19} = \frac{\Delta V}{1k}$$

FIGURE 9. Constant Current Brightness Control

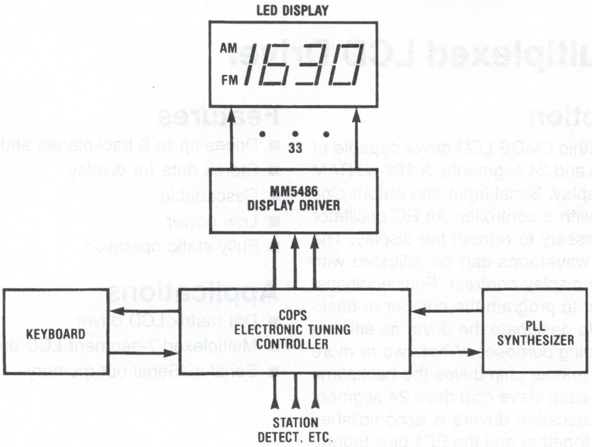

5V
CD4046
(VCO)
MM74HC123
10μs
Q
19
20
MM5486
1

TL/F/6142-10

FIGURE 10. Brightness Control Varying the Duty Cycle

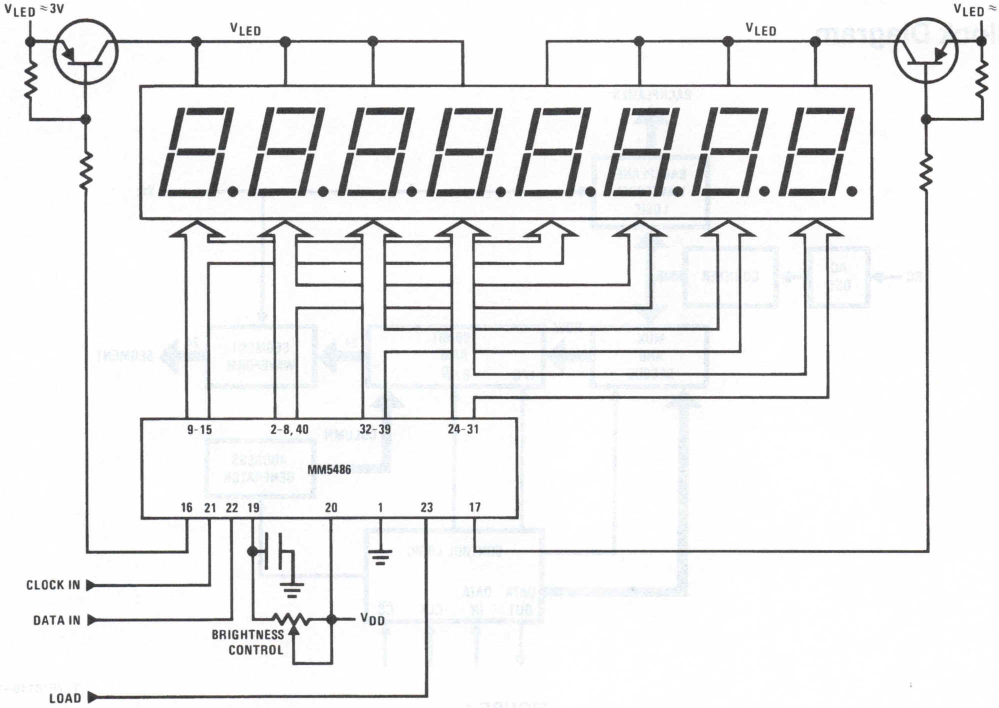
Typical Applications (Continued)

Basic Electronically Tuned Radio System


LED DISPLAY
AM
FM
1630
33
MM5486
DISPLAY DRIVER
KEYBOARD
COPS
ELECTRONIC TUNING
CONTROLLER
PLL
SYNTHESIZER
STATION
DETECT, ETC.

TL/F/6142-11

Duplexing 8 Digits with One MM5486


V_LED ≈ 3V
V_LED
V_LED
V_LED ≈ 3V
9-15
2-8, 40
32-39
24-31
MM5486
16
21
22
19
20
1
23
17
CLOCK IN
DATA IN
V_DD
BRIGHTNESS
CONTROL
LOAD

TL/F/6142-12

*This driver has 7 segments only.

4

National Semiconductor

MM58201 Multiplexed LCD Driver

General Description

The MM58201 is a monolithic CMOS LCD driver capable of driving up to 8 backplanes and 24 segments. A 192-bit RAM stores the data for the display. Serial input and output pins are provided to interface with a controller. An RC oscillator generates the timing necessary to refresh the display. The magnitude of the driving waveforms can be adjusted with the V_{TC} input to optimize display contrast. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines. Synchronizing the cascaded drivers is accomplished by tying the RC OSC pins together and the BP1 pins together.

The MM58201 is packaged in a 40-lead dual-in-line package, or 44 lead plastic chip carrier package.

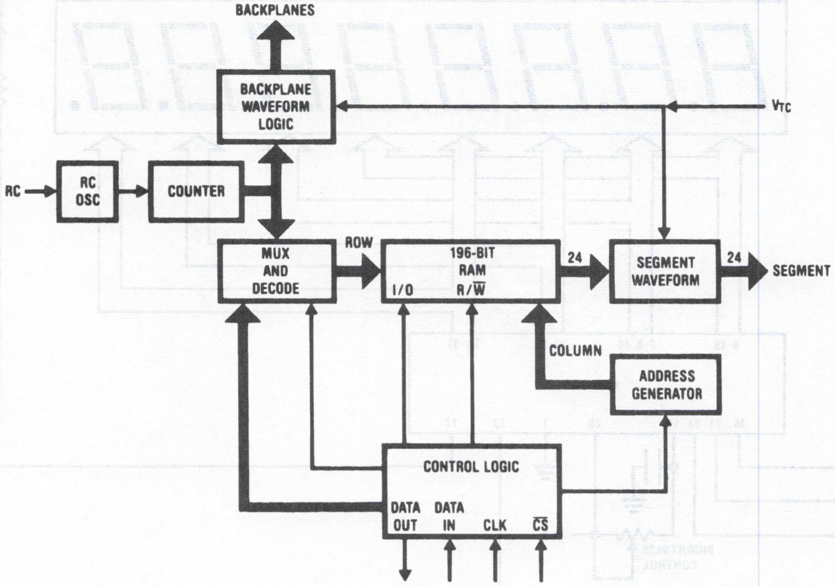
Features

- Drives up to 8 backplanes and 24 segment lines
- Stores data for display
- Cascadable
- Low power
- Fully static operation

Applications

- Dot matrix LCD driver
- Multiplexed 7-segment LCD driver
- Serial in/Serial out memory

Block Diagram


BACKPLANES
BACKPLANE WAVEFORM LOGIC
V_{TC}
RC
RC OSC
COUNTER
MUX AND DECODE
ROW
196-BIT RAM
I/O
R/$\overline{W}$
24
SEGMENT WAVEFORM
24
SEGMENT
COLUMN
ADDRESS GENERATOR
CONTROL LOGIC
DATA OUT
DATA IN
CLK
$\overline{CS}$

TL/F/6146-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} −0.3V to V_{SS} +18V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} +7.0V to V_{SS} +18.0V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Supply Current				0.3	mA
$V_{IN(1)}$	Logical "1" Input Voltage		0.45 V_{DD}		V_{DD} +0.3	V
$V_{IN(0)}$	Logical "0" Input Voltage		V_{SS} −0.3		1.0	V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{SINK} = 0.6 mA			0.4	V
$I_{OUT(1)}$	Logical "1" Output Leakage Current	V_{OUT} = V_{DD}	0		±10	μA
$I_{IN(1)}$	Logical "1" Input Leakage Current	V_{IN} = V_{DD}	0		1.0	μA
$I_{IN(0)}$	Logical "0" Input Leakage Current	V_{IN} = V_{SS}	−1.0		0	μA
V_{TC}	Input Voltage		4.5		V_{DD} +0.3	V
V_{TC}	Input Impedance		10		30	kΩ
Z_{OUT}	Output Impedance	Backplane and Segment Outputs			10	kΩ
Z_{OUT}	DC Offset Voltage	Between Any Backplane and Segment Output	0		±10	mV

AC Electrical Characteristics

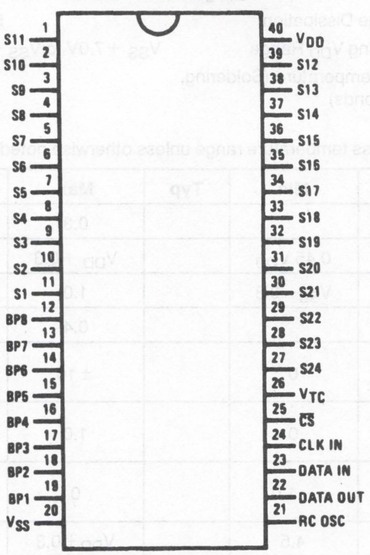
T_A and V_{DD} within operating range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator Frequency*		128η		400η	Hz
$f_{CLK\ IN}$	Clock Frequency		DC		100	kHz
t_{ON}	Clock Pulse Width		5.0			μs
t_{OFF}	Clock OFF Time		5.0			μs
t_s	Input Data Set-Up Time		2.0			μs
t_H	Input Data Hold Time		1.0			μs
t_{ACC}	Access Time		5.0			μs
t_r	Rise Time	Backplane, Segment Outputs C_L = 2000 pF			60	μs
t_f	Fall Time	Backplane, Segment Outputs C_L = 2000 pF			60	μs

* η is the number of backplanes programmed.

Connection Diagrams

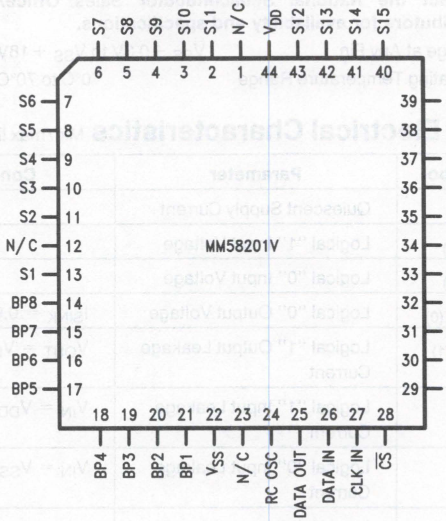
Dual-In-Line Package


S11
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
BP8
BP7
BP6
BP5
BP4
BP3
BP2
BP1
VSS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
40 VDD
39 S12
38 S13
37 S14
36 S15
35 S16
34 S17
33 S18
32 S19
31 S20
30 S21
29 S22
28 S23
27 S24
26 VTC
25 CS
24 CLK IN
23 DATA IN
22 DATA OUT
21 RC OSC

TL/F/6146-2

Top View

Plastic Chip Carrier


S7 6
S8 5
S9 4
S10 3
S11 2
N/C 1
VDD 44
S12 43
S13 42
S14 41
S15 40
S6 7
S5 8
S4 9
S3 10
S2 11
N/C 12
S1 13
BP8 14
BP7 15
BP6 16
BP5 17
39 S16
38 S17
37 S18
36 S19
35 S20
34 N/C
33 S21
32 S22
31 S23
30 S24
29 VTC
MM58201V
18 BP4
19 BP3
20 BP2
21 BP1
22 VSS
23 N/C
24 RC OSC
25 DATA OUT
26 DATA IN
27 CLK IN
28 CS

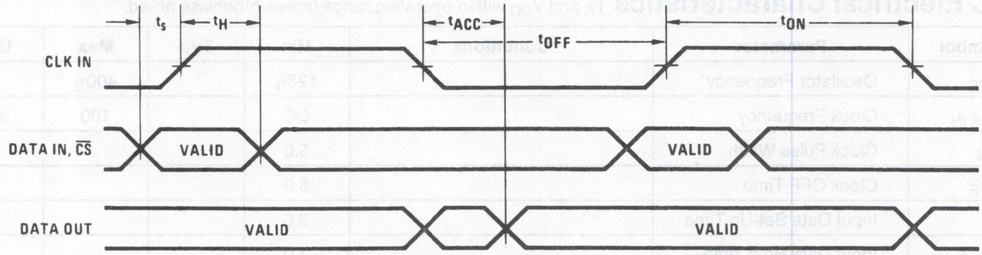
TL/F/6146-10

Top View

FIGURE 2

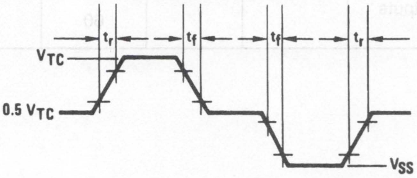
Order Number MM58201N or MM58201V
See NS Package Number N40A or V44A

Switching Time Waveforms


tS
tH
tACC
tOFF
tON
CLK IN
DATA IN, CS
VALID
VALID
DATA OUT
VALID
VALID

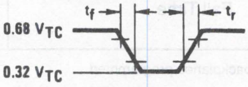
TL/F/6146-3

Backplane Output


tr
tf
tf
tr
VTC
0.5 VTC
VSS

TL/F/6146-4

Segment Output


tf
tr
0.68 VTC
0.32 VTC

TL/F/6146-5

Functional Description

A functional diagram of the MM58201 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

SERIAL INPUTS AND OUTPUTS

A negative-going edge on the $\overline{CS}$ input initiates a frame. The $\overline{CS}$ input must then stay low for at least one rising edge of CLK IN, and may not be pulsed low again for the next 31 clocks. At least one clock must occur while $\overline{CS}$ is high. If CLK IN is held at a logic "1", $\overline{CS}$ is disabled. This allows the signal that drives $\overline{CS}$ to be used for other purposes when the MM58201 is not being addressed.

CLK IN latches data from the DATA IN input on its rising edge. Data from the DATA OUT pin changes on the falling edge of CLK IN and is valid before the next rising edge.

The first five bits of data following $\overline{CS}$ are the address bits *(Figure 3)*. The address selects the column where the operation is to start. Bit 1 is the MSB and bit 5 is the LSB. The sixth bit is the read/write bit. A logic "1" specifies a read operation and a logic "0" specifies a write operation. The next 24 bits are the data bits. The first data bit corresponds to the BP1 row of the display, the second data bit to the BP2 row, and so on. After the eighth and sixteenth data bits, the column pointer is incremented. When starting address 10110 or 10111 is specified, the column pointer increments from 10111 to 00000.

During a read or write cycle, the LCD segment outputs do not reflect the data in the RAM. To avoid disrupting the pattern viewed on the display, the read or write cycle time should be kept short. Since the LCD turn-on time can be as little as 30 ms, a clock rate of at least 10 kHz would be required in order to address the entire contents of the RAM within that time interval. The formula below can be used to estimate the minimum clock rate:

$$f_{CLK\ IN} = \frac{30}{(t_{LCD} - 7t_s)}$$

where t_s is the processor's set-up time between each read or write cycle, and t_{LCD} is the minimum turn-on or turn-off time of the LCD as specified by the LCD manufacturer.

The DATA OUT output is an open drain N-channel device to V_{SS} *(Figure 4)*. With an external pull-up this configuration allows the controller to operate at a lower supply voltage, and also permits the DATA OUT output to be wired in parallel with the DATA OUT outputs from any other drivers in the system.

To program the number of backplanes being driven and the M/$\overline{S}$ bit, load address 11000, a write bit, three bits for the number of backplanes (Table I), and the M/$\overline{S}$ bit. The remaining 20 data bits will be ignored but it is necessary to provide 21 more clocks before initiating another frame.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

RC OSC Pin

This oscillator generates the timing required for multiplexing the liquid crystal display. The oscillator operates at a frequency that is 4η times the refresh rate of the display, where η is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency must be:

$$128\eta \le f_{OSC} \le 400\eta$$

The frequency of oscillation is related to the external R and C components in the following way:

$$f_{OSC} = \frac{1}{1.25\ RC} \pm 30\%$$

The value used for the external resistor should be in the range from 10 kΩ to 1 MΩ.

The value used for the external capacitor should be less than 0.005 μF.

V_{TC} Pin

The V_{TC} pin is an analog input that controls the contrast of the segments on the LCD. If eight backplanes are being driven ($\eta = 8$), a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display. It also has a significant negative temperature coefficient.

The voltage source on the V_{TC} input must be of relatively low impedance since the input impedance of V_{TC} ranges from 10 kΩ to 30 kΩ. A suitable circuit is shown in *Figure 5*.

In a standby mode, the V_{TC} input can be set to V_{SS}. This reduces the supply current to less than 300 μA per driver.

BACKPLANE AND SEGMENT OUTPUTS

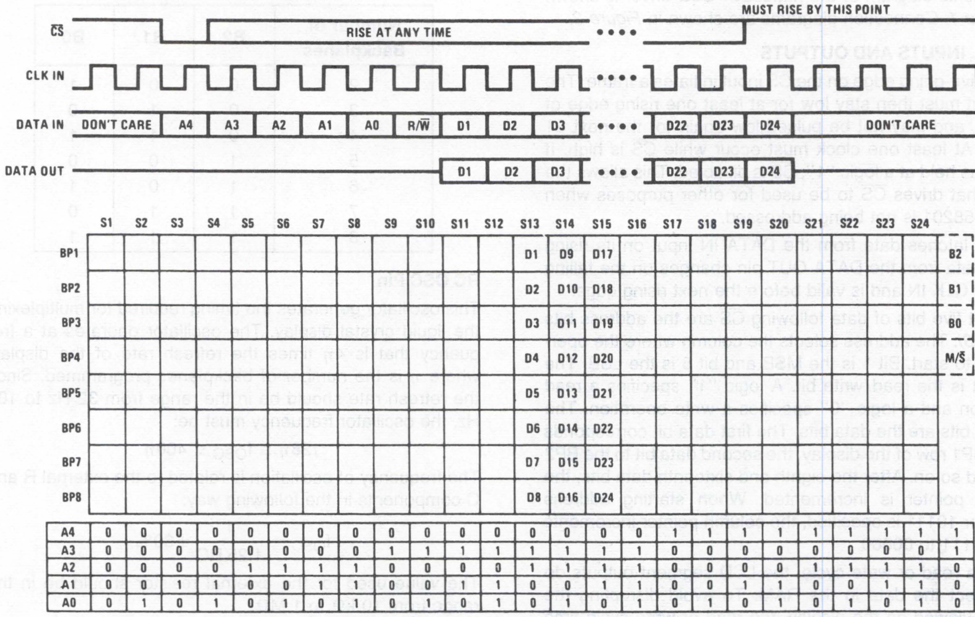
Connect the backplane and segment outputs directly to the LCD row and column lines. The outputs are designed to drive a display with a total ON capacitance of up to 2000 pF.

The output structure consists of transmission gates tapped off of a resistor string driven by V_{TC} *(Figure 6)*.

A critical factor in the lifetime of an LCD is the amount of DC offset between a backplane and segment signal. Typically, 50 mV of offset is acceptable. The MM58201 guarantees an offset of less than 10 mV.

The BP1 output is disabled when the M/$\overline{S}$ bit is set to zero. This allows the BP1 output from the master chip to be connected directly to it so that synchronizing signals can be generated. Synchronization occurs once each refresh cycle, so the cascaded chips are assured of remaining synchronized.

Functional Description (Continued)

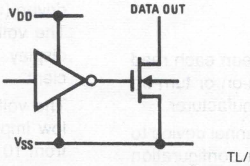

CS
RISE AT ANY TIME
MUST RISE BY THIS POINT
CLK IN
DATA IN
DON'T CARE
A4
A3
A2
A1
A0
R/W̄
D1
D2
D3
D22
D23
D24
DON'T CARE
DATA OUT
D1
D2
D3
D22
D23
D24
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16 S17 S18 S19 S20 S21 S22 S23 S24
BP1
BP2
BP3
BP4
BP5
BP6
BP7
BP8
D1 D9 D17
D2 D10 D18
D3 D11 D19
D4 D12 D20
D5 D13 D21
D6 D14 D22
D7 D15 D23
D8 D16 D24
B2
B1
B0
M/S̄

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	
A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

TL/F/6146–6

Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

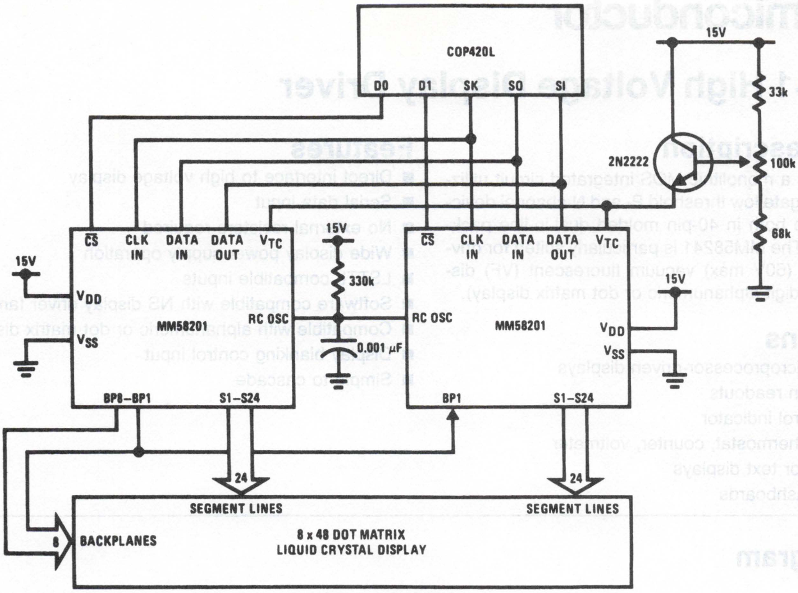
FIGURE 3. Data Format


DATA OUT
V_{DD}
V_{SS}

TL/F/6146–7

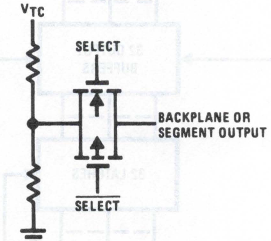
FIGURE 4. DATA OUT Structure

Functional Description (Continued)


COP420L
D0
D1
SK
SO
SI
15V
33k
2N2222
100k
68k
15V
CS
CLK IN
DATA IN
DATA OUT
VTC
15V
330k
VDD
MM58201
RC OSC
VSS
0.001 μF
CS
CLK IN
DATA IN
DATA OUT
VTC
RC OSC
MM58201
VDD
VSS
BP8–BP1
S1–S24
BP1
S1–S24
24
24
SEGMENT LINES
SEGMENT LINES
8
BACKPLANES
8 x 48 DOT MATRIX
LIQUID CRYSTAL DISPLAY

TL/F/6146–8

FIGURE 5. Typical Application


VTC
SELECT
BACKPLANE OR
SEGMENT OUTPUT
SELECT

TL/F/6146–9

FIGURE 6. Structure of LCD Outputs

National Semiconductor

MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

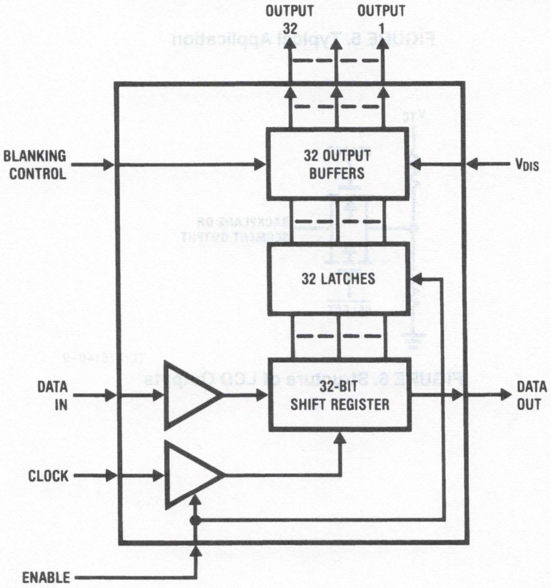
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram


OUTPUT 32
OUTPUT 1
BLANKING CONTROL
32 OUTPUT BUFFERS
V_{DIS}
32 LATCHES
DATA IN
32-BIT SHIFT REGISTER
DATA OUT
CLOCK
ENABLE

TL/F/5600–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 62.5V
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	µA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −55V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 µA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 µA	V_{DD} − 0.5			V
V_{OH}	Logic '1'	I_{OUT} = −500 µA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	µA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off *(Figure 3a)*	V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = −40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −55V ≤ V_{DIS} ≤ −25V	V_{DIS}		V_{DIS} + 4	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 µA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 µA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

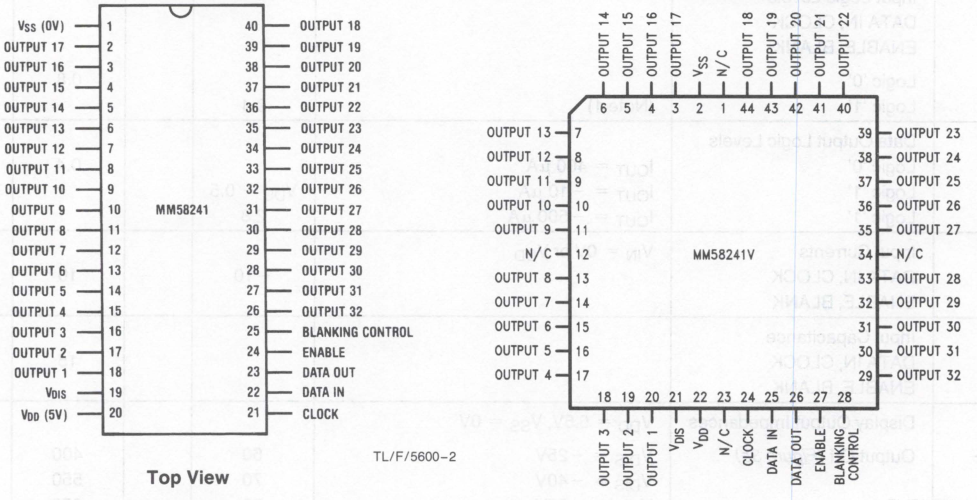
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input					
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50\ pF$				
t_{CDO}	CLOCK Low to Data Out Time				500	ns

Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams


VSS (0V) 1
OUTPUT 17 2
OUTPUT 16 3
OUTPUT 15 4
OUTPUT 14 5
OUTPUT 13 6
OUTPUT 12 7
OUTPUT 11 8
OUTPUT 10 9
OUTPUT 9 10
OUTPUT 8 11
OUTPUT 7 12
OUTPUT 6 13
OUTPUT 5 14
OUTPUT 4 15
OUTPUT 3 16
OUTPUT 2 17
OUTPUT 1 18
VDIS 19
VDD (5V) 20
40 OUTPUT 18
39 OUTPUT 19
38 OUTPUT 20
37 OUTPUT 21
36 OUTPUT 22
35 OUTPUT 23
34 OUTPUT 24
33 OUTPUT 25
32 OUTPUT 26
31 OUTPUT 27
30 OUTPUT 28
29 OUTPUT 29
28 OUTPUT 30
27 OUTPUT 31
26 OUTPUT 32
25 BLANKING CONTROL
24 ENABLE
23 DATA OUT
22 DATA IN
21 CLOCK
MM58241
OUTPUT 14 6
OUTPUT 15 5
OUTPUT 16 4
OUTPUT 17 3
VSS 2
N/C 1
OUTPUT 18 44
OUTPUT 19 43
OUTPUT 20 42
OUTPUT 21 41
OUTPUT 22 40
OUTPUT 13 7
OUTPUT 12 8
OUTPUT 11 9
OUTPUT 10 10
OUTPUT 9 11
N/C 12
OUTPUT 8 13
OUTPUT 7 14
OUTPUT 6 15
OUTPUT 5 16
OUTPUT 4 17
39 OUTPUT 23
38 OUTPUT 24
37 OUTPUT 25
36 OUTPUT 26
35 OUTPUT 27
34 N/C
33 OUTPUT 28
32 OUTPUT 29
31 OUTPUT 30
30 OUTPUT 31
29 OUTPUT 32
18 OUTPUT 3
19 OUTPUT 2
20 OUTPUT 1
21 VDIS
22 VDD
23 N/C
24 CLOCK
25 DATA IN
26 DATA OUT
27 ENABLE
28 BLANKING CONTROL
MM58241V

Dual-In-Line Package

Top View

TL/F/5600-2

Plastic Chip Carrier

Top View

TL/F/5600-8

FIGURE 2

Order Number MM58241N or MM58241V
See NS Package Number N40A or V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58421 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58241 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58241 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following ENABLE high. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58241, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

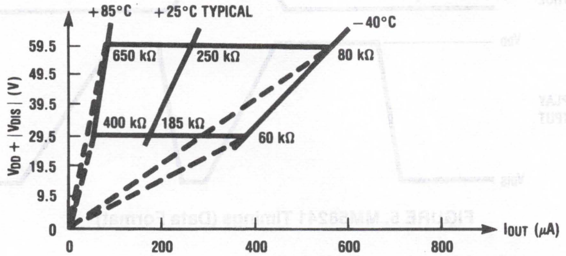
Functional Description (Continued)

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58241.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

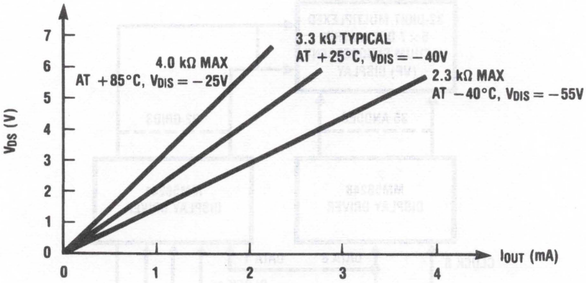
In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58241, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58241 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vaccum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.



TL/F/5600-3

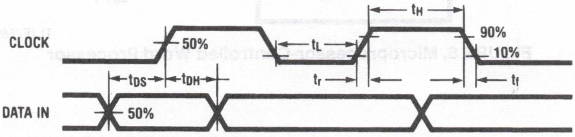
FIGURE 3a. Output Impedance Off



TL/F/5600-4

FIGURE 3b. Output Impedance On

Timing Diagrams

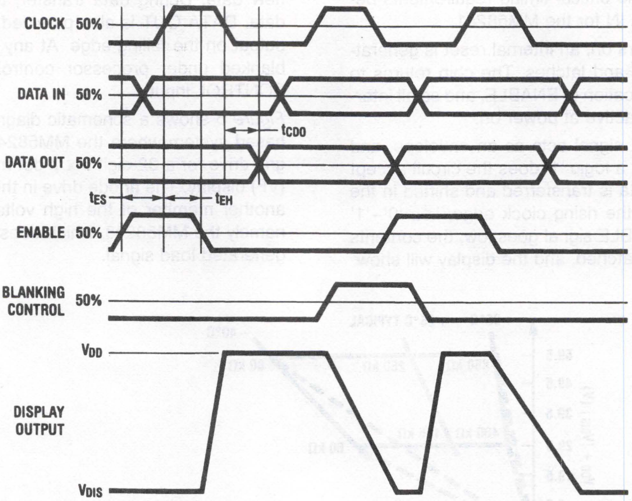


TL/F/5600-5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

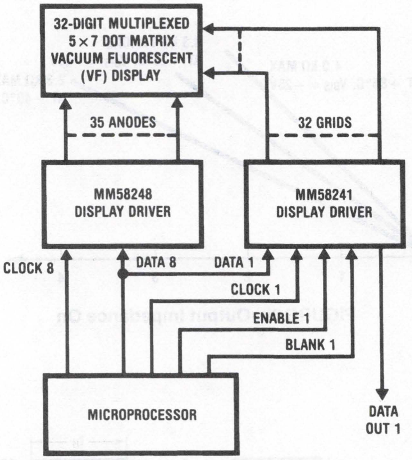
Timing Diagrams (Continued)


CLOCK 50%
DATA IN 50%
tCDO
DATA OUT 50%
tES
tEH
ENABLE 50%
BLANKING CONTROL 50%
VDD
DISPLAY OUTPUT
VDIS

TL/F/5600-6

FIGURE 5. MM58241 Timings (Data Format)

Typical Application


32-DIGIT MULTIPLEXED 5×7 DOT MATRIX VACUUM FLUORESCENT (VF) DISPLAY
35 ANODES
32 GRIDS
MM58248 DISPLAY DRIVER
MM58241 DISPLAY DRIVER
CLOCK 8
DATA 8
DATA 1
CLOCK 1
ENABLE 1
BLANK 1
MICROPROCESSOR
DATA OUT 1

TL/F/5600-7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58242 High Voltage Display Driver

General Description

The MM58242 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58242 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

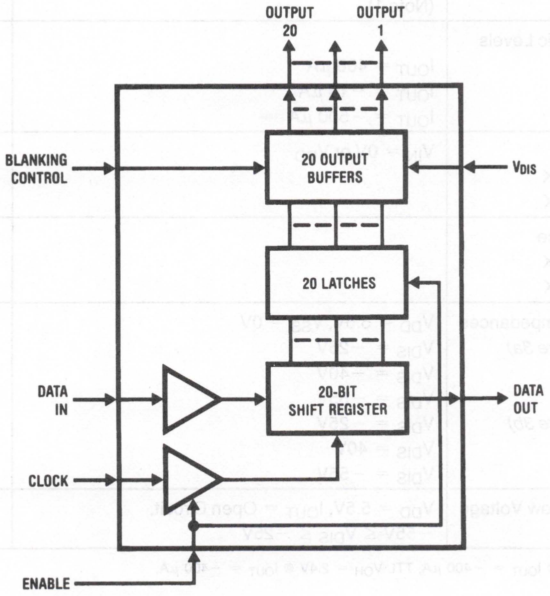
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram


OUTPUT 20
OUTPUT 1
BLANKING CONTROL
20 OUTPUT BUFFERS
V_{DIS}
20 LATCHES
DATA IN
20-BIT SHIFT REGISTER
DATA OUT
CLOCK
ENABLE

TL/F/7924–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} −0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} −62.5V
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	µA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = 55V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 µA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 µA	V_{DD}−0.5			V
V_{OH}	Logic '1'	I_{OUT} = −500 µA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	µA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off *(Figure 3a)*	V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = 40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, $-55V \le V_{DIS} \le -25V$	V_{DIS}		V_{DIS}+4	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 µA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 µA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input	(Note 2)				
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
CLOCK Low to Data Out Time, t_{CDO}				500	ns

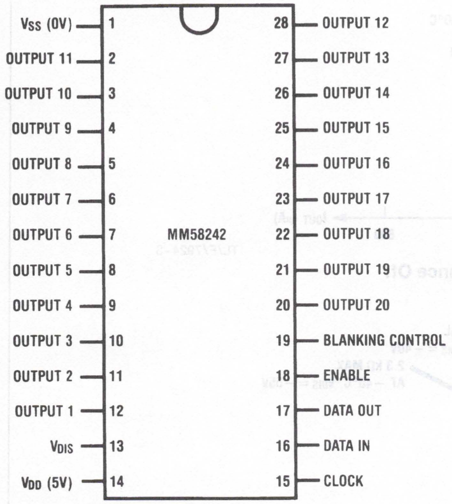
Note 2: For timimg purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $f = 800$ kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 µs.

Connection Diagrams

Dual-In-Line Package

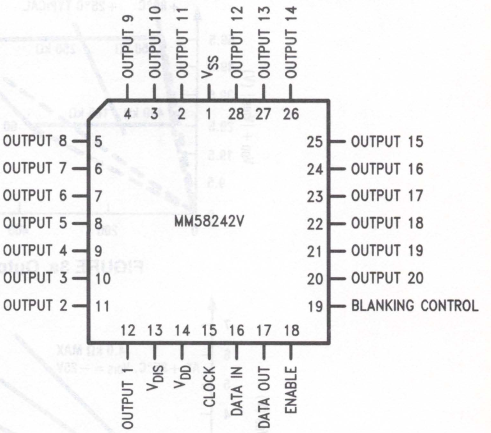

VSS (0V) 1
OUTPUT 11 2
OUTPUT 10 3
OUTPUT 9 4
OUTPUT 8 5
OUTPUT 7 6
OUTPUT 6 7
OUTPUT 5 8
OUTPUT 4 9
OUTPUT 3 10
OUTPUT 2 11
OUTPUT 1 12
VDIS 13
VDD (5V) 14
28 OUTPUT 12
27 OUTPUT 13
26 OUTPUT 14
25 OUTPUT 15
24 OUTPUT 16
23 OUTPUT 17
22 OUTPUT 18
21 OUTPUT 19
20 OUTPUT 20
19 BLANKING CONTROL
18 ENABLE
17 DATA OUT
16 DATA IN
15 CLOCK
MM58242

TL/F/7924-2

Top View
FIGURE 2

Order Number MM58242N
See NS Package Number N28B

Plastic Chip Carrier


OUTPUT 9 4
OUTPUT 10 3
OUTPUT 11 2
VSS 1
OUTPUT 12 28
OUTPUT 13 27
OUTPUT 14 26
OUTPUT 8 5
OUTPUT 7 6
OUTPUT 6 7
OUTPUT 5 8
OUTPUT 4 9
OUTPUT 3 10
OUTPUT 2 11
25 OUTPUT 15
24 OUTPUT 16
23 OUTPUT 17
22 OUTPUT 18
21 OUTPUT 19
20 OUTPUT 20
19 BLANKING CONTROL
12 OUTPUT 1
13 VDIS
14 VDD
15 CLOCK
16 DATA IN
17 DATA OUT
18 ENABLE
MM58242V

TL/F/7924-8

Top View
Order Number MM58242V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58242 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58242 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58242 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58242, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied, However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58242.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58242 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58242 is used to provide the grid drive for a 40-digit 2 line 5 × 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.

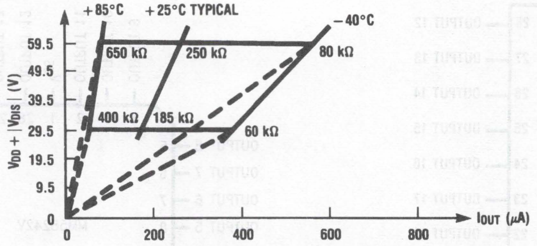


FIGURE 3a. Output Impedance Off

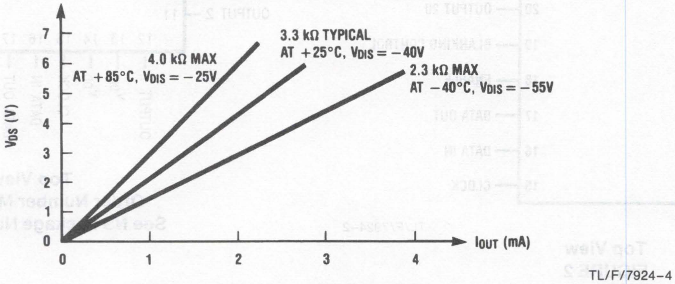
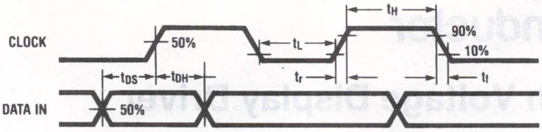


FIGURE 3b. Output Impedance On

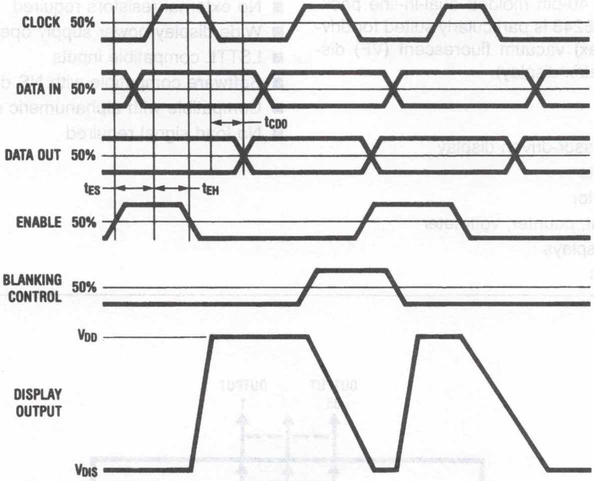
Timing Diagrams


CLOCK
50%
tH
tL
90%
10%
tDS
tDH
tr
tf
DATA IN
50%

TL/F/7924-5

For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

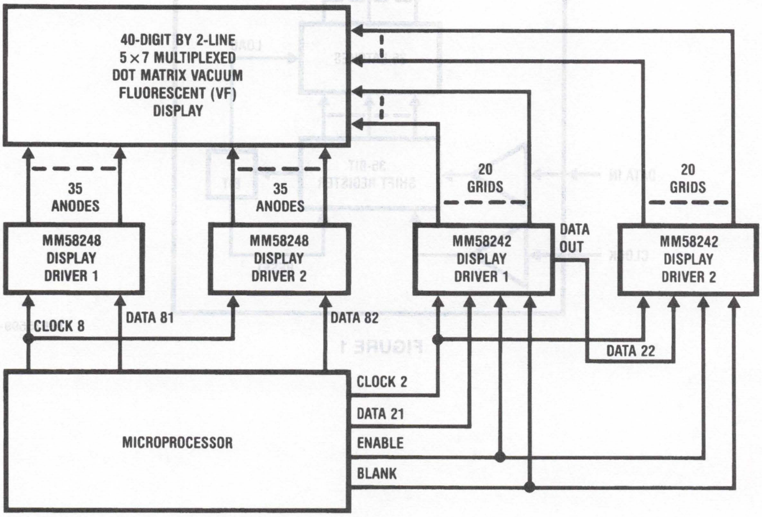
FIGURE 4. Clock and Data Timings


CLOCK 50%
DATA IN 50%
tCDO
DATA OUT 50%
tES
tEH
ENABLE 50%
BLANKING CONTROL 50%
VDD
DISPLAY OUTPUT
VDIS

TL/F/7924-6

FIGURE 5. MM58242 Timings (Data Format)

Typical Application


40-DIGIT BY 2-LINE 5×7 MULTIPLEXED DOT MATRIX VACUUM FLUORESCENT (VF) DISPLAY
35 ANODES
35 ANODES
20 GRIDS
20 GRIDS
MM58248 DISPLAY DRIVER 1
MM58248 DISPLAY DRIVER 2
MM58242 DISPLAY DRIVER 1
MM58242 DISPLAY DRIVER 2
DATA OUT
CLOCK 8
DATA 81
DATA 82
DATA 22
MICROPROCESSOR
CLOCK 2
DATA 21
ENABLE
BLANK

TL/F/7924-7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58248 High Voltage Display Driver

General Description

The MM58248 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58248 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

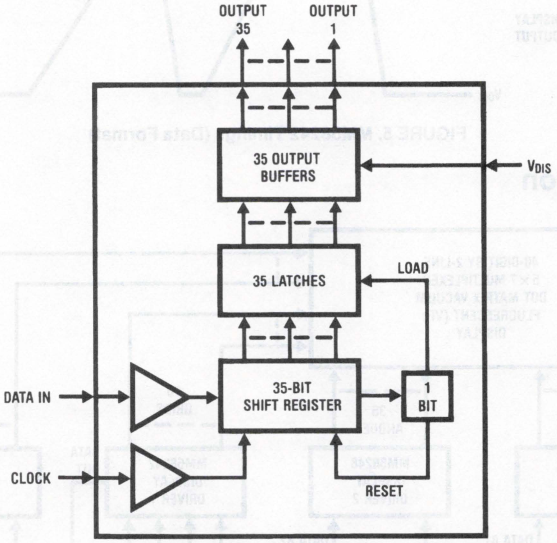
Applications

- COPS™ or microprocessor-driven display
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

Block Diagram



TL/F/5599–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 62.5V
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −55V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK Logic '1'	(Note 1)	2.4			V
I_{IN}	Input Currents, DATA IN, CLOCK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance, DATA IN, CLOCK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V				
		V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Display Output Impedances Output on *(Figure 3b)*	V_{DD} = 5.5V, V_{SS} = 0V				
		V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = −40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −55V ≤ V_{DIS} ≤ −25V	V_{DIS}		V_{DIS} + 4	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

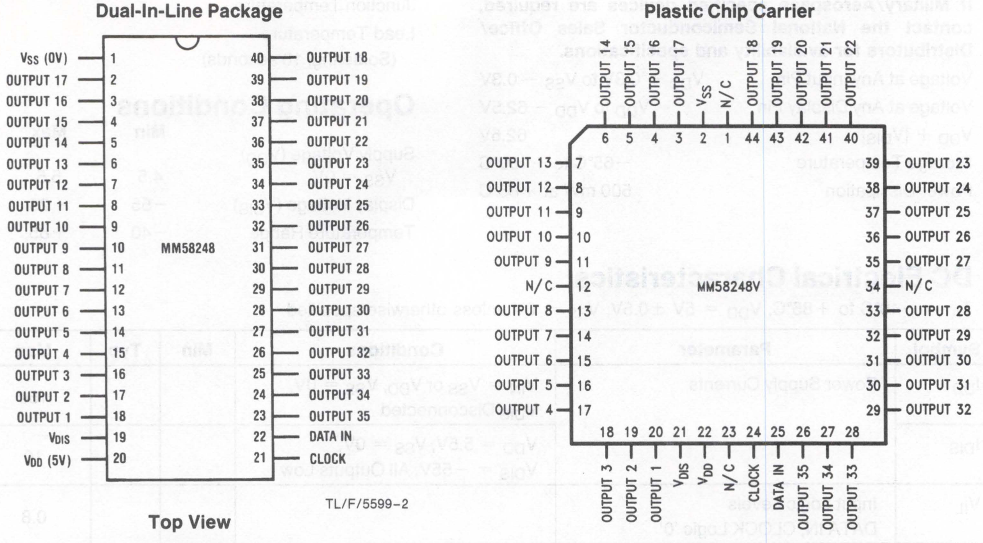
AC Electrical Characteristics T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 2, 3)			1.0	MHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time	C_L = 50 pF	100			ns
t_{DH}	Data Input Hold Time		100			ns

Note 2: AC input waveform specification for test purposes: t_r, t_f ≤ 20 ns, f = 1 MHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams



Dual-In-Line Package
VSS (0V) 1
OUTPUT 17 2
OUTPUT 16 3
OUTPUT 15 4
OUTPUT 14 5
OUTPUT 13 6
OUTPUT 12 7
OUTPUT 11 8
OUTPUT 10 9
OUTPUT 9 10
OUTPUT 8 11
OUTPUT 7 12
OUTPUT 6 13
OUTPUT 5 14
OUTPUT 4 15
OUTPUT 3 16
OUTPUT 2 17
OUTPUT 1 18
VDIS 19
VDD (5V) 20
40 OUTPUT 18
39 OUTPUT 19
38 OUTPUT 20
37 OUTPUT 21
36 OUTPUT 22
35 OUTPUT 23
34 OUTPUT 24
33 OUTPUT 25
32 OUTPUT 26
31 OUTPUT 27
30 OUTPUT 28
29 OUTPUT 29
28 OUTPUT 30
27 OUTPUT 31
26 OUTPUT 32
25 OUTPUT 33
24 OUTPUT 34
23 OUTPUT 35
22 DATA IN
21 CLOCK
MM58248
TL/F/5599-2
Plastic Chip Carrier
6 OUTPUT 14
5 OUTPUT 15
4 OUTPUT 16
3 OUTPUT 17
2 VSS
1 N/C
44 OUTPUT 18
43 OUTPUT 19
42 OUTPUT 20
41 OUTPUT 21
40 OUTPUT 22
OUTPUT 13 7
OUTPUT 12 8
OUTPUT 11 9
OUTPUT 10 10
OUTPUT 9 11
N/C 12
OUTPUT 8 13
OUTPUT 7 14
OUTPUT 6 15
OUTPUT 5 16
OUTPUT 4 17
39 OUTPUT 23
38 OUTPUT 24
37 OUTPUT 25
36 OUTPUT 26
35 OUTPUT 27
34 N/C
33 OUTPUT 28
32 OUTPUT 29
31 OUTPUT 30
30 OUTPUT 31
29 OUTPUT 32
18 OUTPUT 3
19 OUTPUT 2
20 OUTPUT 1
21 VDIS
22 VDD
23 N/C
24 CLOCK
25 DATA IN
26 OUTPUT 35
27 OUTPUT 34
28 OUTPUT 33
MM58248V
TL/F/5599-8

Top View

Order Number MM58248N
See NS Package Number N40A

Top View

Order Number MM58248V
See NS Package Number V44A

FIGURE 2

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58248 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58248 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58248 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following the start bit. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by the use of the MM58248, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

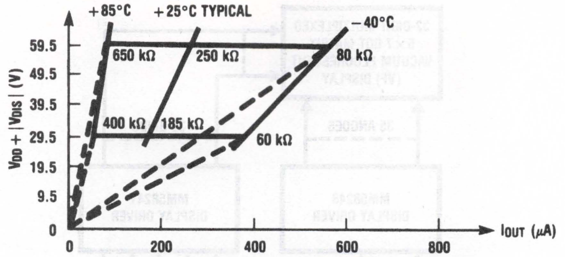
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58248.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'–'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58248, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 'zeroes', followed by a 'one' (start bit), followed by 35 'zeroes'. This procedure will completely blank the display.

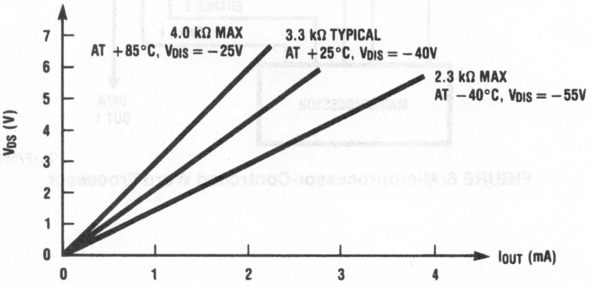
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58248 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58241, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

Functional Description (Continued)



TL/F/5599-3

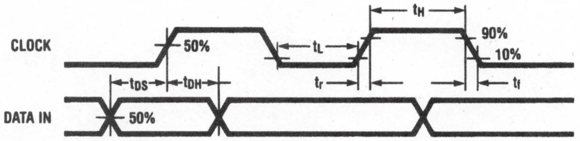
FIGURE 3a. Output Impedance Off



TL/F/5599-4

FIGURE 3b. Output Impedance On

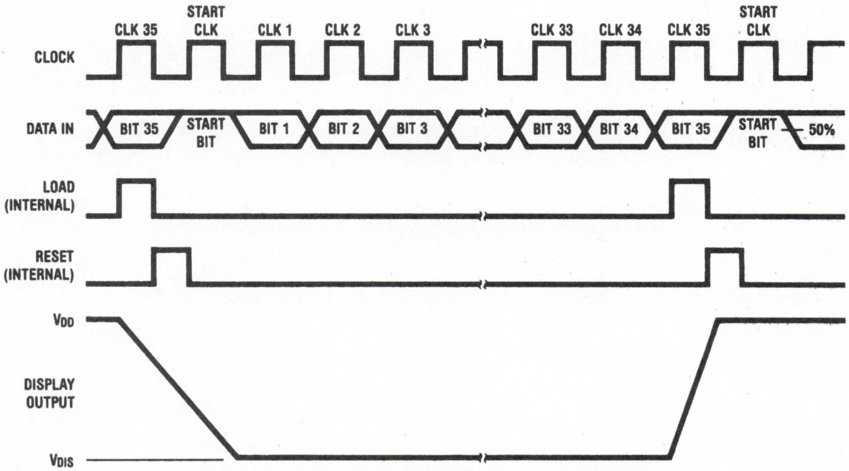
Timing Diagrams


CLOCK
DATA IN
50%
tL
tH
90%
10%
tDS
tDH
tr
tf
50%

TL/F/5599-5

For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

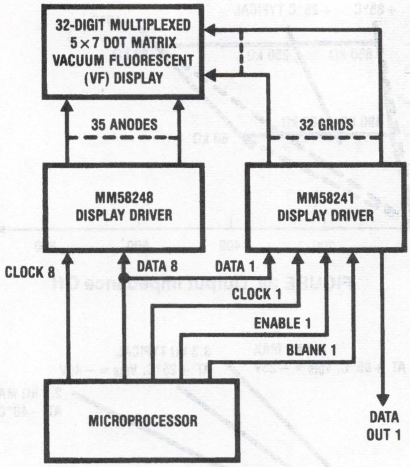
FIGURE 4. Clock and Data Timings


START CLK
CLK 35
CLK 1
CLK 2
CLK 3
CLK 33
CLK 34
CLK 35
START CLK
CLOCK
DATA IN
BIT 35
START BIT
BIT 1
BIT 2
BIT 3
BIT 33
BIT 34
BIT 35
START BIT
50%
LOAD (INTERNAL)
RESET (INTERNAL)
VDD
DISPLAY OUTPUT
VDIS

TL/F/5599-6

FIGURE 5. MM58248 Timings (Data Format)

Typical Applications


32-DIGIT MULTIPLEXED
5×7 DOT MATRIX
VACUUM FLUORESCENT
(VF) DISPLAY
35 ANODES
32 GRIDS
MM58248
DISPLAY DRIVER
MM58241
DISPLAY DRIVER
CLOCK 8
DATA 8
DATA 1
CLOCK 1
ENABLE 1
BLANK 1
MICROPROCESSOR
DATA
OUT 1

TL/F/5599-7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

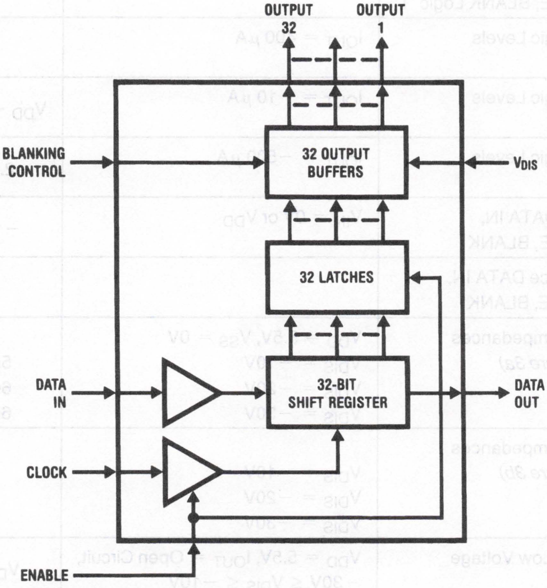
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram


OUTPUT 32
OUTPUT 1
BLANKING CONTROL
32 OUTPUT BUFFERS
V_{DIS}
32 LATCHES
DATA IN
32-BIT SHIFT REGISTER
DATA OUT
CLOCK
ENABLE

TL/F/5603-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 36.5V
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −30V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '1'	(Note 1)	2.4			V
V_{OH}	Data Output Logic Levels Logic '0'	I_{OUT} = 400 μA			0.4	V
V_{OH}	Data Output Logic Levels Logic '1'	I_{OUT} = −10 μA	V_{DD} − 0.5			V
V_{OH}	Data Output Logic Levels Logic '1'	I_{OUT} = −500 μA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V	 55 60 65		 250 300 400	 kΩ kΩ kΩ
R_{ON}	Display Output Impedances Output On *(Figure 3b)*	V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V		700 600 500	800 750 680	Ω Ω Ω
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −30V ≤ V_{DIS} ≤ −10V	V_{DIS}		V_{DIS} + 2	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 3, 4)			800	kHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time		100			ns
t_{DH}	Data Input Hold Time		100			ns
t_{ES}	Enable Input Setup Time		100			ns
t_{EH}	Enable Input Hold Time		100			ns
t_{CDO}	Data Output Clock Low to Data Out Time	$C_L = 50$ pF			500	ns

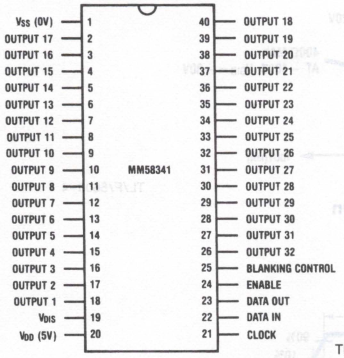
Note 2: Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package

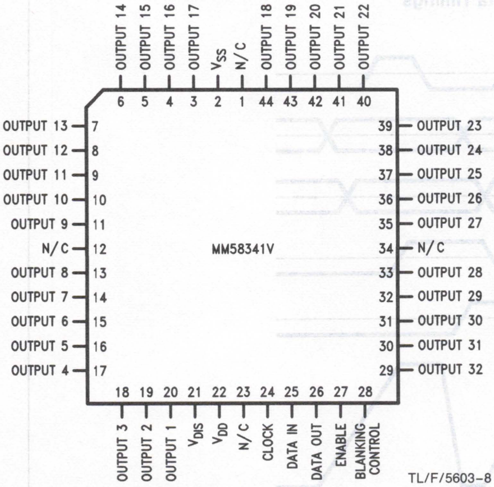

VSS (0V) 1
OUTPUT 17 2
OUTPUT 16 3
OUTPUT 15 4
OUTPUT 14 5
OUTPUT 13 6
OUTPUT 12 7
OUTPUT 11 8
OUTPUT 10 9
OUTPUT 9 10
OUTPUT 8 11
OUTPUT 7 12
OUTPUT 6 13
OUTPUT 5 14
OUTPUT 4 15
OUTPUT 3 16
OUTPUT 2 17
OUTPUT 1 18
VDIS 19
VDD (5V) 20
MM58341
40 OUTPUT 18
39 OUTPUT 19
38 OUTPUT 20
37 OUTPUT 21
36 OUTPUT 22
35 OUTPUT 23
34 OUTPUT 24
33 OUTPUT 25
32 OUTPUT 26
31 OUTPUT 27
30 OUTPUT 28
29 OUTPUT 29
28 OUTPUT 30
27 OUTPUT 31
26 OUTPUT 32
25 BLANKING CONTROL
24 ENABLE
23 DATA OUT
22 DATA IN
21 CLOCK

TL/F/5603-2

Top View

Order Number MM58341N
See NS Package Number N40A

Plastic Chip Carrier


OUTPUT 14 6
OUTPUT 15 5
OUTPUT 16 4
OUTPUT 17 3
VSS 2
N/C 1
OUTPUT 18 44
OUTPUT 19 43
OUTPUT 20 42
OUTPUT 21 41
OUTPUT 22 40
OUTPUT 13 7
OUTPUT 12 8
OUTPUT 11 9
OUTPUT 10 10
OUTPUT 9 11
N/C 12
OUTPUT 8 13
OUTPUT 7 14
OUTPUT 6 15
OUTPUT 5 16
OUTPUT 4 17
MM58341V
39 OUTPUT 23
38 OUTPUT 24
37 OUTPUT 25
36 OUTPUT 26
35 OUTPUT 27
34 N/C
33 OUTPUT 28
32 OUTPUT 29
31 OUTPUT 30
30 OUTPUT 31
29 OUTPUT 32
18 OUTPUT 3
19 OUTPUT 2
20 OUTPUT 1
21 VDIS
22 VDD
23 N/C
24 CLOCK
25 DATA IN
26 DATA OUT
27 ENABLE
28 BLANKING CONTROL

TL/F/5603-8

Top View

Order Number MM58341V
See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

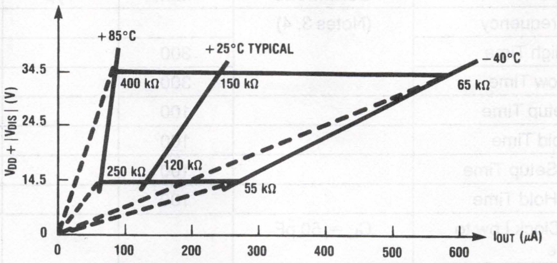
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

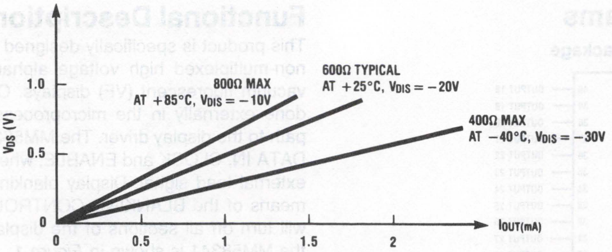
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58341 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

Functional Decription (Continued)



TL/F/5603-3

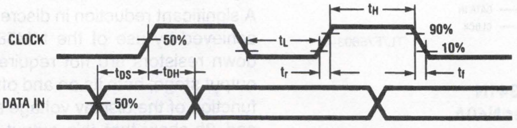
FIGURE 3a. Output Impedance Off



TL/F/5603-4

FIGURE 3b. Output Impedance On

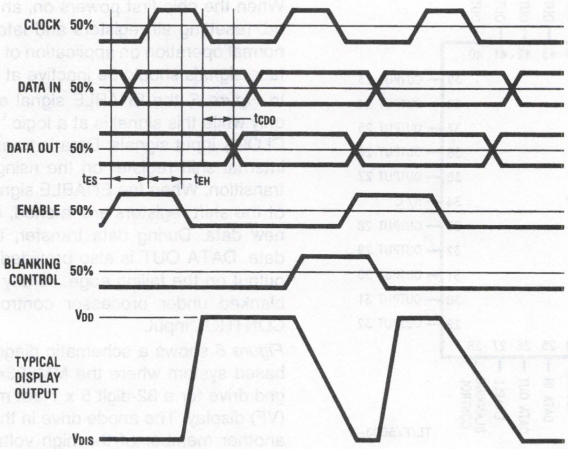
Timing Diagrams


CLOCK
50%
t_H
90%
10%
t_L
t_r
t_f
t_{DS}
t_{DH}
DATA IN
50%

TL/F/5603-5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

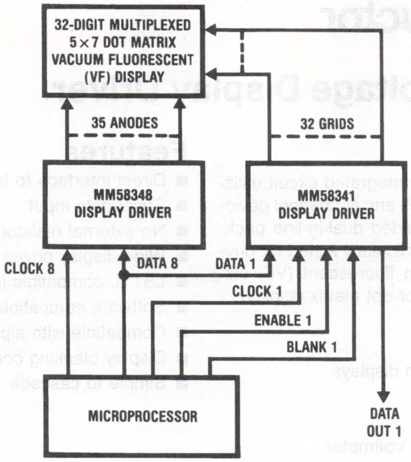
FIGURE 4. Clock and Data Timings


CLOCK 50%
DATA IN 50%
t_{CDO}
DATA OUT 50%
t_{ES}
t_{EH}
ENABLE 50%
BLANKING CONTROL 50%
V_{DD}
TYPICAL DISPLAY OUTPUT
V_{DIS}

TL/F/5603-6

FIGURE 5. MM58341 Timings (Data Format)

Typical Application


32-DIGIT MULTIPLEXED
5×7 DOT MATRIX
VACUUM FLUORESCENT
(VF) DISPLAY
35 ANODES
32 GRIDS
MM58348
DISPLAY DRIVER
MM58341
DISPLAY DRIVER
CLOCK 8
DATA 8
DATA 1
CLOCK 1
ENABLE 1
BLANK 1
MICROPROCESSOR
DATA
OUT 1

TL/F/5603-7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58342 High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

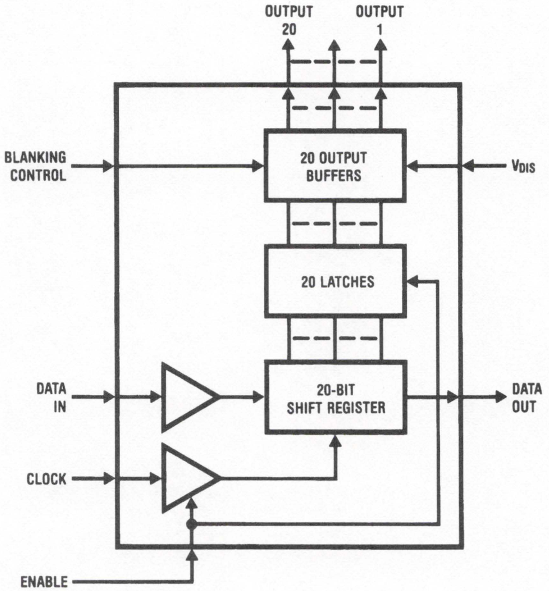
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram


OUTPUT 20
OUTPUT 1
BLANKING CONTROL
20 OUTPUT BUFFERS
V_{DIS}
20 LATCHES
DATA IN
20-BIT SHIFT REGISTER
DATA OUT
CLOCK
ENABLE

TL/F/7925-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 36.5V
$V_{DD} + \lvert V_{DIS}\rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN} = V_{SS}$ or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −30V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 μA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 μA	V_{DD} − 0.5			V
V_{OH}	Logic '1'	I_{OUT} = −500 μA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off (*Figure 3a*)	V_{DIS} = −10V	55		250	kΩ
		V_{DIS} = −20V	60		300	kΩ
		V_{DIS} = −30V	65		400	kΩ
R_{ON}	Output On (*Figure 3b*)	V_{DIS} = −10V		700	800	Ω
		V_{DIS} = −20V		600	750	Ω
		V_{DIS} = −30V		500	680	Ω
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −30V ≤ V_{DIS} ≤ −10V	V_{DIS}		V_{DIS} + 2	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input	(Note 2)				
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50$ pF				
t_{CDO}	CLOCK Low to Data Out Time				500	ns

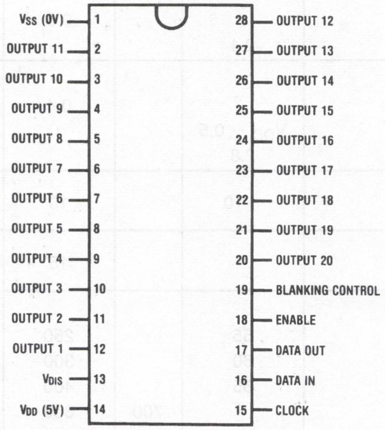
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 µs.

Connection Diagrams

Dual-In-Line Package


VSS (0V) 1
OUTPUT 11 2
OUTPUT 10 3
OUTPUT 9 4
OUTPUT 8 5
OUTPUT 7 6
OUTPUT 6 7
OUTPUT 5 8
OUTPUT 4 9
OUTPUT 3 10
OUTPUT 2 11
OUTPUT 1 12
VDIS 13
VDD (5V) 14
28 OUTPUT 12
27 OUTPUT 13
26 OUTPUT 14
25 OUTPUT 15
24 OUTPUT 16
23 OUTPUT 17
22 OUTPUT 18
21 OUTPUT 19
20 OUTPUT 20
19 BLANKING CONTROL
18 ENABLE
17 DATA OUT
16 DATA IN
15 CLOCK

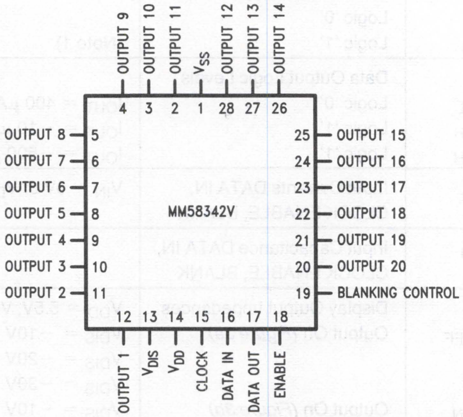
TL/F/7925-2

Top View

FIGURE 2

Order Number MM58342N
See NS Package Number N28B

Plastic Chip Carrier


OUTPUT 9
OUTPUT 10
OUTPUT 11
VSS
OUTPUT 12
OUTPUT 13
OUTPUT 14
4 3 2 1 28 27 26
OUTPUT 8 5
OUTPUT 7 6
OUTPUT 6 7
OUTPUT 5 8
OUTPUT 4 9
OUTPUT 3 10
OUTPUT 2 11
MM58342V
25 OUTPUT 15
24 OUTPUT 16
23 OUTPUT 17
22 OUTPUT 18
21 OUTPUT 19
20 OUTPUT 20
19 BLANKING CONTROL
12 13 14 15 16 17 18
OUTPUT 1
VDIS
VDD
CLOCK
DATA IN
DATA OUT
ENABLE

TL/F/7925-8

Top View
Order Number MM58342V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58342 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58342 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58342 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58342, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a*

Functional Description (Continued)

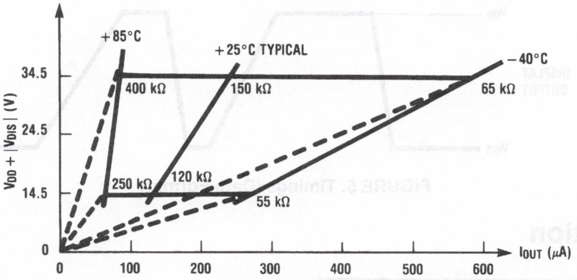
and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58342.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

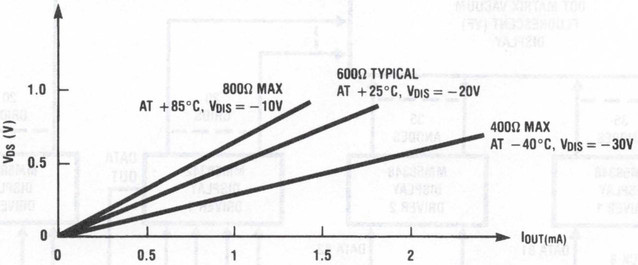
In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58342 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58342 is used to provide the grid drive for a 40-digit 2 line 5 x 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.



TL/F/7925-3

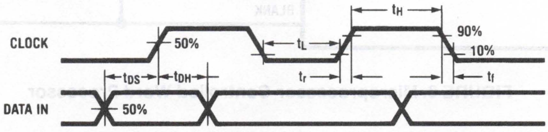
FIGURE 3a. Output Impedance Off



TL/F/7925-4

FIGURE 3b. Output Impedance On

Timing Diagrams

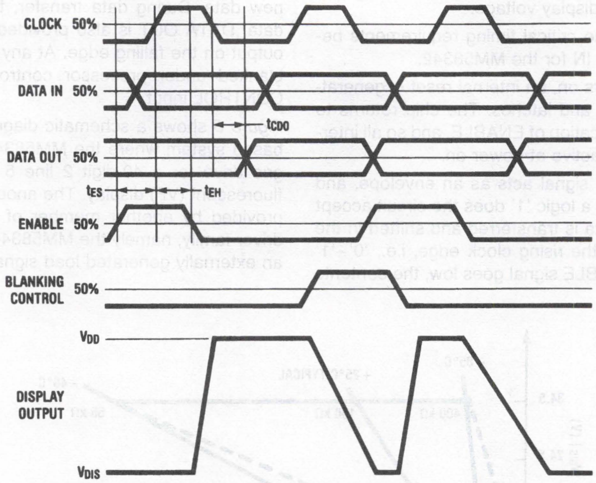


TL/F/7925-5

For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

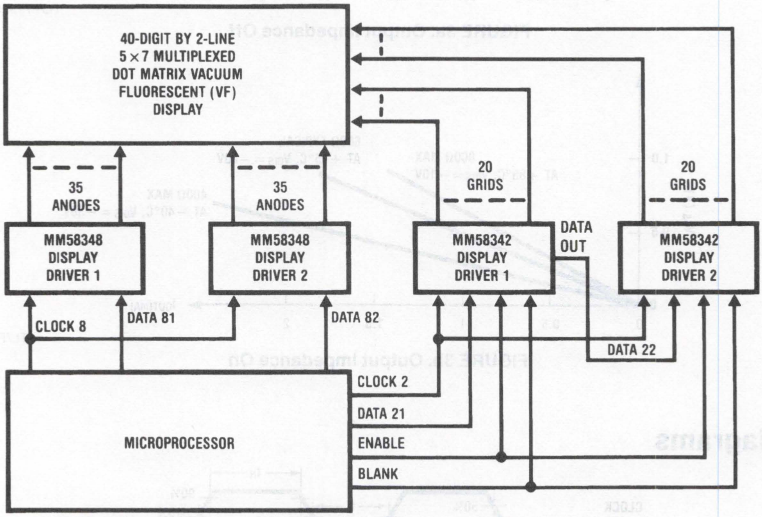
Timing Diagrams (Continued)


CLOCK 50%
DATA IN 50%
tCDO
DATA OUT 50%
tES
tEH
ENABLE 50%
BLANKING CONTROL 50%
VDD
DISPLAY OUTPUT
VDIS

TL/F/7925-6

FIGURE 5. Timings (Data Format)

Typical Application


40-DIGIT BY 2-LINE 5×7 MULTIPLEXED DOT MATRIX VACUUM FLUORESCENT (VF) DISPLAY
35 ANODES
35 ANODES
20 GRIDS
20 GRIDS
MM58348 DISPLAY DRIVER 1
MM58348 DISPLAY DRIVER 2
MM58342 DISPLAY DRIVER 1
MM58342 DISPLAY DRIVER 2
DATA OUT
CLOCK 8
DATA 81
DATA 82
DATA 22
MICROPROCESSOR
CLOCK 2
DATA 21
ENABLE
BLANK

TL/F/7925-7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58348 High Voltage Display Driver

General Description

The MM58348 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58348 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

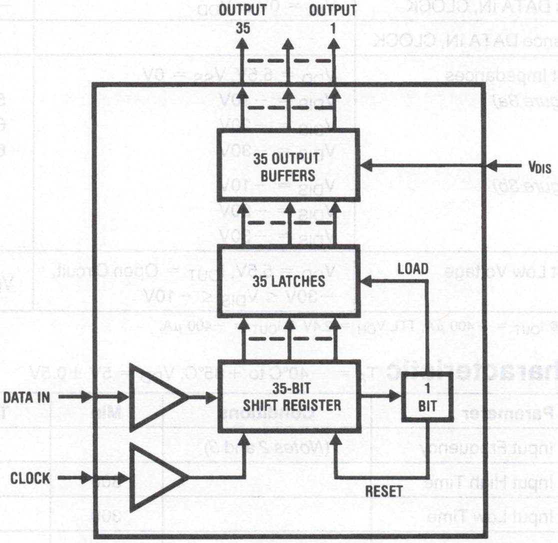
Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Block Diagram



TL/F/5601-1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 36.5V
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −30V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK Logic '0'				0.8	V
V_{IH}	Logic '1'		2.4			V
I_{IN}	Input Currents DATA IN, CLOCK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V	 55 60 65		 250 300 400	 kΩ kΩ kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V		700 600 500	800 750 680	Ω Ω Ω
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −30V ≤ V_{DIS} ≤ −10V	V_{DIS}		V_{DIS} + 2	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristic T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V

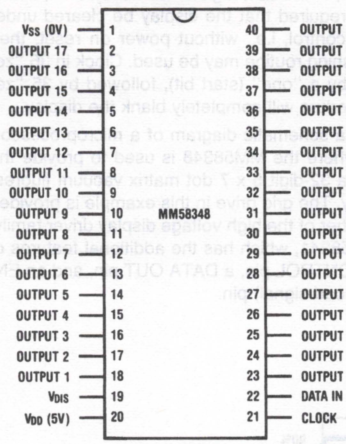
Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	*(Notes 2* and *3)*			1.0	MHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Set-Up Time		100			ns
t_{DH}	Data Input Hold Time		100			ns

Note 2: AC input waveform specification for test purpose: t_r ≤ 20 ns, t_f ≤ 20 ns, f = 1 MHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package


VSS (0V) 1
OUTPUT 17 2
OUTPUT 16 3
OUTPUT 15 4
OUTPUT 14 5
OUTPUT 13 6
OUTPUT 12 7
OUTPUT 11 8
OUTPUT 10 9
OUTPUT 9 10
OUTPUT 8 11
OUTPUT 7 12
OUTPUT 6 13
OUTPUT 5 14
OUTPUT 4 15
OUTPUT 3 16
OUTPUT 2 17
OUTPUT 1 18
VDIS 19
VDD (5V) 20
40 OUTPUT 18
39 OUTPUT 19
38 OUTPUT 20
37 OUTPUT 21
36 OUTPUT 22
35 OUTPUT 23
34 OUTPUT 24
33 OUTPUT 25
32 OUTPUT 26
31 OUTPUT 27
30 OUTPUT 28
29 OUTPUT 29
28 OUTPUT 30
27 OUTPUT 31
26 OUTPUT 32
25 OUTPUT 33
24 OUTPUT 34
23 OUTPUT 35
22 DATA IN
21 CLOCK
MM58348

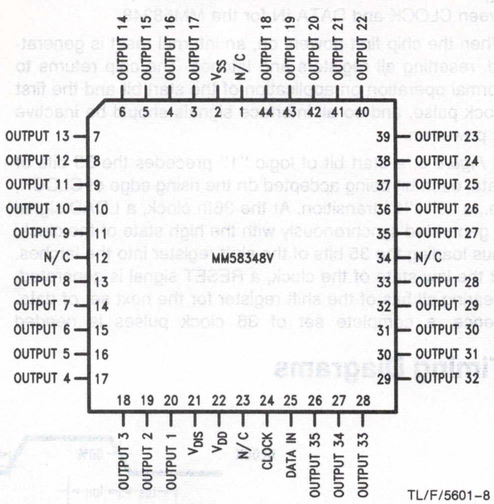
TL/F/5601-2

Top View

FIGURE 2

Order Number MM58348N
See NS Package Number N40A

Plastic Chip Carrier


OUTPUT 14 6
OUTPUT 15 5
OUTPUT 16 4
OUTPUT 17 3
VSS 2
N/C 1
OUTPUT 18 44
OUTPUT 19 43
OUTPUT 20 42
OUTPUT 21 41
OUTPUT 22 40
OUTPUT 13 7
OUTPUT 12 8
OUTPUT 11 9
OUTPUT 10 10
OUTPUT 9 11
N/C 12
OUTPUT 8 13
OUTPUT 7 14
OUTPUT 6 15
OUTPUT 5 16
OUTPUT 4 17
39 OUTPUT 23
38 OUTPUT 24
37 OUTPUT 25
36 OUTPUT 26
35 OUTPUT 27
34 N/C
33 OUTPUT 28
32 OUTPUT 29
31 OUTPUT 30
30 OUTPUT 31
29 OUTPUT 32
18 OUTPUT 3
19 OUTPUT 2
20 OUTPUT 1
21 VDIS
22 VDD
23 N/C
24 CLOCK
25 DATA IN
26 OUTPUT 35
27 OUTPUT 34
28 OUTPUT 33
MM58348V

TL/F/5601-8

Top View

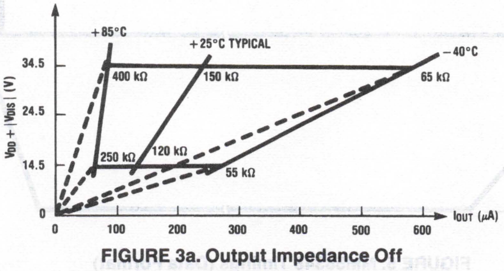
Order Number MM58348V
See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58348 uses two signals, DATA IN and CLOCK, with a format of a leading "1" followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58348 is shown in *Figure 1*.

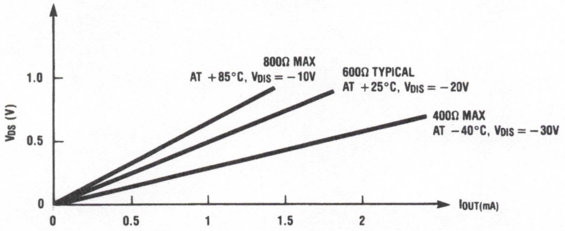
Figure 2 shows the pinout of the MM58348 device, where output 1 (pin 18) is equivalent to bit 1, (i.e., the first bit of data to be loaded into the shift register following the start bit). A logic "1" at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58348, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figure 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.



TL/F/5601-3

FIGURE 3a. Output Impedance Off



TL/F/5601-4

FIGURE 3b. Output Impedance On

Functional Description (Continued)

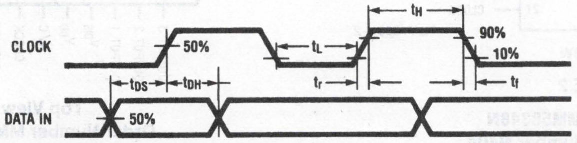
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58348.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic "1" precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a "0"-"1" transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58348, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 "zeroes", followed by a "one" (start bit), followed by 35 "zeroes". This procedure will completely blank the display.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58348 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58341, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

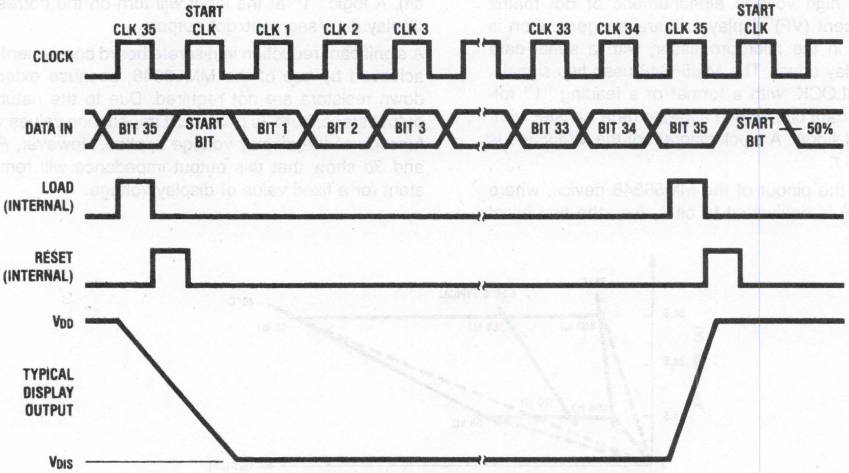
Timing Diagrams


tH
90%
CLOCK
50%
tL
10%
tDS
tDH
tr
tf
DATA IN
50%

TL/F/5601-5

For the purpose of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

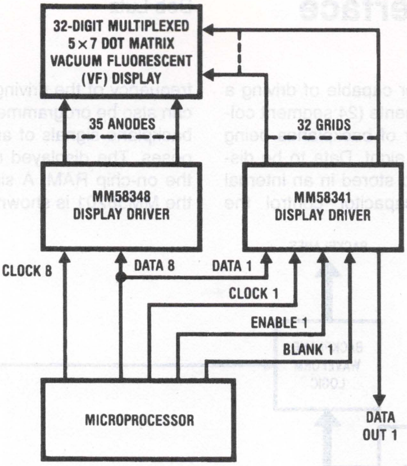
FIGURE 4. Clock and Data Timings


CLK 35
START CLK
CLK 1
CLK 2
CLK 3
CLK 33
CLK 34
CLK 35
START CLK
CLOCK
DATA IN
BIT 35
START BIT
BIT 1
BIT 2
BIT 3
BIT 33
BIT 34
BIT 35
START BIT
50%
LOAD (INTERNAL)
RESET (INTERNAL)
VDD
TYPICAL DISPLAY OUTPUT
VDIS

TL/F/5601-6

FIGURE 5. MM58348 Timings (Data Format)

Typical Application


32-DIGIT MULTIPLEXED
5 × 7 DOT MATRIX
VACUUM FLUORESCENT
(VF) DISPLAY
35 ANODES
32 GRIDS
MM58348
DISPLAY DRIVER
MM58341
DISPLAY DRIVER
CLOCK 8
DATA 8
DATA 1
CLOCK 1
ENABLE 1
BLANK 1
MICROPROCESSOR
DATA
OUT 1

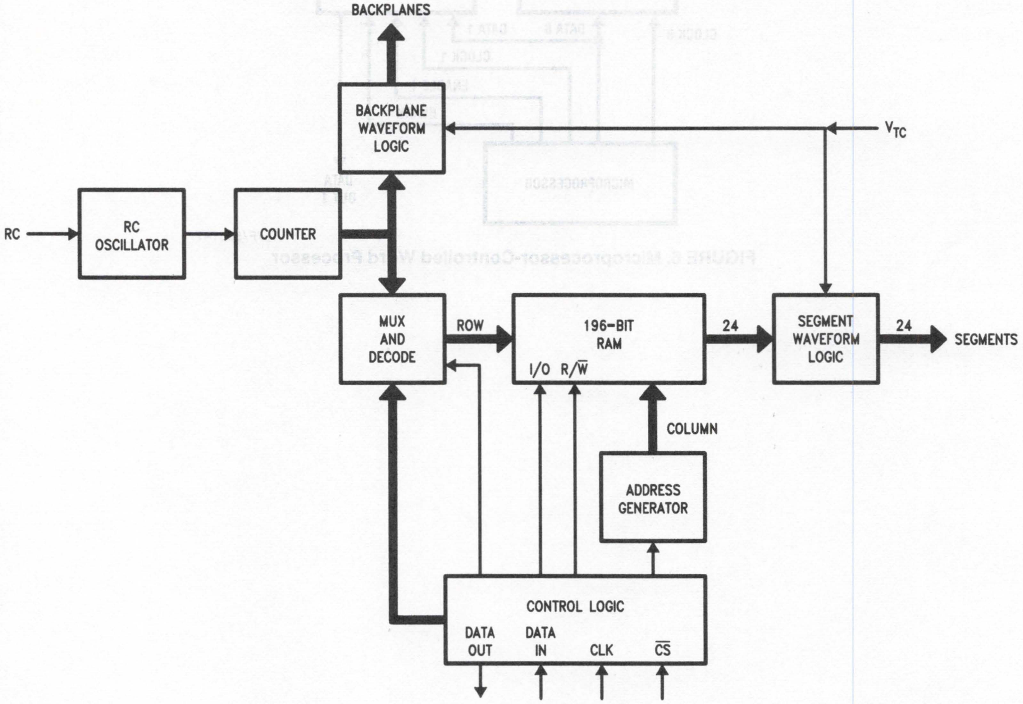
TL/F/5601-7

FIGURE 6. Microprocessor-Controlled Word Processor

Designing an LCD Dot Matrix Display Interface

National Semiconductor
Application Note 350
Bob Lutz

The MM58201 is a CMOS LCD driver capable of driving a multiplexed display of up to 192 segments (24 segment columns by 8 backplanes). The number of backplanes being driven is programmable from one to eight. Data to be displayed is sent to the chip serially and stored in an internal RAM. An external resistor and capacitor control the frequency of the driving signals to the LCD. The MM58201 can also be programmed to accept the oscillator output and backplane signals of another MM58201 for cascading purposes. The displayed data may also be read serially from the on-chip RAM. A simplified functional block diagram of the MM58201 is shown in *Figure 1*.


BACKPLANES
BACKPLANE WAVEFORM LOGIC
V_{TC}
RC
RC OSCILLATOR
COUNTER
MUX AND DECODE
ROW
196-BIT RAM
I/O
R/$\overline{W}$
24
SEGMENT WAVEFORM LOGIC
24
SEGMENTS
COLUMN
ADDRESS GENERATOR
CONTROL LOGIC
DATA OUT
DATA IN
CLK
$\overline{CS}$

TL/B/5606–1

FIGURE 1. MM58201 Functional Diagram

BACKGROUND

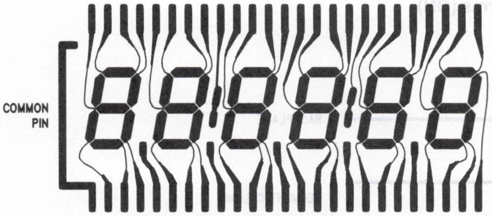
LCD displays have become very popular because of their ultra-low power consumption and high contrast ratio under high ambient light levels. Typically an LCD has a backplane that overlaps the entire display area and multiple segment lines that each overlap just one segment or descriptor. This means that a separate external connection is needed for every segment or descriptor as shown in *Figure 2*. For a display with many segments such as a dot matrix display, the number of external connections could easily grow to be very large.

Unlike other display technologies that respond to peak or average voltage and current, LCDs are sensitive to the rms voltage between the backplane and given segment location. Also, any DC bias across this junction would cause an irreversible electrochemical action that would shorten the life of the display. A typical LCD driving signal is shown in *Figure 3*. The backplane signal is simply a symmetrical square wave. The individual segment outputs are also square waves, either in phase with the backplane for an "off" segment or out of phase for an "on" segment. This causes a Vrms of zero for an "off" segment and a Vrms of +V for an "on" segment.

One way to reduce the number of external connections is to multiplex the display. An example of this could be an LCD with its segments arranged as intersections of an X-Y grid. A driver to control a matrix like this would be fairly straightforward for an LED display. However, it is more complex for an LCD because of the DC bias restriction.

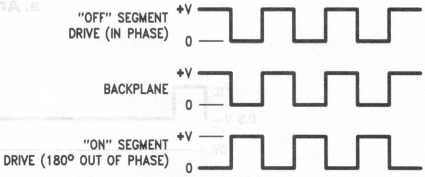
A multiplexed LCD driver must generate a complex set of output signals to insure that an "on" segment sees an rms voltage greater than the display's turn-on voltage and that an "off" segment sees an rms voltage less than the display's turn-off voltage. The driver must also insure that there is no DC bias.

One pattern that can accomplish this is shown as an example in *Figure 4*. This is the pattern that the MM58201 uses. The actual Vrms of an "on" segment and an "off" segment is shown in *Figure 5*. If there are eight backplanes, the Vrms (ON) = 0.2935 × V_{TC} and the Vrms (OFF) = 0.2029 × V_{TC}. It can be seen in *Figure 6* that as the number of backplanes increases, the difference between Vrms (ON) and Vrms (OFF) becomes less. Refer to the specifications of the LCD to determine exactly what Vrms is required.



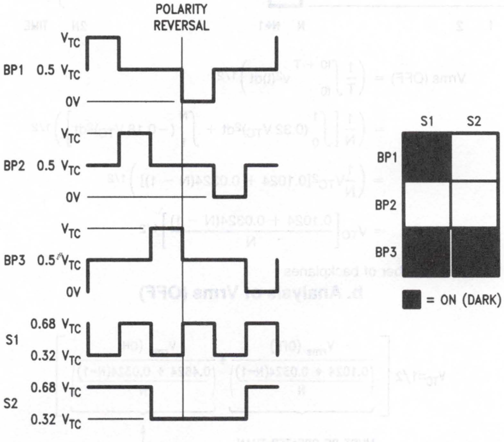
TL/B/5606-2

FIGURE 2. Typical LCD Pin Connections


"OFF" SEGMENT DRIVE (IN PHASE)
+V
0
BACKPLANE
+V
0
"ON" SEGMENT DRIVE (180° OUT OF PHASE)
+V
0

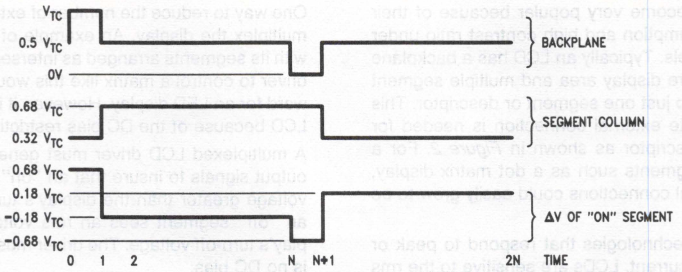
TL/B/5606-3

FIGURE 3. Drive Signals from a Direct Connect LCD Driver



TL/B/5606-4

FIGURE 4. Example of Backplane and Segment Patterns



TL/B/5606-5

$$\text{Vrms (ON)} = \left(\frac{1}{T}\int_{t0}^{t0+T} v^2(t)dt\right)^{1/2}$$

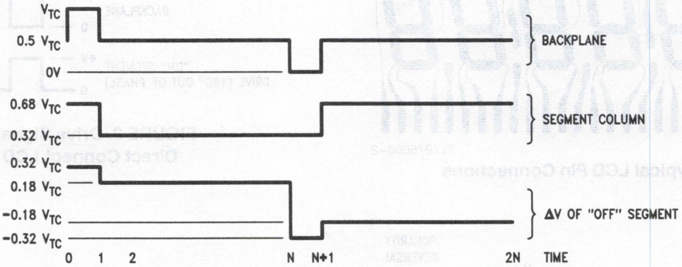
$$= \left(\frac{1}{N}\left[\int_0^1 (0.68\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}{}^2[0.4624 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.4624 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

a. Analysis of Vrms (ON)



TL/B/5606-6

$$\text{Vrms (OFF)} = \left(\frac{1}{T}\int_{t0}^{t0+T} v^2(t)dt\right)^{1/2}$$

$$= \left(\frac{1}{N}\left[\int_0^1 (0.32\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}{}^2[0.1024 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.1024 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

b. Analysis of Vrms (OFF)

$$V_{TC} = 1/2\left[\underbrace{\frac{V_{rms}\ (OFF)}{\left(\frac{0.1024 + 0.0324(N-1)}{N}\right)}} + \underbrace{\frac{V_{rms}\ (ON)}{\left(\frac{0.4624 + 0.0324(N-1)}{N}\right)}}\right]$$

MUST BE GREATER THAN

TL/B/5606-7

Example: If N = 8
and Vrms (OFF) = 1.8V
and Vrms (ON) = 2.2V
then V_{TC} = 7.5V

FIGURE 5

FUNCTIONAL DESCRIPTION

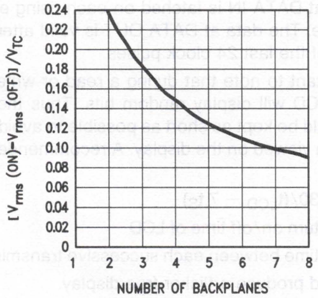
Connecting an MM58201 to an LCD

The backplane and segment outputs of the MM58201 connect directly to the backplane and segment lines of the LCD. These outputs are designed to drive a display with a total "on" capacitance of up to 2000 pF. This is especially important for the backplane outputs, as it is usually the backplanes that have the most capacitance. As the capacitance of the output lines increases, the DC offset between a backplane and segment signal may increase. Most LCD displays specify that a maximum offset of 50 mV is acceptable. For backplane capacitance under 2000 pF the MM58201 guarantees an offset of less than 10 mV.

If the LCD display to be used has 24 segments per backplane or less, then each MM58201 should be configured as a "master" so that each one will generate its own set of backplane signals. However, if the LCD display has more than 24 segments per backplane, more than one MM58201 will be needed for each backplane. To synchronize the driving signals there must be one "master" chip and then an additional "slave" chip for every 24 segments after the first 24. When a chip is configured as a "slave" it does not generate its own backplane signals. It simply synchonizes itself to the backplane signals generated by a "master" chip by sensing the BP1 signal. An example of both an all "master" configuration and a "master-slave" configuration will be shown later.

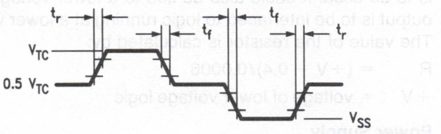
Voltage Control Pin and Circuitry

The voltage presented at the V_{TC} pin determines the actual voltage that is output on the backplane and segment lines. These voltages are shown in *Figure 7*. V_{TC} should be set with respect to Vrms (ON) and Vrms (OFF) and can be calculated as shown in *Figure 5*.



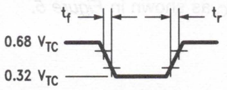
TL/B/5606-8

FIGURE 6. ΔVrms/V_{TC}



TL/B/5606-9

a. Backplane Output

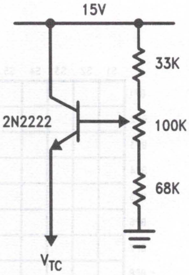


TL/B/5606-10

b. Segment Output

FIGURE 7. Output Voltages

Since the input impedance of V_{TC} may vary between 10 kΩ and 30 kΩ, the output impedance of the voltage reference at V_{TC} should be relatively low. One example of a V_{TC} driver is shown in *Figure 8*. To put the MM58201 in a standby mode, bring V_{TC} to V_{SS} (ground). This will blank out the display and reduce the supply current to less than 300 μA.



TL/B/5606-11

FIGURE 8. Example of V_{TC} Driver

RC Oscillator

This oscillator works with an external resistor tied to V_{DD} and an external capacitor tied to V_{SS}. The frequency of oscillation is related to the external R and C by:

$$f_{OSC} = 1/1.25\ RC \pm 30\%$$

The value of the external resistor should be in the range from 10 kΩ to 1 MΩ. The value of the external capacitor should be less than 0.005 μF.

The oscillator generates the timing required for multiplexing the LCD. The frequency of the oscillator is 4N times the refresh rate of the display, where N is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency should be:

$$128N < f_{OSC} < 400N$$

If the frequency is too slow, there will be a noticeable flicker in the display. If the frequency is too fast, there will be a loss of contrast between segments and an increase in power consumption.

Serial Input and Output

Data is sent to the MM58201 serially through the DATA IN pin. Each transmission must consist of 30 bits of information, as shown in *Figure 9*. The first five bits are the address, MSB first, of the first column of LCD segments that are to be changed. The next bit is a read or write flag. The following 24 bits are the actual data to be displayed.

The address specifies the first LCD column that is going to be affected. The columns are numbered as shown in *Figure 10*. Data is always written in three column chunks. Twenty-four bits of data must always be sent, even if some of the backplanes are not in use. The starting column can be any number between one (00000) and twenty-four (10111). If column 23 or 24 is specified the displayed data will wrap around to column 1.

If the $R/\overline{W}$ bit is a "0" then the specified columns of the LCD will be overwritten with the new data. If the bit is a "1" then the data displayed in the specified columns will be available serially at the DATA OUT pin and the display will not be changed.

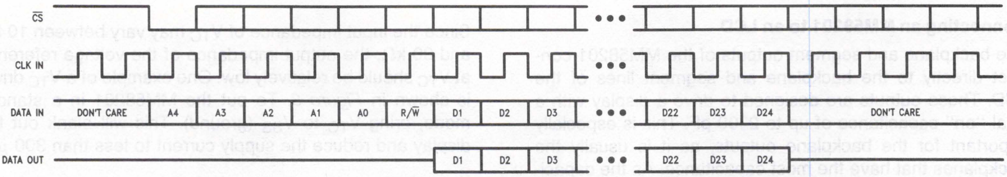


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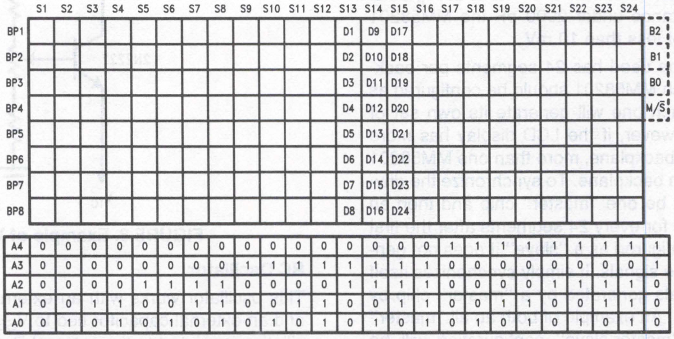
FIGURE 9. Transmission of Data



A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

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Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

FIGURE 10. Address of Particular Segment Columns

The data is formatted as shown in *Figure 10*. The first bit in the data stream corresponds to backplane 1 in the first specified column. The second bit corresponds to backplane 2 in the first specified column and so on.

During initialization each MM58201 must be programmed to select how many backplanes are to be used, and whether the chip is to be a "master" or a "slave". The format of this transmission is just like a regular data transmission except for the following: the address must be 11000; the R/$\overline{\text{W}}$ must be a write (0); the first three data bits must be selected from the list in Table I. The next bit should be a "1" for the chip to be a master or a "0" for the chip to be a slave. The following 20 bits are necessary to complete the transmission but they will be ignored. The mode cannot be read back from the chip.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	0
3	0	1	0
4	0	0	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

The timing of the CLK, $\overline{\text{CS}}$, DATA IN, and DATA OUT are illustrated in *Figure 11*. The frequency of the clock can be between DC and 100 kHz with the shortest half-period being 5.0 μs. A transmission is initiated by $\overline{\text{CS}}$ going low. $\overline{\text{CS}}$ can then be raised anytime after the rising edge of the first clock pulse and before the rising edge of the last clock pulse (the clock edge that reads in D24). 30 bits of information must always be sent.

The data at DATA IN is latched on each rising edge of the clock pulse. The data at DATA OUT is valid after each falling edge of the last 24 clock pulses.

It is important to note that during a read or write transmission the LCD will display random bits. Thus the transmissions should be kept as short as possible to avoid disrupting the pattern viewed on the display. A recommended frequency is:

$f_{OSC} = 30/(t_{LCD} - 7\,t_S)$

t_{LCD} = turn on/off time of LCD

t_S = time between each successive transmission.

This should produce a flicker-free display.

The DATA OUT pin is an open drain N-channel device to V_{SS}. This output must be tied to V_{DD} through a resistor if it is to be used. It could also be tied to a lower voltage if this output is to be interfaced to logic running at a lower voltage. The value of the resistor is calculated by:

R = (+V − 0.4)/0.0006

+V = voltage of lower voltage logic

Power Supply

V_{DD} can range between 7V and 18V. A voltage should be used that is greater than or equal to the voltage that you calculate for V_{TC} as shown in *Figure 5*.

TYPICAL APPLICATIONS

One application of the MM58201 is a general purpose display to show graphic symbols and text. This type of display could be used in an electronic toy or a small portable computer or calculator. One such display is shown in *Figure 12.* This display consists of four separate LCD displays that are built into one housing. Each separate LCD display has 8 backplanes and 24 segment lines. The entire display will require four MM58201s to control it.

The circuit diagram of this application is shown in *Figure 14.* Each separate LCD display is driven by one MM58201. The backplanes are driven by the separate MM58201s and are not paralleled together. There are three common lines: CLK, DATA IN, and DATA OUT. The CLK and DATA IN are generated from an output port such as an INS8255. Four other bits of the output port generate a linear select with a different bit going to each MM58201 chip select as shown in *Figure 13.* DATA OUT is sent to one bit of an input port.

The V_{TC} driver is as described beforehand. The MM74C906 is an open drain CMOS buffer that has near regular TTL compatible inputs. This is to provide level translation from the 5V supply of the computer system to the 12V supply of the MM58201.

If I/O ports are not available, the circuit in *Figure 15* could be used as an interface between the MM58201s and a microprocessor bus.

To reduce the number of connections between the circuit and the LCD, all of the backplanes could have been driven by one MM58201 as shown in *Figure 16.* The other MM58201s would be configured as "slaves" synchronized to the one "master" MM58201. This would save 24 connections to the LCD but would increase the capacitance of the backplanes. In this application the capacitance is not a problem with either setup.

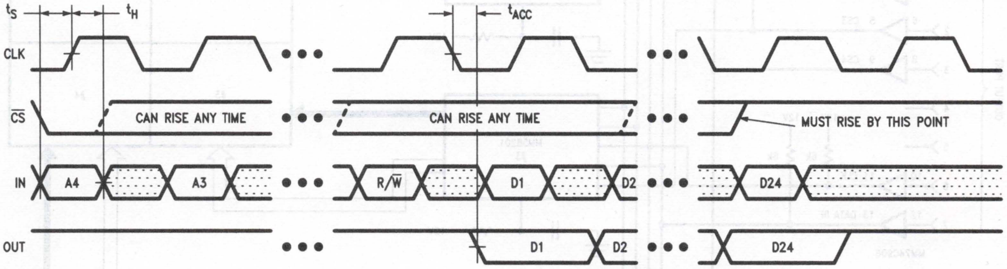

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FIGURE 11. Timing of One Transmission

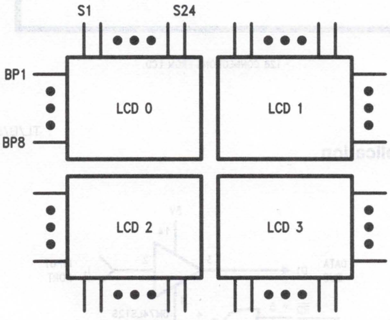

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FIGURE 12. Four Separate LCD Displays Positioned to Look Like One Display

7	6	5	4	3	2	1	0
DATA IN	CLK	X	X	$\overline{CS4}$	$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$

$\overline{CS4}$	$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	
1	1	1	0	Chip 1 Selected
1	1	0	1	Chip 2 Selected
1	0	1	1	Chip 3 Selected
0	1	1	1	Chip 4 Selected
1	1	1	1	No Chip Selected

FIGURE 13. Chip Select Scheme

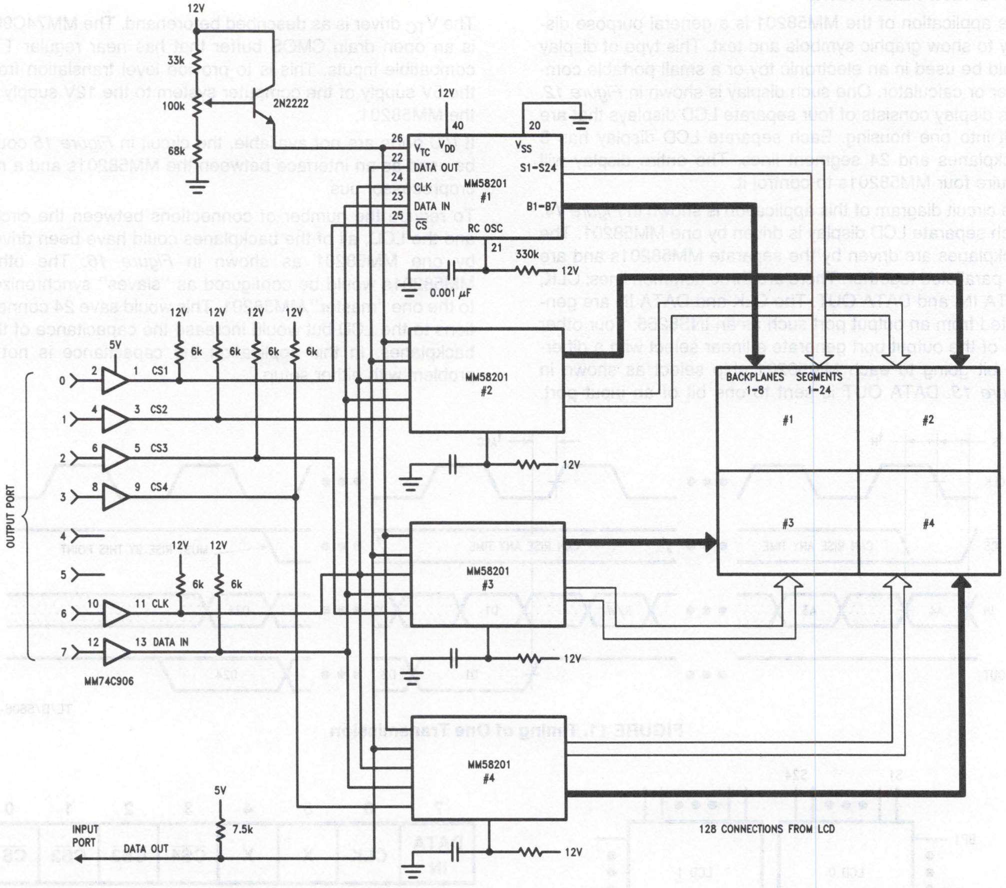
12V
33k
100k
2N2222
68k
12V
40
20
26
22
24
23
25
V_{TC} V_{DD}
V_{SS}
DATA OUT
CLK
DATA IN
$\overline{CS}$
MM58201
#1
S1–S24
B1–B7
RC OSC
21
330k
12V
0.001 µF
12V
12V
12V
12V
5V
6k
6k
6k
6k
0
1
2
3
4
5
6
7
OUTPUT PORT
2
1
CS1
4
3
CS2
6
5
CS3
8
9
CS4
12V
12V
6k
6k
10
11
CLK
12
13
DATA IN
MM74C906
MM58201
#2
MM58201
#3
MM58201
#4
12V
12V
12V
BACKPLANES 1–8
SEGMENTS 1–24
#1
#2
#3
#4
5V
7.5k
INPUT PORT
DATA OUT
128 CONNECTIONS FROM LCD

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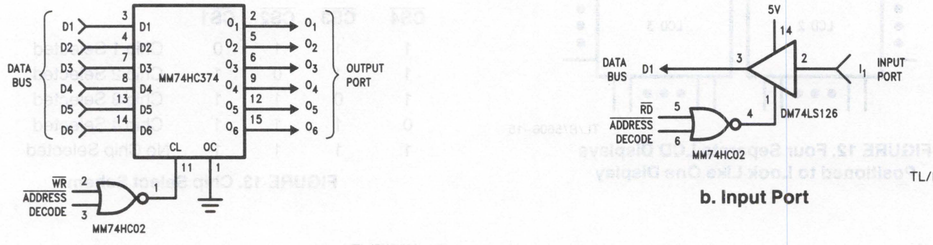
FIGURE 14. Diagram of Application


DATA BUS
D1
D2
D3
D4
D5
D6
3
4
7
8
13
14
D1
D2
D3
D4
D5
D6
MM74HC374
O_1
O_2
O_3
O_4
O_5
O_6
2
5
6
9
12
15
O_1
O_2
O_3
O_4
O_5
O_6
OUTPUT PORT
CL
OC
11
1
$\overline{WR}$
ADDRESS DECODE
2
1
3
MM74HC02
5V
14
DATA BUS
D1
3
2
I_1
INPUT PORT
$\overline{RD}$
ADDRESS DECODE
5
6
4
1
DM74LS126
MM74HC02

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a. Output Port

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b. Input Port

FIGURE 15. Input and Output Ports for Interface

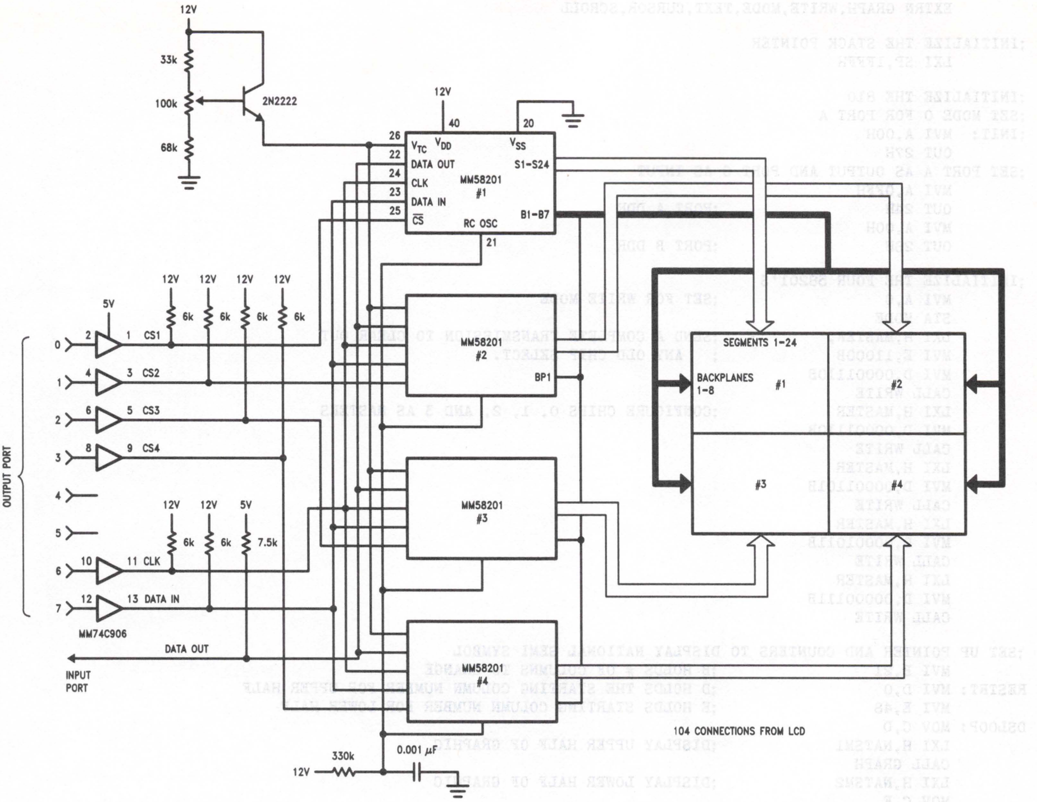
12V
33k
100k
68k
2N2222
12V
40
20
26
22
24
23
25
V_TC
V_DD
V_SS
DATA OUT
CLK
DATA IN
CS
MM58201 #1
S1–S24
B1–B7
RC OSC
21
12V
12V
12V
12V
5V
6k
6k
6k
6k
0
1
2
3
4
5
6
7
2
1 CS1
4
3 CS2
6
5 CS3
8
9 CS4
12V
12V
5V
6k
6k
7.5k
10
11 CLK
12
13 DATA IN
MM74C906
OUTPUT PORT
DATA OUT
INPUT PORT
MM58201 #2
BP1
MM58201 #3
MM58201 #4
SEGMENTS 1–24
BACKPLANES 1–8
#1
#2
#3
#4
104 CONNECTIONS FROM LCD
330k
0.001 µF
12V

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FIGURE 16. Diagram of a Master-Slave Set-Up Not Used for This Application

SOFTWARE

The real heart of this system is the software which consists of four parts. Part one is the initialization portion. This sets up the MM58201s as "masters" and programs them for 8 backplanes. It then sets up the needed pointers for the other subroutines which consist of:

1) GRAPH: displays pattern on LCD.
2) TEXT: prints ASCII characters on display.
3) SCROLL: scrolls whatever pattern is displayed to the right until LCD is cleared.

This application used an NSC800™ with 8080 mnemonics. It could easily be adapted for other microprocessors.

MAIN

This program initializes the MM58201s. It controls the sequence of display output by calling other programs.

It first sends out a "dummy" transmission to make sure that the chips are ready to respond to a valid transmission. It then programs the chips to be "masters" and to use eight backplanes.

After initialization, this program sets up the correct pointers to display a graphic symbol. First it displays the upper eight bits of it, then it displays the lower eight bits.

The words "TESTING MM58201" are then displayed. A call to scroll then causes this to scroll to the right until the screen is blank. Finally the words "END OF TEST" appear and the program ends.

The method to create a custom graphic symbol will be demonstrated in the next section.

```
        N8080
        EXTRN GRAPH,WRITE,MODE,TEXT,CURSOR,SCROLL

;INITIALIZE THE STACK POINTER
        LXI SP,1FFFH

;INITIALIZE THE 810
;SET MODE 0 FOR PORT A
;INIT:  MVI A,00H
        OUT 27H
;SET PORT A AS OUTPUT AND PORT C AS INPUT
        MVI A,0FFH
        OUT 24H                 ;PORT A DDR
        MVI A,00H
        OUT 26H                 ;PORT B DDR

;INITIALIZE THE FOUR 58201'S
        MVI A,0                 ;SET FOR WRITE MODE
        STA MODE
        LXI H,MASTER,           ;SEND A COMPLETE TRANSMISSION TO CLEAR OUT
        MVI E,11000B            ;   ANY OLD CHIP SELECT.
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER            ;CONFIGURE CHIPS 0, 1, 2, AND 3 AS MASTERS
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001101B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001011B
        CALL WRITE
        LXI H,MASTER
        MVI D,00000111B
        CALL WRITE

;SET UP POINTER AND COUNTERS TO DISPLAY NATIONAL SEMI SYMBOL
        MVI B,21                ;B HOLDS # OF COLUMNS TO CHANGE
RESTRT: MVI D,0                 ;D HOLDS THE STARTING COLUMN NUMBER FOR UPPER HALF
        MVI E,48                ;E HOLDS STARTING COLUMN NUMBER FOR LOWER HALF
DSLOOP: MOV C,D
        LXI H,NATSM1            ;DISPLAY UPPER HALF OF GRAPHIC
        CALL GRAPH
        LXI H,NATSM2            ;DISPLAY LOWER HALF OF GRAPHIC
        MOV C,E
        CALL GRAPH

        LXI H,0FFFFH            ;PAUSE
PAUSE:  DCX H
        MOV A,H
        ORA L
        JNZ PAUSE

        INR D                   ;INCREMENT STARTING COLUMN NUMBERS
        INR D
        INR D
        INR E
        INR E
        INR E
        MVI A,30                ;DISPLAY IT UNTIL COLUMN COUNT IS 30
        CMP D
        JNZ DSLOOP

        LXI H,TEXT1             ;PRINT FIRST TEXT
        MVI A,0                 ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        CALL SCROLL             ;SCROLL THE TEXT

        LXI H,TEXT2             ;PRINT SECOND TEXT
        MVI A,0                 ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        LXI H,0FFFFH            ;PAUSE
PAUSE1: DCX H
        MVI A,2
PAUSE2: DCR A
        JNZ PAUSE2
        MOV A,H
        ORA L
        JNZ PAUSE1
        LXI H,TEXT3             ;PRINT THIRD TEXT
        MVI A,0
        STA CURSOR
        CALL TEXT

        RST 6                   ;END

TEXT1:  DB "TESTING MM58201 ", 0
TEXT2:  DB "THIS IS THE END ", 0
TEXT3:  DB " OF THE   TEST  ", 0

MASTER: DB 1111B                ;ADDRESS FOR MASTER
SLAVE:  DB 0111B                ;ADDRESS FOR SLAVE

NATSM1: DB 0FFH, 0FFH, 0FFH, 7FH, 3FH, 9FH, 0CFH, 67H, 33H, 01H, 7FH
        DB 3FH, 9FH, 0CFH, 67H, 33H
        DB 99H, 0FFH, 0FFH, 00H, 00H
NATSM2: DB 0FFH, 0FFH, 0FFH, 0E6H, 0F3H, 0F9H, 0FCH, 0FEH, 0FFH
        DB 0E0H, 0E6H, 0F3H, 0F9H, 0FCH
        DB 0FEH, 0FFH, 0FFH, 0FFH, 0FFH, 00H, 00H
        END
```

GRAPH

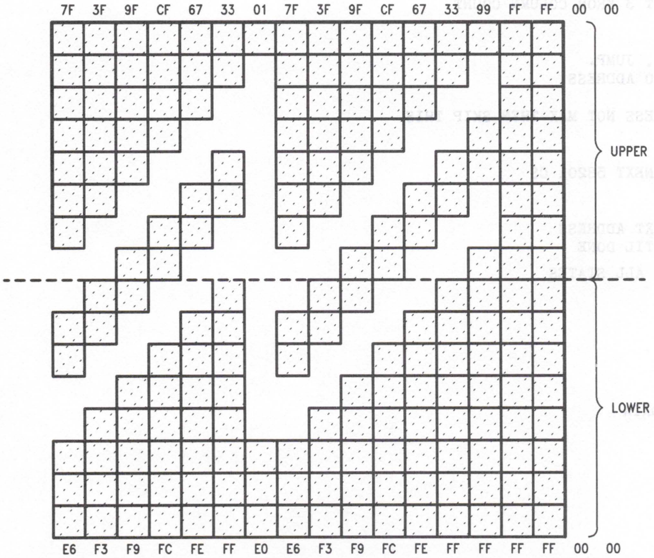
This subroutine is the center of the software. It is the interface between the calling programs and the hardware. All I/O is generated by this subroutine.

There are two entrances to this subroutine: graph and read. Graph is the entrance used to display new data. Read is the entrance used to read data from the display.

The HL register should point to the beginning of the data to be displayed. The B register should hold the number of columns to change. This must be a multiple of three. The C register should hold the column number to start with. This must also be a multiple of three. These restrictions are to simplify the software.

The first operation is the calculation of the correct chip to enable and the column number to start within that chip. The first bit of the column address is output with the correct chip select going low. The rest of the column address is then output with all the chip selects high. If the operation is a write, the data is sent to the display bit by bit. If the operation is a read, the data is read in bit by bit.

To create a custom graphic symbol, draw it on a grid as shown in *Figure 17*. Group the upper eight squares as a byte with the least significant bit at the top, counting a dark square as a one. Group the lower eight squares as a byte with the most significant bit at the bottom. Use this generated data as input lists to the graph subroutine. A good example of this is shown in the listing of main when it calls graph. Pad the data at the end with zeros as shown to keep the number of data values a multiple of three. Remember, this is only a software restriction. A different routine could be used that would allow any number of columns to be displayed.


7F 3F 9F CF 67 33 01 7F 3F 9F CF 67 33 99 FF FF 00 00
UPPER
LOWER
E6 F3 F9 FC FE FF E0 E6 F3 F9 FC FE FF FF FF FF 00 00

Data Upper: 7F, 3F, 9F, CF, 67, 33, 01, 7F, 3F, 9F, CF, 67, 33, 99, FF, FF, 00, 00

Data Lower: E6, F3, F9, FC, FE, FF, E0, E6, F3, F9, FC, FE, FF, FF, FF, FF, 00, 00

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FIGURE 17. Example Graphic Symbol

```
        N8080
        PUBLIC GRAPH, READ, WRITE, MODE
;GRAPHIC DISPLAY DRIVER
;       INPUT:  HL - POINTS TO START OF DATA
;               B- # OF 8 BIT COLUMNS TO CHANGE (MUST BE MULT. OF 3)
;               C- COLUMN # TO START WITH (MUST BE MULT. OF 3)
;       OUTPUT: NO REGISTERS DISTURBED
;               DATA POINTED TO IS DISPLAYED ON LCD DISPLAY.
;               COLUMNS NOT SPECIFIED ARE NOT AFFECTED.
READ:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H
;FLAG FOR A READ OPERATION
        MVI A,10000000B
        STA MODE
        JMP GRAPH1
GRAPH:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H
;FLAG FOR A WRITE OPERATION
        MVI A,0
        STA MODE
;CALCULATE WHICH 58201 TO ACCESS
GRAPH1: MVI D,0EEH                ;START WITH CS1
ACC:    MOV A,C
        SUI 24                    ;SUBTRACT 24 FROM COLUMN COUNT
        JC GO                     ;IF CARRY IS SET THE CORRECT CHIP IS SELECTED
        MOV C,A                   ;REG C GETS NEW COLUMN NUMBER
        MOV A,D
        RLC                       ;INCREMENT THE CS TO NEXT CHIP
        MOV D,A
        JMP ACC
;MAIN LOOP
GO:     MOV E,C                   ;GET COLUMN NUMBER
M.LOOP: CALL WRITE                ;DRAW 3 COLUMNS
        DCR B                     ;SUBTRACT 3 FROM COLUMN COUNT
        DCR B
        DCR B
        JZ END.G                  ;IF DONE, JUMP.
        MOV A,E                   ;ADD 3 TO ADDRESS
        ADI 3
        CPI 11000B                ;IF ADDRESS NOT MAX THEN SKIP THIS
        JNZ SKIP1
        MOV A,D
        RLC                       ;SELECT NEXT 58201 CS
        MOV D,A
        MVI A,0
SKIP1:  MOV E,A                   ;SAVE NEXT ADDRESS
        JMP M.LOOP                ;LOOP UNTIL DONE
END.G:  POP H                     ;RESTORE ALL STATES
        POP D
        POP B
        POP PSW
        RET
WRITE:
;       DISPLAY 3 COLUMNS OF DATA
;       INPUT:  HL- POINTS TO START OF DATA
;               E - ADDRESS
;               D - OUTPUT CS
;       OUTPUT: HL <- HL + 3
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
START:  MVI A,00001111B ;ISOLATE CS IN REG D
        ANA D
        MOV D,A
        MOV A,E                   ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS WITH CHIP SELECT
        MVI C,5
W.LOOP: MOV A,E
        RLC                     ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B
        ANA E                   ;GET MSB
        ORA D                   ;MERGE WITH CHIP SELECT
        CALL DISPLY
        DCR C                   ;DEC ADDRESS BIT COUNTER
        JNZ W.LOOP              ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A READ OR WRITE
        LDA MODE
        ORI 00001111B
        CALL DISPLY
        JP DISO                 ;JUMP IF THIS IS A WRITE

;READ THE DATA
        MVI B,3                 ;3 BYTES OF DATA
READ1:  MVI C,B                 ;8 BITS PER BYTE
        MVI D,0                 ;CLEAR DATA BYTE
READ2:  IN 22H                  ;GET A BIT OF DATA
        ANI 00000001B           ;MASK OFF UNWANTED BITS
        ORA D                   ;MERGE WITH DATA BYTE
        RRC                     ;ROTATE DATA
        MOV D,A
        MVI A,00001111B         ;SET UP 58201 TO READ NEXT BIT
        CALL DISPLY
        DCR C                   ;LOOP UNTIL DONE WITH BYTE
        JNZ READ2
        MOV M,D
        INX H                   ;INCREMENT BYTE POINTER
        DCR B                   ;LOOP UNTIL DONE WITH ALL BYTES
        JNZ READ1

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

;DISPLAY THE DATA
DISO:   MVI B,3                 ;3 BYTES OF DATA
DIS1:   MVI C,8                 ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D                 ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B           ;GET NEXT BIT
        ORI 00001111B           ;SET CS
        CALL DISPLY             ;OUTPUT A BIT OF DATA
        DRC C
        JNZ DIS2                ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1                ;LOOP UNTIL DONE WITH 3 BYTES

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

DISPLY:
;DISPLAY ROUTINE
;       INPUT:  A - DATA AND CHIP SELECT
;                               BIT 7 - DATA
;                               BITS 0-3 - CHIP SELECT
;       OUTPUT: NO REGISTERS DISTURBED
;               OUTPUT ONE BIT TO 58201

        PUSH PSW                ;SAVE STATES

        ANI 10001111B           ;MASK OFF UNWANTED BITS
        OUT 20H                 ;SET UP DATA AND CHIP SELECT
        ORI 01000000B           ;CLOCK HIGH
        OUT 20H
        ANI 10111111B           ;CLOCK LOW

        POP PSW                 ;RESTORE STATES
        RET

MODE:   DS 1
        END
```

TEXT

This subroutine will take the ASCII text pointed to by HL and display it on the LCD starting at the column pointed to by the memory location CURSOR. The data should end with a zero. CURSOR should be in the range of 0–15 as this is the extent of this LCD display. The first operation is the calculation of the offset into the ASCII table of the first character. Thirty-two is subtracted from the ASCII number because the table starts with a space character. This result is then multiplied by six because the data to be displayed is six bytes long. We now have the offset into the table. The character is displayed on the LCD. This operation is repeated until all the characters have been displayed.

A custom font can be generated using the same technique as that used to create a custom graphic symbol.

```
        N8080
        EXTRN GRAPH
        PUBLIC TEXT, LET        TR, CURSOR

TEXT:
;DISPLAY A CHARACTER STRING ON LCD DISPLAY
;       INPUT:  HL-POINTS TO BEGINNING OF STRING
;               CURSOR-CURRENT CURSOR POSITION
;       OUTPUT: CURSOR <= CURSOR + LENGTH OF STRING
;               NO REGISTERS DISTURBED

        PUSH PSW                ;SAVE STATES
        PUSH H
T.LOOP: MOV A,M                 ;CHECK FOR END OF STRING
        CPI 0
        JZ T.FIN
        CALL LETTR              ;PRINT LETTER
        INX H
        JMP T.LOOP              ;LOOP UNTIL DONE
T.FIN:  POP H                   ;RESTORE STATES
        POP PSW
        RET


LETTR:
;DISPLAY AN ASCII CHARACTER ON LCD DISPLAY
;       INPUT:  A-CHARACTER TO DISPLAY
;               CURSOR-CURRENT CURSOR LOCATION (0 - 95)
;       OUTPUT: CURSOR <= CURSOR + 1
;               NO REGISTERS DISTURBED

;SAVE STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP HL TO POINT TO CORRECT DATA
        LXI H,ASCII             ;HL POINTS TO BASE ADDRESS
        MVI B,0                 ;BC GETS ASCII OFFSET MINUS A CONSTANT
        SUI 20H
        MOV C,A
        CALL MULT               ;MULTIPLY OFFSET BY 6 (DOUBLE PRECISION)
        DAD B                   ;HL POINTS TO CORRECT CHARACTER DATA
        LDA CURSOR              ;MULTIPLY CURSOR BY 6 TO GET COLUMN NUMBER
        MOV B,A
        ADD B
        ADD B
        ADD B
        ADD B
        ADD B
        MOV C,A
        MVI B,6                 ;EACH CHARACTER IS SIX COLUMNS WIDE
        CALL GRAPH              ;DISPLAY THE CHARACTER
        LDA CURSOR              ;INCREMENT CURSOR
        INR A
        CPI 16                  ;CHECK FOR END OF LCD DISPLAY
        JNZ T.END
        MVI A,0                 ;IF SO, RESET TO ZERO
T.END:  STA CURSOR

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET
```

```
MULT:
;MULTIPLY BC REG BY SIX
;       INPUT:  BC - MULTIPLICAND
;       OUTPUT: BC <= BC * 6
;               NO REGISTERS DISTURBED

        PUSH PSW
        PUSH H
        MOV H,B
        MOV L,C
        DAD B
        DAD B
        DAD B
        DAD B
        DAD B
        MOV B,H
        MOV C,L
        POP H
        POP PSW
        RET

CURSOR: DS 1
ASCII:  DB 0,0,0,0,0,0              ;SPACE
        DB 0,95,95,0,0,0            ;!
        DB 0,7,0,7,0,0              ;"
        DB 20,127,20,127,20,0       ;#
        DB 36,42,127,42,18,0        ;$
        DB 35,19,8,100,98,0         ;%
        DB 54,73,102,32,80,0        ;&
        DB 0,0,7,0,0,0              ;'
        DB 0,28,34,65,0,0           ;(
        DB 0,65,34,28,0,0           ;)
        DB 34,20,127,20,34,0        ;*
        DB 8,8,62,8,8,0             ;+
        DB 0,64,48,0,0,0            ;'
        DB 8,8,8,8,8,0              ;-
        DB 0,96,96,0,0,0            ;,
        DB 32,16,8,4,2,0            ;/

        DB 62,81,73,69,62,0         ;0
        DB 0,66,127,64,0,0          ;1
        DB 122,73,73,73,70,0        ;2
        DB 34,65,73,73,54,0         ;3
        DB 15,8,8,126,8,0           ;4
        DB 39,69,69,69,57,0         ;5
        DB 62,73,73,73,49,0         ;6
        DB 1,97,17,9,7,0            ;7
        DB 54,73,73,73,54,0         ;8
        DB 6,9,9,9,126,0            ;9
        DB 0,54,54,0,0,0            ;:
        DB 96,54,54,0,0,0           ;;
        DB 8,20,34,65,0,0           ;<
        DB 20,20,20,20,20,0         ;=
        DB 0,65,34,20,8,0           ;>
        DB 2,1,88,5,2,0             ;?
        DB 62,65,93,89,78,0         ;@

        DB 124,18,17,18,124,0       ;A
        DB 127,73,73,73,54,0        ;B
        DB 62,65,65,65,34,0         ;C
        DB 127,65,65,65,62,0        ;D
        DB 127,73,73,65,65,0        ;E
        DB 127,9,9,1,1,0            ;F
        DB 62,65,65,81,114,0        ;G
        DB 127,8,8,8,127,0          ;H
        DB 0,65,127,65,0,0          ;I
        DB 32,64,64,64,63,0         ;J
        DB 127,8,20,34,65,0         ;K
        DB 127,64,64,64,64,0        ;L
        DB 127,2,12,2,127,0         ;M
        DB 127,4,8,16,127,0         ;N
        DB 62,65,65,65,62,0         ;O
        DB 127,9,9,9,6,0            ;P
        DB 62,65,81,33,94,0         ;Q
        DB 127,9,25,41,70,0         ;R
        DB 34,69,73,81,34,0         ;S
        DB 1,1,127,1,1,0            ;T
        DB 63,64,64,64,63,0         ;U
        DB 31,32,64,32,31,0         ;V
        DB 127,32,24,32,127,0       ;W
        DB 99,20,8,20,99,0          ;X
        DB 3,4,120,4,3,0            ;Y
        DB 97,81,73,69,67,0         ;Z

END
```

SCROLL

This subroutine will scroll whatever is displayed on the LCD to the right until the screen is clear. It first reads in three columns of data. It then writes three columns of data with the HL pointer shifted by one byte. This will shift the displayed data by one column. This is repeated until the entire LCD has been shifted by one column. Then the entire operation is repeated until all the displayed data is shifted off the screen.

This subroutine could easily be adapted to scroll the display to the left if desired.

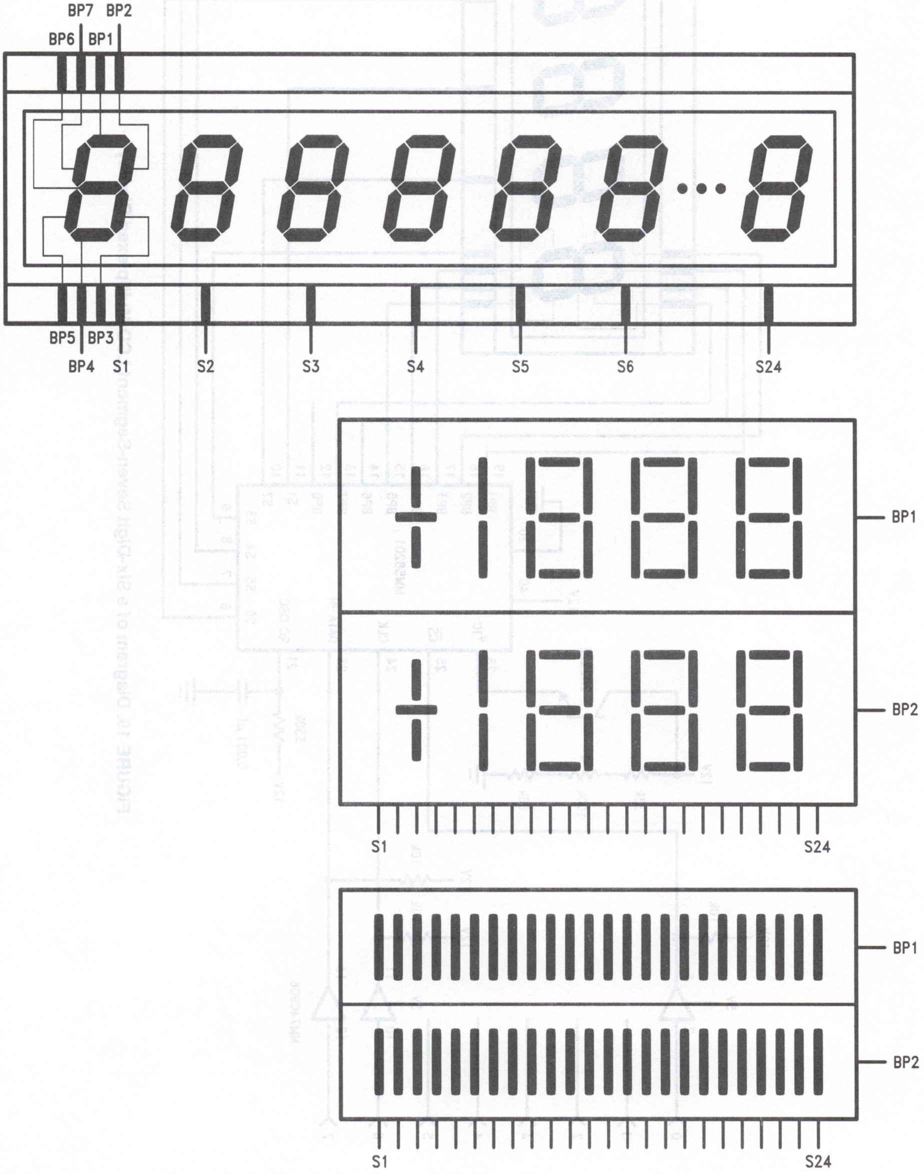
```
        N8080
        PUBLIC SCROLL
        EXTRN READ,GRAPH

SCROLL:
;SCROLLS DISPLAY TO THE RIGHT UNTIL CLEAR
;       INPUT:  NONE
;       OUTPUT: NO REGISTERS ARE CHANGED
;               SCREEN IS SCROLLED UNTIL CLEAR

;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP ALL THE POINTERS
        MVI D,96                        ;LOOP UNTIL SCREEN IS CLEAR (96 CYCLES)
REPEAT: MVI A,0                         ;CLEAR FIRST BYTE IN BUFFER
        STA BUFFER
        MVI B,3                         ;READ 3 COLUMNS ALWAYS
        MVI C,0                         ;START WITH COLUMN ZERO

;READ THE DATA
L.READ: LXI H,BUFFER+1                  ;SET HL TO POINT TO BUFFER+1
        CALL READ
        LXI H,BUFFER                    ;SET HL TO SHIFT THE DATA
        CALL GRAPH                      ;REDRAW THE SHIFTED DATA

;MOVE LAST COLUMN OF LAST READ INTO FIRST COLUMN OF NEXT WRITE
        LDA BUFFER+3
        STA BUFFER

;UPDATE COUNTERS
        MOV A,C                         ;INCREMENT COLUMN NUMBER
        ADI 3
        MOV C,A
        CPI 96                          ;CHECK IF DONE WITH ONE CYCLE
        JNZ L.READ
        DCR D                           ;DECREMENT LOOP COUNT
        JNZ REPEAT                      ;LOOP UNTIL DONE WITH ALL CYCLES

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET

BUFFER: DS 4

        END
```

OTHER APPLICATIONS

There are many different types of LCDs that can be controlled by the MM58201. Some of these are shown in *Figure 18*.

Up to 24 seven-segment digits can be controlled by one MM58201. The software to control a multiplexed seven-segment display is not too much different from that of the previous application. The software is simpler because only one MM58201 is needed instead of four. A logic diagram for a six-digit multiplexed seven-segment LCD display is shown in *Figure 19* and the software to control it is in Listing 5.

Given a string of numbers to display, this subroutine simply looks up the data it needs from a look-up table and stores this data in a buffer. After every three digits, the subroutine sends this data to the MM58201 to be displayed. The digit backplanes are wired backward in groups of three to simplify the software. The subroutines that this subroutine uses are very similar to the equivalent subroutines in the LCD dot matrix application. Since there is only one MM58201, the software is simpler. There is no need to calculate which MM58201 chip select to enable.



TL/B/5606-21

FIGURE 18. Typical LCD Connections to the MM58201

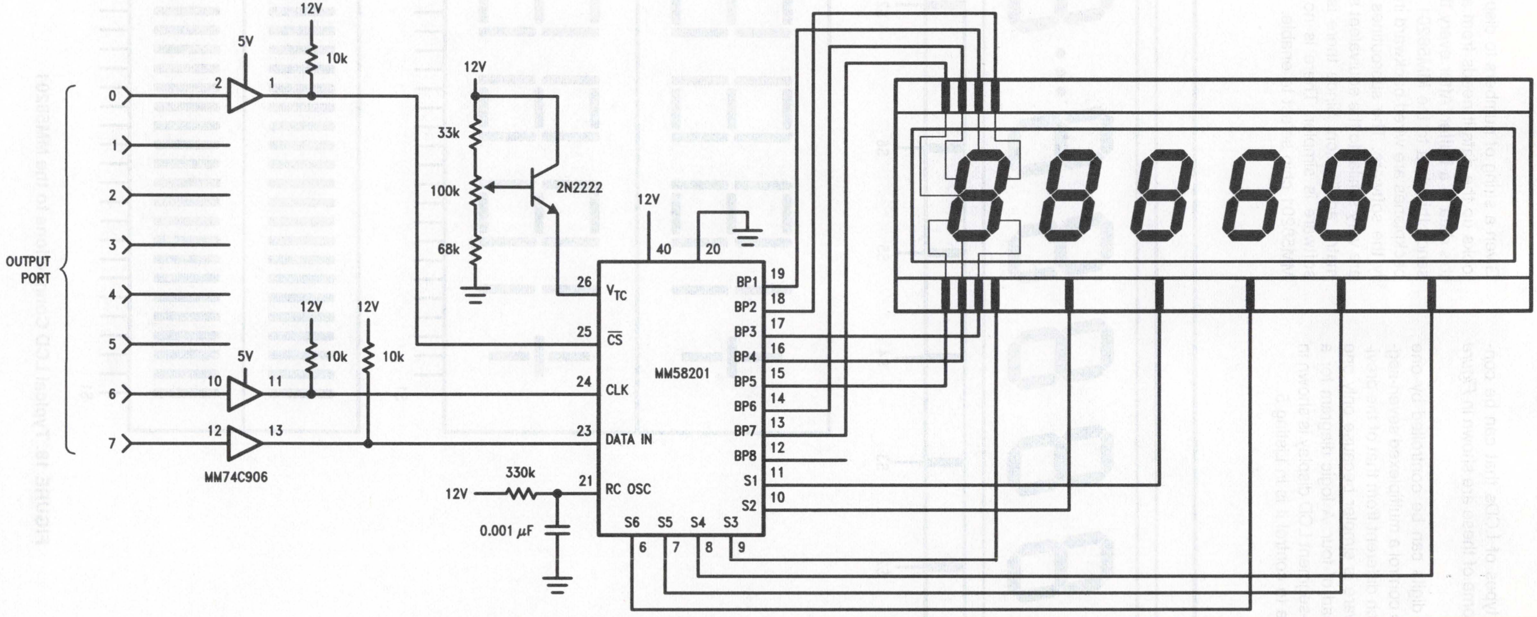

OUTPUT PORT
0
1
2
3
4
5
6
7
5V
2
1
12V
10k
12V
33k
100k
68k
2N2222
12V
10k
12V
10k
5V
10
11
12
13
MM74C906
330k
12V
0.001 μF
12V
40
20
26
25
24
23
21
V_{TC}
$\overline{CS}$
CLK
DATA IN
RC OSC
MM58201
BP1
BP2
BP3
BP4
BP5
BP6
BP7
BP8
S1
S2
S6
S5
S4
S3
19
18
17
16
15
14
13
12
11
10
6
7
8
9

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FIGURE 19. Diagram of a Six-Digit Seven-Segment LCD Multiplexed Display

```
        N8080
;INITIALIZE THE 810
        MV A,0
        OUT 27H
        MVI A,0FFH
        OUT 24H

        LXI BC,TEST
        MVI E,6
        CALL NUMBER
        RST 6

TEST:   DB 1,2,3,4,5,6

;SUBROUTINE TO DISPLAY NUMERALS ON LCD DISPLAY
;       INPUT   BC-POINTS TO BCD DATA STRING
;               E -LENGTH OF DATA STRING (MULTIPLE OF 3)
;       OUTPUT    -NO REGISTERS DISTURBED
;                 -DATA STRING IS DISPLAYED
;
NUMBER: PUSH PSW                ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

DIG3:   MVI D,3                 ;LOOP FOR 3 DIGITS
LOOP:   LDAX B
        LXI H,TABLE             ;CALCULATE ADDRESS INTO TABLE
        ADD L
        MOV L,A
        MVI A,00H
        ADC H
        MOV H,A

        MOV A,M                 ;GET OUTPUT DATA FROM TABLE
        PUSH PSW

        LXI H,DATA              ;STORE INTO DATA BUFFER
        MOV A,L
        ADD D
        MOV L,A
        DCR L
        POP PSW
        MOV M,A

        INX B                   ;INCREMENT POINTER TO DATA STRING
        DCR E                   ;DECREMENT # OF DIGITS
        DCR D                   ;DECREMENT 3 DIGIT COUNT
        JNZ LOOP                ;IF NOT THIRD DIGIT THEN LOOP BACK

        LXI H,DATA
        CALL WRITE              ;DISPLAY THESE THREE DIGITS

        MOV A,E                 ;CHECK FOR LAST DIGIT OF DATA STRING
        ANA A
        JNZ DIG3

        POP H                   ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

WRITE:
; DISPLAY 3 DIGITS
;       INPUT   HL-POINTS TO START OF DATA
;               E -COLUMN ADDRESS
;       OUTPUT    -NO REGISTERS DISTURBED
;
        PUSH PSW                ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

        MOV A,E                 ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS
        MVI C,5
W.LOOP: MOV A,E
        RLC                     ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B         ;GET MSB & ENABLE CHIP SELECT BIT
        ANA E
        CALL OUT                ;OUTPUT BIT WITH CHIP SELECT
        DCR C
        JNZ W.LOOP              ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A WRITE
        MVI A,00H
        CALL OUT                ;OUTPUT A ZERO BIT

;OUTPUT THE DATA
        MVI B,3                 ;3 BYTES OF DATA
DIS1:   MVI C,B                 ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D                 ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B           ;GET NEXT BIT
        ORI 00000001B           ;DISABLE CHIP SELECT
        CALL OUT
        DCR C
        JNZ DIS2                ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1                ;LOOP UNTIL DONE WITH 3 BYTES

        POP H                   ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

OUT:
;SUBROUTINE TO OUTPUT ONE BIT TO THE MM58201
;       INPUT   A -DATA BIT IN MSB POSITION
;       OUTPUT    -NO REGISTERS DISTURBED
;                 -OUTPUT ONE BIT TO 58201

        PUSH PSW
        OUT 20H
        ORI 01000000B           ;CLOCK HIGH
        OUT 20H
        ANI 10111111B           ;CLOCK LOW
        OUT 20H
        POP PSW
        RET

DATA:   DS 3
TABLE:  DB 00111111B, 00000110B, 01011011B, 01001111B
        DB 01100110B, 01101101B, 01111101B, 00000111B
        DB 01111111B, 01101111B

        END
```

SUMMARY

The MM58201 makes it easy to interface a multiplexed LCD display to a microprocessor. It is simply a matter of connecting the display and the microprocessor to the chip, choosing a value for V_{CT}, then interfacing your program to use the subroutines listed here or similar ones. Multiplexed LCDs are the perfect way to cut down on display interconnections while still taking advantage of the LCD's low power consumption and high contrast ratio—and the MM58201 makes them easy to use.

The MM58348/342/341/248/242/241 Directly Drive Vacuum Fluorescent (VF) Displays

National Semiconductor
Application Note 371
David Stewart

1.0 INTRODUCTION

National has produced a family of high voltage display drivers which is specially designed for use with vacuum fluorescent (VF) displays. These circuits are fabricated using a standard metal gate CMOS process which has been extended to allow a maximum operating voltage of 60V, thus enabling the design of bright multiplexed displays. In this way, the advantages of CMOS are retained (low power), while the range of applications for this technology is increased. Many of today's high voltage MOS display drivers require the use of one external resistor per display output, and this leads to a considerable increase in component count and board area. National's display drivers, however, incorporate an on-board pull-down resistor structure which removes these disadvantages.

This application note is intended to demonstrate several ways in which these display drivers can be configured to drive and control a wide range of VF displays. Although particular attention will be given to one specific display, a 32-character alphanumeric display, the design is presented in such a way as to enable easy extrapolation to the system designer's specific applications.

2.0 FUNCTIONAL DESCRIPTION

There are six circuits in this new family of high voltage VF drivers and they can be sub-divided according to maximum operating voltage, number of display outputs, data interfacing requirements and ability to be cascaded. Each of the three circuit configurations is available with maximum operating voltages of 35V (MM583XX) or 60V (MM582XX). Due to the nature of the output stage required to attain high voltage operation of CMOS devices, the drive capabilities of the display output decrease as maximum operating voltage increases. Therefore, to maintain the option of trading off display voltage against drive current, each circuit has a high voltage (reduced drive) version and a low voltage (high drive) version. The three circuit configurations can be identified by the number of display outputs they contain (e.g., 20, 32 or 35 outputs). In all cases, data is entered serially into a 5V internal CMOS shift register. This data is latched to the output either by an external enable control signal (MM58241/341/242/342) or automatically by a leading start bit in the data stream (MM58248/348). *Figure 1* shows how the 6 device numbers correspond to the different circuit configurations and operating voltages.

The MM58348/248 devices use a two control line data input format (data in and clock) which enables the 40-pin part to have 35 display outputs. To load data into the controller, a start bit precedes the 35 data bits. The start bit is a logical "1" clocked into the IC by the first clock pulse. Next, 35 data bits are clocked into these parts. The start and data bits are shifted in on the rising edge of the clock. As the data is clocked into the IC, the start bit is shifted down the 35-bit register. On the rising edge of the 36th clock pulse, data is transferred to the display register and the start bit is shifted into the control latch. On the negative edge of the clock, the shift register is cleared. The display register feeds the level shifters that translate 5V CMOS levels to the 35V–60V required by the display. The MM58348/248 devices are not cascadable. Typically, these devices would perform the segment refresh drive in a multiplexed multi-digit system. A functional block diagram is shown in *Figure 2*.

The MM58341/241/342/242 devices use a three control line data input format (data in, clock and enable) and have either 32 or 20 display outputs, as given by *Figure 1*. This configuration sacrifices some outputs to enable cascading, enhance control signal flexibility, and provide brightness control. Here again, data is shifted into the shift register on the rising edge of clock, but no start bit is needed. Instead, the enable signal is taken high to input data to the chip. When the enable is taken low, the contents of the shift register are loaded into the display register. Again, the display register feeds the level translator and display driver outputs.

Each of the MM58241/341 and MM58242/342 devices has a serial data output pin which is connected directly to the last stage's output of the shift register. By connecting data out from one device to the data in pin of another device, and by holding each circuit's enable constantly high, the display drivers can be cascaded. The result is a shift register with a variable number of bits, depending on the mix of circuits used.

The MM58341/241/342/242 devices also have a blanking control input. A logic high on this pin turns all outputs off, while still retaining the display data. If a logic "0" is then applied, the display data will return unchanged. Consequently, the brightness of the display is proportional to the duty cycle of this blank signal. A functional block diagram of these devices is shown in *Figure 3*.

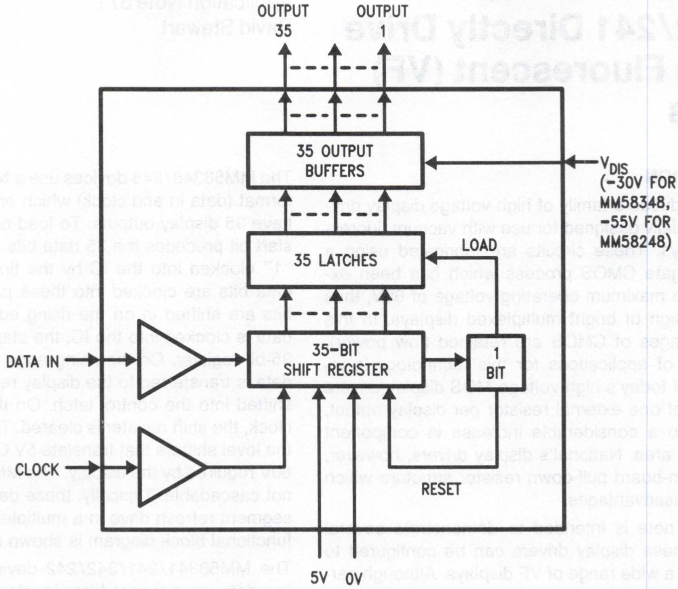
		Operating Voltage	
		35V	**60V**
Number of Outputs	20	MM58342	MM58242
	32	MM58341	MM58241
	35	MM58348	MM58248

20 and 32 output drivers use envelope enable data format and may be cascaded.

35 output (5 x 7 dot matrix) drivers use start bit data format.

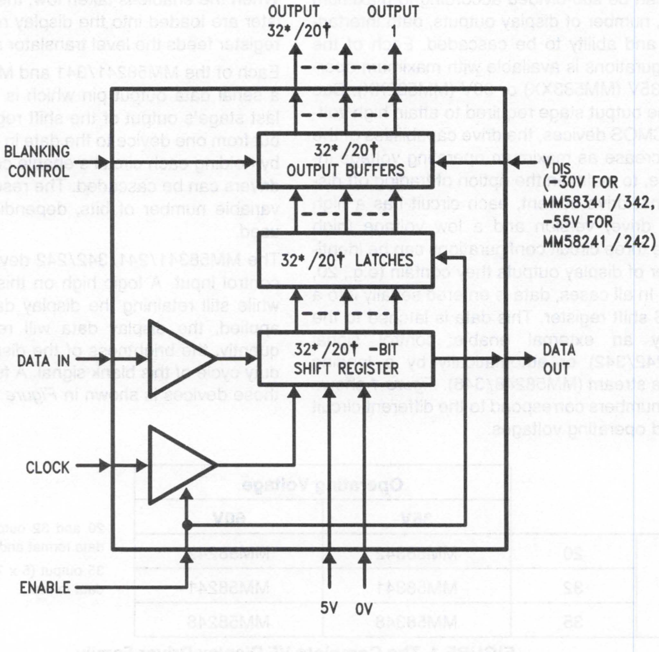
FIGURE 1. The Complete VF Display Driver Family

BLOCK DIAGRAMS


OUTPUT 35
OUTPUT 1
35 OUTPUT BUFFERS
V_{DIS} (−30V FOR MM58348, −55V FOR MM58248)
LOAD
35 LATCHES
DATA IN
35-BIT SHIFT REGISTER
1 BIT
CLOCK
RESET
5V
0V

TL/F/7394-1

FIGURE 2. MM58348/248

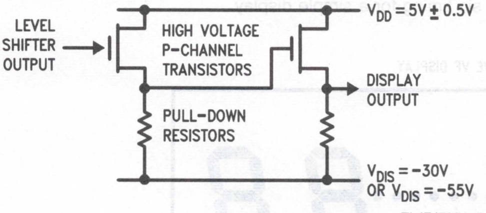

OUTPUT 32*/20†
OUTPUT 1
BLANKING CONTROL
32*/20† OUTPUT BUFFERS
V_{DIS} (−30V FOR MM58341/342, −55V FOR MM58241/242)
32*/20† LATCHES
DATA IN
32*/20† -BIT SHIFT REGISTER
DATA OUT
CLOCK
ENABLE
5V
0V

TL/F/7394-2

FIGURE 3. MM58341/241* and MM58342/242†

2.0 FUNCTIONAL DESCRIPTION (Continued)

Referring to the functional block diagrams shown in *Figures 2* and *3*, it is clear that all the internal logic is implemented in standard 5V CMOS. Such signals do not possess sufficient drive for the high voltage output stage, so the data passes through a bank of 15V level shifters to the output section. A schematic of the output stage is shown in *Figure 4*. It can be seen that all these display drivers use a two-stage high voltage structure with active pull-up transistors and passive pull-down resistors to the display voltage. Because resistor pull-downs are used, it is the output switching "off" time which is critical for the system design, and this is typically 20 μs for a rail-to-rail voltage swing.



TL/F/7394-3

FIGURE 4. High Voltage Output Structure

3.0 DESIGN CONSIDERATIONS

3.1 The VF Display Configuration

The operation of a VF display is merely an extension of the valve principle, i.e., it is a voltage controlled device. An AC waveform is applied across the filament of the display, and this excitation causes electrons to be emitted. If both the grid and the anode are at a high positive voltage with respect to the cathode, the electrons reach the anode area, which is coated with a fluorescent material. When bombarded by electrons, this material emits light, hence one segment of the display is turned on.

This particular family of display drivers can drive a wide range of VF displays. The simplest case is where each display segment can be directly driven by wiring each output to the display anode. This normally occurs on displays with a small number of digits and segments (e.g., 4 characters of 7 segments) and this can be driven by cascading the drivers until sufficient data bits are available. This display configuration has the advantage of not requiring any refresh (which would be required if a multiplexed configuration were used) but has the disadvantage of needing one wire per segment.

As the size of the display increases, the number of available segments also rises, thus a multiplexing scheme which will reduce the number of display connections is desirable. This is normally achieved by hard wiring all the segments (anodes) of each digit together, then using the grids to select each digit in turn. The correct segment data can then be displayed. Using these techniques necessitates that the display be continually refreshed with each digit of data, even when that data has not changed.

To see the advantage of multiplexing, if a 32 character 5 x 7 dot matrix display is used, a total of 1120 segments is available. For this reason, the display is multiplexed and has 32 grid inputs and 35 segment inputs. The required refreshing task must be accomplished without the detection of flickering by the human eye, i.e., at a rate greater than 50 Hz. (Refresh timing is discussed later.)

Given the aforementioned display pinout and control logic, it is desirable in multiplexed displays to use the MM58341 to control the display grids (digits) and one MM58348 to control the display anodes (segments).

3.2 The Display-Driver Interface

When using the MM58XXX series, no buffering is required between the driver output pins and the VF display. It is necessary only that the driver charge and discharge the display in such a time that the refresh rate outlined in the previous section can be achieved. All the CF drivers have LSTTL compatible inputs, and, as the data source is generally a microprocessor, no special interface requirements exist.

3.3 The Microprocessor-Driver Interface

Typically, the system utilizing these display drivers will have some sort of microprocessor or single chip computer controlling the display. Thus, this processor will control one or more of the display drivers. The drivers have relatively little intelligence, therefore the host processor will be in charge of updating the display drivers and generating refresh timing if needed. The advantage of having minimal intelligence on the drivers themselves is flexibility. Virtually any display size or type can be used with equal ease, from small 7-segment, to British flag types, to larger 5 x 7, 7 x 9 or 5 x 12 displays.

The drivers can be directly interfaced to the microcontroller, COPS™4XX, or 80C48/9. This would normally be accomplished by connecting the driver's data and clock lines to control ports on the microprocessor. The MM58248/348 series is capable of accepting clock rates up to 1 MHz, and the MM58241/341 800 kHz. This is far faster than the control port bit manipulation rates for these controllers and will ensure compatibility with most low end microprocessors. 1 MHz input clock rates will also ensure that the desired display refreshing rate is attained.

In higher end systems using NSC800™ or 6800 8-bit microprocessors, the 1 MHz clock rate, coupled with a 300 ns minimum pulse width, simplified direct interfacing of these drivers to a μP bus. In the simple case, some logic for address decoding would set aside an I/O port for communiction to each driver, then several bits of the data bus could be gated to create the clock, data and enable signals.

4.0 TYPICAL DESIGN IMPLEMENTATION

4.1 Simple Direct Drive Application

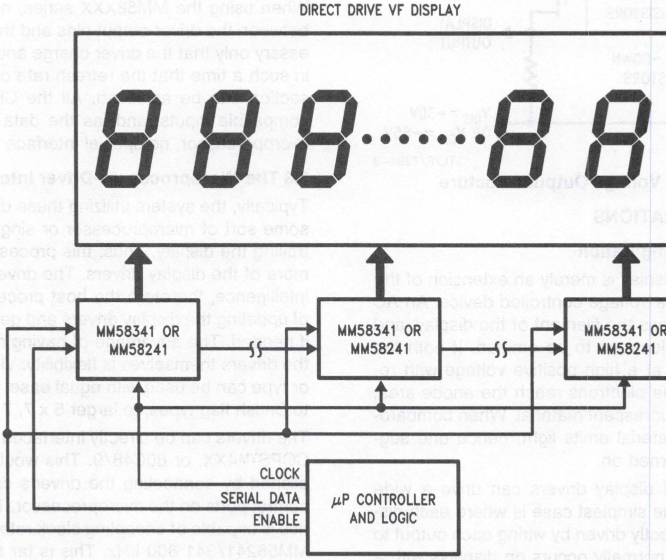
Figure 5 illustrates a simple cascaded direct drive application where MM58241s are cascaded to drive a 7-segment (plus decimal point) display. The MM58241s were chosen because of the ease with which they can be cascaded. The MM58248s can also be used and provide a few more outputs per package, but cannot be cascaded.

In this application, the controlling μP need only update the display whenever the data changes. When updating the display, the data is assembled, enable is raised, and the data is clocked serially to the driver. Once all the data is loaded into the shift registers, the enable is taken low. This action updates the display.

4.2 A 32-Digit 5 x 7 Dot Matrix Application

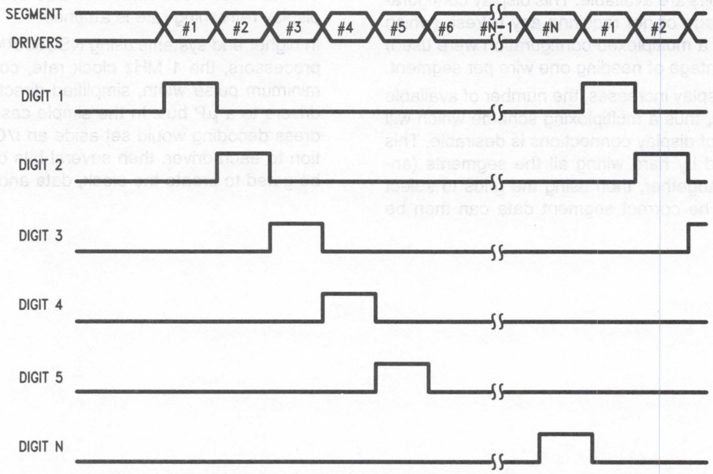
In this application, the obvious choice is to implement some sort of multiplexing scheme to drive the display with fewer lines. This application usually requires that a dedicated controller be used to generate all the timing signals.

General multiplex timing of a VF display is usually similar to LED multiplexing. First, the segment data for one character is output to the display. Next, the digit strobe for that digit is raised, enabling the character. Then the digit strobe is brought low while the segment data is changed to the next character on the display. The next character is enabled by raising the digit strobe. This action continues until each character is turned on sequentially. *Figure 6* shows the basic timing for a simple display.


DIRECT DRIVE VF DISPLAY
MM58341 OR MM58241
MM58341 OR MM58241
MM58341 OR MM58241
CLOCK
SERIAL DATA
ENABLE
µP CONTROLLER AND LOGIC

TL/F/7394-4

FIGURE 5. Typical Direct Drive System with μP


SEGMENT DRIVERS
#1
#2
#3
#4
#5
#6
#N-1
#N
#1
#2
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
DIGIT 5
DIGIT N

TL/F/7394-5

FIGURE 6. Simplified Timing for Multiplexed VF Display

4.2 A 32-Digit 5 x 7 Dot Matrix Application (Continued)

In this design, it is logical to use one MM58341 to control the display's digits. As will be seen, this driver can be easily used to shift a single high level bit which will be used to sequentially enable each character. One MM58348 can be used to drive the segments. A 5 x 7 matrix has 35 segments, which is ideal for the MM58348. Therefore, this configuration has a total of 6 connecting lines to interface the microprocessor to the display drivers. The connection diagram is shown in *Figure 7*. Because both of the drivers accept data only when the clock is active, it would be possible to couple both data lines together. However, although this saves one interface line, there is a disproportionate increase in the software burden.

The choice of which driver to use for segments and which for digits is dependent only on which configuration is the simplest to implement in hardware or software. The MM58241/242/248 devices are all equally capable of driving the digits or segments of a display.

4.3 Multiplexed Display Refresh Timing: The Controllers

Considering first the digit driver (MM58341), it is clear that the digits must be enabled sequentially and that this process must be continuous, even when the display data has not changed. To this end, the data for the MM58341 is simply a one followed by 31 zeroes, where the one is shifted along the internal register. As each digit is enabled, the corresponding segment data is displayed. To ensure that no ghosting effects are seen during the transition between digits, the blank signal is activated for a short time before and after the segment data is changed. *Figure 8* shows the microprocessor waveforms and the resultant display waveforms for the 32-character design. Thus, one can see how the blank is used to mask the display while the digit enable signal goes low and the segment data is latched.

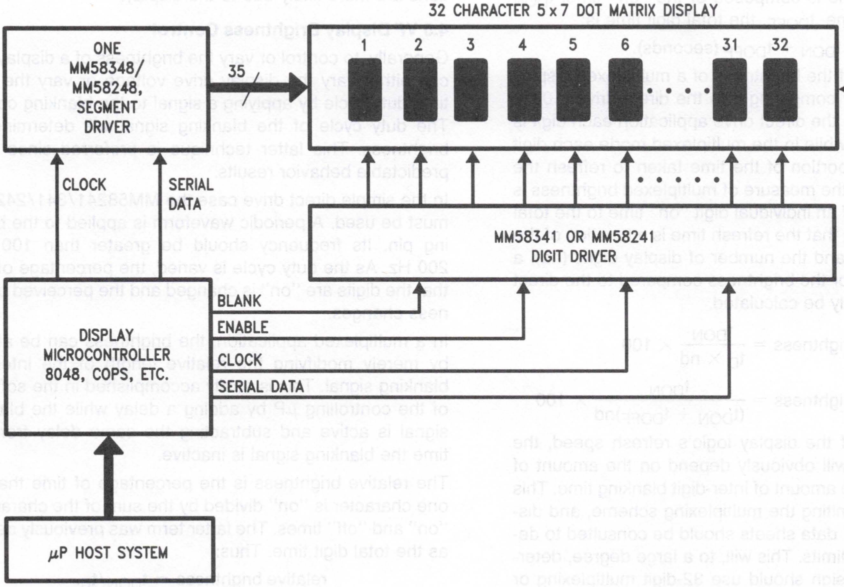

32 CHARACTER 5 x 7 DOT MATRIX DISPLAY
ONE MM58348/ MM58248, SEGMENT DRIVER
35
1
2
3
4
5
6
31
32
FILAMENT
CLOCK
SERIAL DATA
MM58341 OR MM58241 DIGIT DRIVER
BLANK
ENABLE
CLOCK
SERIAL DATA
DISPLAY MICROCONTROLLER 8048, COPS, ETC.
µP HOST SYSTEM

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FIGURE 7a. Typical Architecture for Higher End System Utilizing Dedicated Display μP

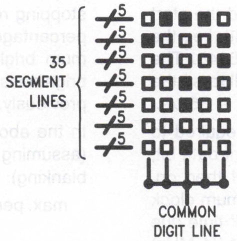
5
5
5
5
5
5
5
35 SEGMENT LINES
COMMON DIGIT LINE

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FIGURE 7b. Detail of Typical Dot Matrix Digit

4.4 Multiplexed Display Refresh Timing: Display Brightness (Continued)

The refresh rate of the display is defined as the frequency at which each digit is enabled (i.e., the reciprocal of the time taken to display all digits). It is generally accepted that in order to avoid visible flickering, a refresh rate in excess of 50 Hz is required. Typically, VF manufacturers recommend 100 Hz–200 Hz. Some sample calculations follow and assume a refresh rate of 100 Hz. Therefore, the time given to display all digits is 1/(100 Hz) = 10 ms, and is 10 ms/number of digits) for any one digit. For this example, 10 ms/32 = 312.5 µs. This is defined as the total digit multiplex time and will be made up of a digit "on" time and an inter-digit blanking time. The inter-digit blanking is required to prevent display ghosting when digit information changes.

In general, then, the total digit time (t_D) is the inverse of the refresh rate (fr) divided by the number of digits in the display (nd), i.e.,

$$t_D = 1/(\text{fr x nd}) \text{ seconds.}$$

Since each digit time is composed of the "on" time, t_{DON} and the blanking time, t_{DOFF}, the total digit time is:

$$t_D = t_{DON} + t_{DOFF} \text{ (seconds).}$$

A useful measure of the brightness of a multiplexed display can be obtained by comparing it to the direct drive (100% brightness) case. In the direct drive application each digit is "on" permanently, while in the multiplexed mode each digit is "on" only for a portion of the time taken to refresh the display. Therefore, the measure of multiplexed brightness is given by the ratio of an individual digit "on" time to the total refresh time. Noting that the refresh time is a function of the total digit time (t_D) and the number of display digits (nd), a percentage figure for the brightness compared to the direct drive case can easily be calculated.

$$\text{percent muxed brightness} = \frac{t_{DON}}{t_D \times \text{nd}} \times 100$$

$$\text{percent muxed brightness} = \frac{t_{DON}}{(t_{DON} + t_{DOFF})\text{nd}} \times 100$$

Thus, regardless of the display logic's refresh speed, the display brightness will obviously depend on the amount of multiplexing and the amount of inter-digit blanking time. This is one constraint limiting the multiplexing scheme, and display manufacturers' data sheets should be consulted to determine a display's limits. This will, to a large degree, determine whether a design should use 32-digit multiplexing or perhaps two separate 16-digit multiplexed displays.

There are also limitations on the refresh rate based on the speeds of the hardware. In this design, the "on" time has a minimum value given by the time required to load the start bit and the first 34 data bits of the MM58348/248, i.e., the time required for 35 clock pulses of the MM58348. The MM58348 has a maximum clock frequency of 1 MHz, so the minimum time for 35 clock pulses is 35/(1 MHz) = 35 µs.

The digit "off" time is constrained by the time required to clock the digit driver and to load the final segment data bit, or the time for the display outputs to switch off then on, whichever is greater. The MM58341 has a maximum clock frequency of 800 kHz, so the minimum digit "off" time due to driver limitations is related to 1/(800 kHz) + 1/(1 MHz) = 2.25 µs. The blanking signal must be active during this time. Also, though the display outputs take typically 20 µs to switch, the display itself limits the minimum digit "off" time and is actually 20 µs.

Thus, the minimum total digit time per digit is:

$$t_D = 35\ \mu s, + 20\ \mu s = 55\ \mu s.$$

At a refresh rate of 10 ms, 10 ms/55 µs equals the theoretical maximum number of digits that can be multiplexed, or about 180 35-segment characters. This is unrealizable since current display "on" times must be greater than 35 µs, and total digit duty cycles (or percent brightness) must be much higher.

$$\text{percent brightness} = \frac{25\ \mu s}{55\ \mu s \times 180} \times 100 = 0.25\%$$

For the 32-digit case, the percent brightness is more realistic:

$$\text{percent brightness} = \frac{0.29 \text{ ms}}{0.31 \text{ ms} \times 32} \times 100 = 2.9\%$$

These times are the limits of the drivers. If the time required to load them is limited by the speed of the controlling processor, the update times are calculated from the clock rates of the controlling µP. However, as one can see, the limitations are more likely due to the display.

4.5 VF Display Brightness Control

Generally, to control or vary the brightness of a display, one can either vary the display drive voltage or vary the "on" time duty cycle by applying a signal to the blanking control. The duty cycle of the blanking signal will determine the brightness. This latter technique is preferred since more predictable behavior results.

In the simple direct drive case the MM58241/341/242/342 must be used. A periodic waveform is applied to the blanking pin. Its frequency should be greater than 100 Hz–200 Hz. As the duty cycle is varied, the percentage of time that the digits are "on" is changed and the perceived brightness changes.

In a multiplexed application, the brightness can be altered by merely modifying the relative length of the inter-digit blanking signal. This is easily accomplished in the software of the controlling µP by adding a delay while the blanking signal is active and subtracting the same delay from the time the blanking signal is inactive.

The relative brightness is the percentage of time that any one character is "on" divided by the sum of the character's "on" and "off" times. The latter term was previously defined as the total digit time. Thus:

$$\text{relative brightness} = t_{DON}/t_D.$$

Due to hardware refresh update speed limitations, 100% and 0% brightness cannot be achieved and also maintain proper refreshing, although 0% can be achieved just by stopping refresh and blanking continuously. (Note that this percentage is relative to the theoretical minimum and maximum brightness for a given multiplexed display, not the brightness relative to a direct drive display as was done previously.)

In the above 32-digit example, the maximum brightness is (assuming 10 ms refresh rate and 20 µs minimum inter-digit blanking):

$$\text{max. percent brightness} = (0.29 \text{ ms}/0.31 \text{ ms}) \times 100 = 93.6\%.$$

The minimum brightness, assuming 35 µs minimum "on" time is:

$$\text{min. percent brightness} = (0.035 \text{ ms}/0.31 \text{ ms}) \times 100 = 11.2\%.$$

Clearly there is a large range of available display brightness levels which are easily software controllable by altering the duty cycle of the blanking signal.

Again, the above analysis assumes that the microprocessor unit is interfacing with the display drivers at their maximum data rates. If this is not the case, some part of the brightness range will be lost.

Refer to Appendix for general system considerations.

5.0 THE SOFTWARE

Having outlined the general method by which the data can be displayed, it now remains to demonstrate how this can be achieved at the microprocessor level. It was thought best to use a familiar microprocessor for this task, so the implementation will use a 6502 and 6522 VIA circuit. The procedure which will be described is merely one example of how these display drivers can be applied, and it is hoped that by concentrating on the arranging and loading of the data, a more general benefit will be gained.

The application to be described here is that of an alpha-numeric display where characters are entered from a keyboard onto a VF display, feeding in from the left. The program will also accept control codes such as line feed, delete, etc. The general flowchart for this routine is shown in *Figure 9*. When the character is collected from the keyboard buffer it must first be established that it is a valid ASCII code; if not, it is ignored and the present data will continue to be displayed. The next thing to check is whether it is a control code. If it is a control code, the function represented must be executed on the existing data and the resulting data displayed. Assuming the ASCII code is not identified as a control code, it must correspond to a display character, and hence will be entered at the start of the display data buffer. Following this, the 32 characters denoted by the contents of the display data buffer are displayed, and after the last digit is enabled the keyboard buffer is checked for new data. As the display refresh rate far exceeds the speed of the human typist, each set of data is displayed several times before it changes.

Looking at the routine for displaying the 32 digits in more detail, a flowchart can be drawn up, as shown in *Figure 10*.

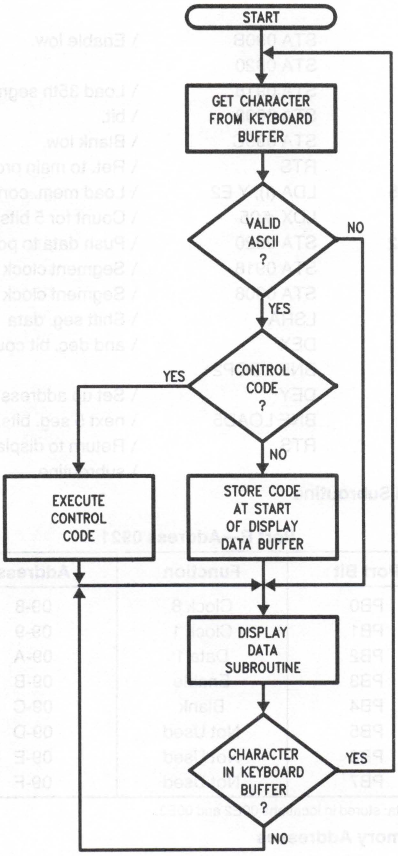
START
GET CHARACTER FROM KEYBOARD BUFFER
VALID ASCII ?
NO
YES
CONTROL CODE ?
YES
NO
EXECUTE CONTROL CODE
STORE CODE AT START OF DISPLAY DATA BUFFER
DISPLAY DATA SUBROUTINE
CHARACTER IN KEYBOARD BUFFER ?
YES
NO

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FIGURE 9. General IC Flowchart

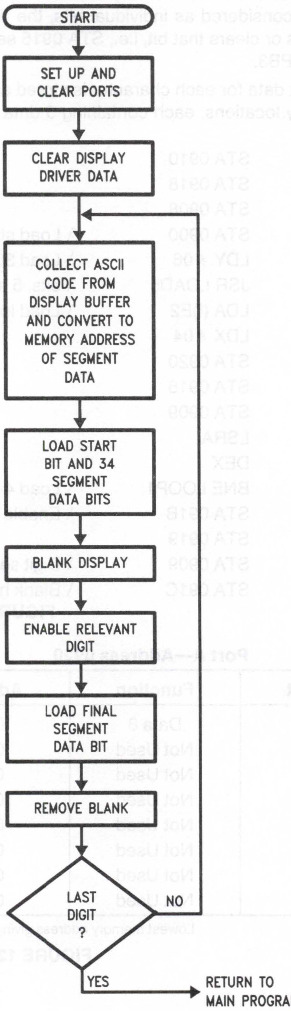
START
SET UP AND CLEAR PORTS
CLEAR DISPLAY DRIVER DATA
COLLECT ASCII CODE FROM DISPLAY BUFFER AND CONVERT TO MEMORY ADDRESS OF SEGMENT DATA
LOAD START BIT AND 34 SEGMENT DATA BITS
BLANK DISPLAY
ENABLE RELEVANT DIGIT
LOAD FINAL SEGMENT DATA BIT
REMOVE BLANK
LAST DIGIT ?
NO
YES
RETURN TO MAIN PROGRAM

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FIGURE 10. Display Data Subroutine Flowchart

5.0 THE SOFTWARE (Continued)

After first setting up and clearing the port lines and both the display drivers, a routine is performed for each of the 32 display characters. The ASCII code is collected and decoded to reveal memory locations where the corresponding 35 segment bits are stored. The start bit and first 34 data bits are loaded into the MM58348. Then the MM58341 blank signal is activated while the relevant digit is enabled and the final segment is loaded. After blank is removed, the next ASCII code is collected and decoded, etc. When the last digit has been loaded, control returns to the main program for the updating of the display data.

The machine code routine for the setting up of each digit of display data is shown in *Figure 11*. The relevant addresses of ports and digit codes are included in *Figure 12* to make the program comprehensible. The address of the segment data is stored in locations 00E2 and 00E3, and it is assumed that this is updated outside the display subroutine. The ports can be addressed as 8-bit memory locations or as individual lines. When considered as individual bits, the fifth address bit either sets or clears that bit, i.e., STA 0915 sets PA5 and 090B clears PB3.

The segment data for each character is stored as 7 consecutive memory locations, each containing 5 data bits.

The contents of each location are loaded into port A via the accumulator, starting with the highest memory address. This is achieved by indexing the lowest memory address by the contents of the Y register (starting as 06) and decrementing this register as every 5 bits are loaded. The least significant bit of port A is used for the segment data (PA0) and the 5 data bits are loaded by storing the code to port A, logically shifting it to the right, and storing it to port A again. This procedure is repeated 5 times for each memory location. The code given in *Figure 11* is for the brightest case, i.e., where the blank signal is disabled, as soon as the data has been latched to the display outputs. Clearly, the brightness can be altered by delaying this action.

The data is held in memory in the form of 7 locations of 5 bits each. This format was chosen because each location can be equated to one row of 5 x 7 dot matrix, where the lowest memory location corresponds to the bottom row. For example, if it is desired that a "5" be displayed in the form shown in *Figure 12*, then the 36-bit data stream is as demonstrated. Assuming that the data is stored at the 7 locations starting at address 2120, then the location contents are as denoted in *Figure 13*.

```
DISPLAY    STA 0910
           STA 0918
           STA 0908
           STA 0900        \ Load start bit.
           LDY #06         \ Load 30 segment
           JSR LOAD5       \ bits, 5 at a time
           LDA (I)E2       \ Load lowest addr.
           LDX #04
LOOP1      STA 0920
           STA 0918
           STA 0909
           LSRA
           DEX
           BNE LOOP1       \ Load 4 seg. bits.
           STA 091B        \ Enable high.
           STA 0919
           STA 0909        \ Digit select clock.
           STA 091C        \ Blank high
           STA 090B        \ Enable low.
           STA 0920
           STA 0918        \ Load 35th segment
           STA 0908        \ bit.
           STA 090C        \ Blank low.
           RTS             \ Ret. to main prog.
LOAD5      LDA (I), Y E2   \ Load mem. contents.
           LDX #05         \ Count for 5 bits.
LOOP2      STA 0920        \ Push data to port A.
           STA 0918        \ Segment clock high.
           STA 0908        \ Segment clock low.
           LSRA            \ Shift seg. data
           DEX             \ and dec. bit count.
           BNE LOOP2
           DEY             \ Set up address of
           BNE LOAD5       \ next 5 seg. bits.
           RTS             \ Return to display
                           \ subroutine.
```

FIGURE 11. Display Data Load Subroutine

Port A—Address 0920

Port Bit	Function	Address
PA0	Data 8	09-0
PA1	Not Used	09-1
PA2	Not Used	09-2
PA3	Not Used	09-3
PA4	Not Used	09-4
PA5	Not Used	09-5
PA6	Not Used	09-6
PA7	Not Used	09-7

Port B—Address 0921

Port Bit	Function	Address
PB0	Clock 8	09-8
PB1	Clock 1	09-9
PB2	Data 1	09-A
PB3	Enable	09-B
PB4	Blank	09-C
PB5	Not Used	09-D
PB6	Not Used	09-E
PB7	Not Used	09-F

Lowest memory address giving location of segment display data: stored in locations 00E2 and 00E3.

FIGURE 12. Port and Relevant Memory Addresses

5.0 THE SOFTWARE (Continued)

Desired Display Character (Numeric 5)

```
XXXXX     row 1
X         row 2
X         row 3
XXXX      row 4
    X     row 5
X   X     row 6
 XXX      row 7
```

Desired Data Stream

01110000010000111110100001000011111 | 1 |

start
bit

direction of data entry →

Memory Contents (Assuming Lowest Address = 2120)

Address	Contents	
2120	0E	row 7
2121	11	row 6
2122	01	row 5
2123	1E	row 4
2124	10	row 3
2125	10	row 2
2126	1F	row 1

FIGURE 13. Example of Segment Data Arrangement

An alternative using 5 locations of 7-segment data bits is possible, where the software would be faster but the data formatting more difficult. There are many trade-offs to be found with so versatile a series of circuits.

The code used to demonstrate this example is that of the 6502 microprocessor, and it would be a simple task to convert the instructions for another device (e.g., National's CMOS NSC800). The versatility of display formats available is a major feature, and the fact that these display drivers are CMOS devices guarantees their low power consumption. In addition, the outputs incorporate internal pull-down resistors which greatly reduce the external component count. This cuts the required board area; consequently a considerable saving in system cost can be made.

6.0 CONCLUSIONS

This design example is merely one of the many possible applications for the MM58348/341/248/241 family of high voltage display drivers. For other applications it should be noted that the other 2 circuits in this series, namely the MM58342 and the MM58242, can provide a much wider range of possible connections. For example, larger displays such as the 2-line by 40-digit 5 x 7 dot matrix formats can be driven with two MM58348s and two MM58342s cascaded to form a 40-bit shift register.

The method by which the segment data is shown to be stored and accessed in memory in convenient in the above example, although again it is only one of the many methods.

APPENDIX: SYSTEM CONSIDERATIONS FOR VF DISPLAY DRIVING

The purpose of the following text is to show how a designer can make decisions on displays he can drive or ranges of brightness he can achieve with a given system. Alternatively, it can be used as a method of designing a system to meet a desired display specification.

THE THEORY

1. System Decisions

System Constraints:

a. Refresh rate (f_r)

b. Number of display digits (nd)

c. Rate at which drivers are clocked by system (f_{CLK})

Associated Parameters:

a. Total time available to diplay all digits (t_r)

b. Total time allocated to each digit (t_D)

c. Total time each digit is on (t_{DON})

d. Total time each digit is off (t_{DOFF})

e. Number of display segments (ns)

f. Number of system clocks required to display one digit (nc_{ON})

g. Number of system clocks required to load segment bits (nc)

h. Number of system clocks required to latch both segment and digit data (nc_{OFF})

From the above definitions, the following equations can be stated:

$tr = 1/f_r$ (seconds)

$t_D = t_r/nd = 1/(f_r \times nd)$ (seconds)

t_{DON} = time to load segment bits for next digit

= ns system clocks

= nc_{ON} system clocks

= nc_{ON}/f_{CLK} (seconds)

t_{DOFF} = time to latch segment bits and to enable relevant digit

= nc_{OFF} system clocks

= nc_{OFF}/f_{CLK} (seconds)

Hence:

$t_D = t_{DON} + t_{DOFF}$

$= (nc_{ON}/f_{CLK}) + (nc_{OFF}/f_{CLK})$

$= (nc_{ON} + nc_{OFF})/f_{CLK}$

$= nc/f_{CLK}$ (seconds)

And:

$f_{CLK} = nc/t_D$

$= nc \times f_r, \times nd$ (Hertz)

2. Brightness Variation Considerations

The brightness of the display is proportional to the duty cycle of the blank signal, and the range of intensities available depends on the size of t_{DON} and ultimately the refresh rate, fr.

Bd = brightness of the display

= duty cycle of blank signal

= t_{DON}/t_D

In the above example, the least bright case is where the blank signal is low for only one system clock per digit.

Bd (min) = 1/nc

And the brightest case is where blank is low only for the time required to latch the segment data and enable the digit.

Bd (max) = $(nc - nc_{OFF})/nc$

$= 1 - [(nc_{OFF})/nc]$

The range of available brightness level, Br, is:

Br = Bd (max)/Bd (min)

$= [(nc - nc_{OFF})/nc]/(1/nc)$

$= nc - nc_{OFF}$

It should be noted that this is the minimum range of available brightness levels because t_D was minimized to maximize fr. If the system clock were fast enough to allow the maximum refresh rate to be in excess of the desired fr, then t_D could be increased from its minimum value. This would, in turn, produce a wider range of brightness levels.

It should also be noted that most manufacturers quote a minimum duty cycle for each digit. The system designer should ensure that neither end of the brightness specification exceeds this value.

THE APPLICATION

For the purposes of doing some sample calculations using the above theory, we will assume use of the system previously described, i.e., the driving of a 32-digit 5 x 7 dot matrix display by one MM58341/241 and one MM58348/248.

1. System Decisions

The number of display digits is fixed, i.e., nd = 32 (nc_{ON} = 35 and nc_{OFF} = 2, so nc = 37 system clocks). Assume system has a 125 kHz clock rate.

Therefore, the resulting refresh rate is:

$f_r = f_{CLK}/(nc \times nd)$

$= 125000/(37 \times 32)$

= 105 Hz

Also, the system clock rate needed for a given refresh rate can be calculated, e.g., f_r = 200 Hz.

$f_{CLK} = nc \times f_r \times nd$

$= 37 \times 32 \times 200$

= 237 kHz

= approximately 250 kHz

There are many other examples of how this theory can be used to evaluate the possibilities for VF systems.

2. Brightness Variation Considerations

We can now calculate range of brightness intensities available with the above system, i.e., where f_{CLK} = 125 kHz, f_r = 105 Hz.

Bd (min) = 1/nc

= 1/37

Bd (max) = $1 - (nc_{OFF}/nc)$

$= 1 - (2/37)$

= 35/37

Br = Bd (max)/Bd (min)

= 35

So the brightness can vary from its lowest value to its maximum value, which is 35 times the minimum level.

Also note that the minimum duty cycle for this display is given as 1/40 (manufacturer's specification), so there is no problem in this application.

Let us now take the example of driving the same display with a system where $f_{CLK} = 500$ kHz, at a desired refresh rate of 200 Hz.

$$nc = f_{CLK}/(f_r \times nd)$$
$$= 500000/(200 \times 32)$$

nc_{OFF} is 2 as before, and although we require only 35 clocks to load the segment data,

$$nc_{ON} = nc - nc_{OFF}$$
$$= 78 - 2$$
$$= 76 \text{ system clocks}$$

In general, the higher the system clock rate, the wider the brightness control range.

Therefore,

$$\text{Bd (min)} = 1/nc$$
$$= 1/78$$

But, remembering that Bd (min) must be less than the stated duty cycle (1/40):

$$\text{Bd (min)} = 2/78$$
$$= 1/39$$

$$\text{Bd (max)} = 1 - (nc_{OFF}/nc)$$
$$= 1 - (2/78)$$
$$= 76/78$$
$$= 38/39$$

$$\text{Br} = \text{Bd (max)}/\text{Bd (min)}$$
$$= (38/39)/(1/39)$$
$$= 38$$

So, we can see that by manipulation of the system constraints, a wider range of brightness levels can be attained, although this is ultimately limited by the stated duty cycle of the display.

A Novel Process for Vacuum Fluorescent (VF) Display Drivers

National Semiconductor
Application Note 378
David Stewart

Introduction

The recent introduction of Vacuum Fluorescent (VF) displays has provoked a great deal of interest in the market place in general, and in particular for use in automotive dashboard applications. Consequently, this attention has spread to the wide range of display drivers presently available. To take advantage of these displays, a new form of high voltage driver was required, at a lower cost than the previously available integrated circuit.

The Vacuum Fluorescent (VF) Display

The operation of a VF display is based upon that of a standard valve, where electrons are emitted from the cathode and are accelerated through the grid on to the anode. Initially, a filament element heats the electrons at the cathode, providing the electrons with the necessary energy for emission. If both the grid and the anode are at a positive potential with respect to the cathode, then the emitted electrons pass through the grid and onto the anode. In a VF display, the anode terminal is coated with a fluorescent material, which will emit light when bombarded by electrons. The general structure of such a display is shown in *Figure 1*. The anode areas correspond to individual segments of the display, and the grid is used to switch on and off whole digits, facilitating the option of multiplexed anodes. The brightness of the display varies directly with the voltage difference between cathode and grid/anode, and this has resulted in the need for high voltage drivers.

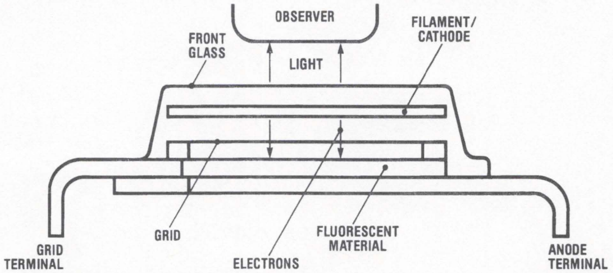
The type of display selected for an automotive dashboard is a critical decision, and there is a wide range from which to choose. Light emitting diode (LED) displays are commonly used in electronic dashboards at present, although they have the serious disadvantage of high power dissipation and a low level of brightness. Given the wide range of applications found for liquid crystal displays (LCD) in recent years, one might expect to find this technique applied to dashboards. However, LCD has the inherent disadvantage of a limited operating temperature range and the low temperature operation demanded in automotive applications results in difficulties when using present LCD technology as a substitute for LED. More modern display techniques, such as gas discharge or plasma, may provide a viable alternative in the future, but the technology has not been sufficiently proven at this stage. A VF display, on the other hand, is well suited to automotive applications because of its high brightness level, relatively low power consumption, and wide operating temperature range. Further, due to the recent introduction of thick and thin film techniques into display device manufacturing processes, it is with relative ease that high volumes of customer designed VF displays can be produced.

The application of VF displays to automotive dashboards demands additional requirements, because of the wide range of environmental conditions under which it must operate efficiently. In particular, it is imperative that the display characters are easily distinguishable in extreme light conditions. The visual recognition of the display information can be optimised readily by means of suitable filtering, and it is also desirable that the character brightness is variable. The latter could be achieved by altering the display voltage in proportion to signals from a light sensor mounted alongside the display on the dashboard.

High Voltage Display Drivers

EXISTING HIGH VOLTAGE DISPLAY DRIVERS

The most common, and indeed the most publicized type of display driver utilizes a mixture of MOS and bipolar technologies. While the logical areas of these devices operate as standard MOS 5V logic, each display output consists of a high voltage (up to 150V) Bipolar buffer. These output structures result from well known npn and pnp design techniques, e.g. emitter follower, Darlington pair, etc., where high output source currents (up to 100 mA) are the aim. These high current circuits appear to be the legacy from high power LED display drivers and, although capable of driving VF displays, such devices have several drawbacks. First and foremost they are expensive, mainly due to the inherent low density of Bipolar technology which, if many display outputs are included in the circuit, can significantly increase die size and hence cost. For certain desired output structures it may be necessary to include extra masking steps to the basic MOS process, e.g. to form an epitaxial layer, and this again will inevitably lead to increased costs. Further, the high current outputs result in very high power consumption on chip which, depending on the package used, may cause problems due to excessive die temperatures. Difficulties associated with power dissipation may lead to a reduction in the number of display outputs per chip, or at least a limitation on the number of segments illuminated simultaneously.



TL/F/8349-1

FIGURE 1. Cross-Section of a Vacuum Fluorescent (VF) Display

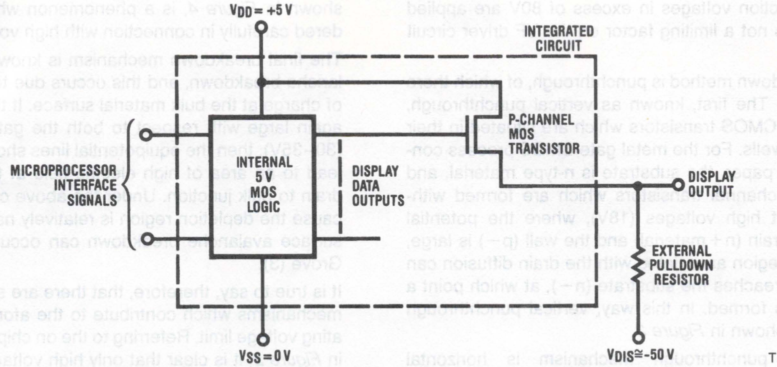


FIGURE 2. Example of a High Voltage MOS Open Drain Structure

Another readily available type of high voltage display driver is fabricated using MOS techniques only. Such devices use PMOS technology, and the high voltage output swings are achieved by means of open drain p-channel output transistors, as shown in *Figure 2*. Significant reductions in chip size can be achieved in this way, although such devices require one external pulldown resistor per display output. Consequently the board component count, and hence the system cost, will increase.

Surveying the literature, several points of interest emerge. First, there is a trend towards including far more decoding and control logic on chip, and it is likely that this has occurred due to the increasing use of high voltage displays in word processor applications. Thus, there is a demand for decoding of both ASCII character display data and ASCII control codes direct from the keyboard. In addition, it appears to be relatively rare to find display drivers with direct TTL data and clock inputs. Some devices cater for RS232 or other standard interface requirements, but many devices require some level shifting circuitry between the data source and display driver inputs.

THE 'IDEAL' VF DISPLAY DRIVER

As has already been stated, the operation of a VF display is similar to that of a valve and hence is a voltage controlled device. In addition, the nature of the fluorescent material is such that the amount of light emerging from the display is directly proportional to both the number of, and the speed at which the electrons arrive at the anode. The number of electrons emitted from the cathode is a function of the current in the filament and as such, has a limit. The acceleration of the electrons, on the other hand, is directly proportional to the voltage between the cathode and the grid/anode. Thus, one major requirement of the VF driver is that it is capable of large output voltage swings between the on and off conditions. At present, typical VF displays operate at a maximum cathode to grid/anode voltage of 50 volts, and so it is essential that the driver can produce output swings of at least 50V.

Coupled with the discussion on output voltage capabilities, an examination of the display output current requirements should be undertaken. The previous conclusion, that the VF display is a voltage controlled device, suggests that high current outputs are not required (typically 5 mA for a segment and 10 mA for a digit). The driver output must charge and discharge the display capacitance in such a time as to avoid visible flickering or ghosting effects. Given that most VF displays now have multiplexed anodes, and that the refresh rate must be greater than 100 Hz to prevent the above effects, then it can be seen that charge/discharge times in excess of 100 µsecs can be tolerated. A typical VF display has a capacitance of 20 pF and if the output off resistance is 200 KΩ, then a discharge time constant of 4 µsecs can be anticipated, more than adequate for the demands of the human eye.

Another desirable characteristic of the VF driver is that it has internal pulldown resistors on each of its display outputs. Thus, the complete structure shown in *Figure 2* can be incorporated on to the integrated circuit, and this will reduce component count and hence cost. The value of this resistor is critical in terms of both output voltage swing and standby power consumption, and as such is a parameter which must be closely defined. In addition, because low power consumption is desirable, the 5V logic on chip should dissipate as little power as possible and for this reason complementary MOS (CMOS) is the optimum processing technology to be used.

The cost of the finished product is closely related to the complexity of the fabrication process used and so the most proven of the available CMOS processes should be chosen. Thus, metal gate CMOS will be the process used.

Standard Metal Gate CMOS Processing

Examining the requirements outlined in the previous section, it is clear that metal gate CMOS design techniques can provide low power 5V internal logic and TTL microprocessor interface inputs with relative ease, using existing methods. Hence, it is the other requirements, namely high voltage outputs and on chip pulldown resistors, which demand closer attention.

OPERATING VOLTAGE LIMITATIONS

The electrical parameters which accompany the CMOS metal gate design rules state that 18V is the maximum voltage of operation of any circuit designed according to those rules. In order to contemplate possible ways by means of which this limitation can be overcome, the mechanisms which cause it must be examined.

In general, it is the phenomenon of breakdown which determines the maximum operating voltage, and there are several methods by which this can occur. One such instance is junction breakdown, where the reverse biased pn diffusion diodes inherent in the process exhibit either avalanche or zener breakdown mechanisms, as described by Bar-lev (1). Under these conditions, the diodes begin to conduct in the reverse direction and clearly this will prevent the circuit from operating as designed. In practice, however, this does not occur until junction voltages in excess of 80V are applied and hence it is not a limiting factor on the VF driver circuit envisaged.

Another breakdown method is punchthrough, of which there are two types. The first, known as vertical punchthrough, occurs only in CMOS transistors which are situated in their own diffusion wells. For the metal gate CMOS process considered in this paper, the substrate is n-type material, and so it is the n-channel transistors which are formed within p−wells. At high voltages (18V), where the potential between the drain (n+material) and the well (p−) is large, the depletion region associated with the drain diffusion can extend until it reaches the substrate (n−), at which point a current path is formed. In this way, vertical punchthrough can occur as shown in *Figure 3*.

The second punchthrough mechanism is horizontal punchthrough, and this normally occurs between drain and source of both n- and p-channel devices. As stated by Hamilton and Howard (2), the threshold voltage of the basic MOS transistor is the voltage required to cause field inversion in bulk material and hence form a drain source channel, the conductive properties of which are controlled by the gate voltage. As before, at high drain voltages (30–35V), a depletion region extends out from the drain diffusion. If the drain (p+ or n+) to bulk (n− or p−) potential is high enough the drain depletion region will reach the source diffusion (p+ or n+) and an uncontrolled drain source channel is formed, causing the transistor to act as a short circuit. Consequently, horizontal drain source punchthrough, as shown in *Figure 4*, is a phenomenon which must be pondered carefully in connection with high voltage applications.

The final breakdown mechanism is known as surface avalanche breakdown, and this occurs due to an accumulation of charge at the bulk material surface. If the drain voltage is again large with respect to both the gate and the source (30–35V), then the equipotential lines shown in *Figure 5* will lead to an area of high electric field at the surface of the drain to bulk junction. Under the above conditions, and because the depletion region is relatively narrow at this point, surface avalanche breakdown can occur as described by Grove (3).

It is true to say, therefore, that there are several breakdown mechanisms which contribute to the aforementioned operating voltage limit. Referring to the on chip structure outlined in *Figure 2*, it is clear that only high voltage p-channel transistors are required, and so vertical punchthrough need not be considered in this case. In addition, junction breakdown will only occur at voltages above those envisaged in this application, and hence horizontal punchthrough and surface avalanche breakdown are the phenomena which must be overcome to facilitate a successful design.

ON CHIP RESISTORS

Due to the nature of CMOS, i.e. because the technology produces both pull-up and pull-down transistors, it is relatively rare to find resistors in such circuits. A further reason for the rare appearance of resistors is that the tolerances on MOS diffusion resistors are so large as to make them unac-

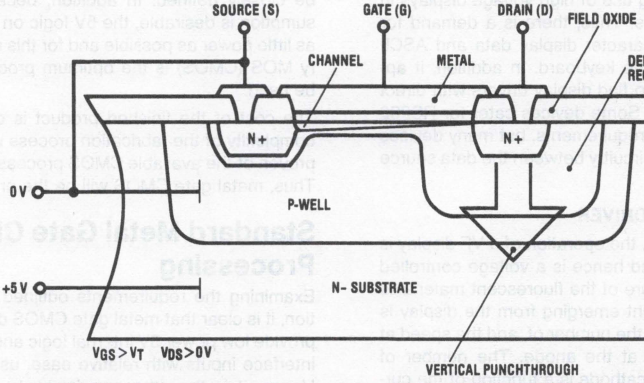


FIGURE 3. Vertical Punchthrough in a CMOS N-Channel Transistor

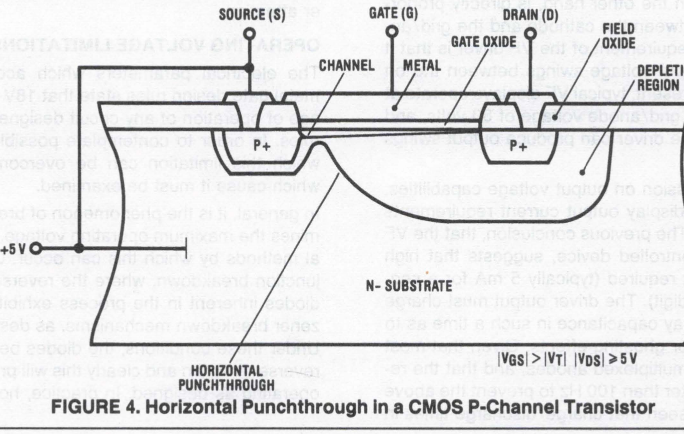


FIGURE 4. Horizontal Punchthrough in a CMOS P-Channel Transistor

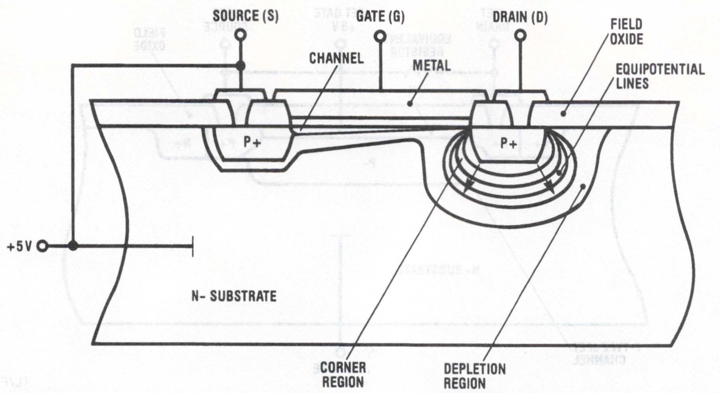


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FIGURE 5. Surface Avalanche Breakdown in a CMOS P-Channel Transistor

ceptable in normal applications. One occasion where such resistors are used is where it is only the ratio between the resistors which is important, and not their precise values, for instance in a voltage divider. Under these circumstances, any change in the nominal resistance value will be reflected in all the resistors and hence the divider will operate as designed.

As was pointed out above, such resistors are normally formed by making use of the sheet resistance of diffusion. In particular, the diffusion with the highest value of sheet resistance is used, and this is p-material. Hence, the structure shown in *Figure 6*, known as a pinched p− resistor, is common, and it is clear that this device is in fact a p-channel junction field effect transistor (JFET). The theory of JFET operation is described by Glaser and Subak-Sharpe (4), and because the p− diffusion process is followed by n+ diffusion it can be seen that the JFET gate completely surrounds the p-type channel region in the form of n+ and n− (substrate) material, which is tied to 5 volts. For this reason, the pinch-off voltage is very low (typically 10V) and so these pinched resistors are widely used in low voltage applications. Further, p− diffusion sheet resistance is a parameter which has a wide process spread, i.e. 4.5–7.0 kΩ per square, and although the pinched resistor technique increases this nominal resistance value due to depletion effects, such resistors are difficult to specify in advance.

If the large changes in resistance value are not tolerable then p+ diffusion resistors in the n− substrate are a viable alternative, for two reasons. First, because of the doping profile of p+ diffusion, the JFET depletion effects are reduced, and consequently such resistors have a much higher pinch-off voltage. Second, the nominal resistance of p+ diffusion is much more stable over the process range, although its value is far lower (40–80Ω per square). For this latter reason, p+ resistors occupy large areas for relatively small values.

High Voltage CMOS

Referring to the 'Ideal' VF Driver section, one of the principal aims of this design is that a standard fabrication process be used. Bearing that in mind then, there follows a study of possible ways by which the original VF display driver specification could be realised or even enhanced.

HIGH VOLTAGE TRANSISTORS

The simpler of the two operating voltage limitation factors to overcome is horizontal punchthrough. From *Figure 5*, it is clear that in order to increase the drain source voltage at which the depletion regions combine the distance between the drain and source must be increased. This has the effect of lengthening the transistor channel, and the consequences of such action should be considered. The basic equations which describe the mode of operation of the MOS transistor are derived by A.M.I. (5), and from these, increasing the channel length (L) will result in lower drain source current (I_{DS}), lower gain factor (β), and higher threshold voltage (V_T). All of these effects will degrade the transistor performance, although it is worth noting that the aspect ratio (W/L), i.e. the ratio of channel width (W) to its length, is a major component of the transistor equations. Hence, some performance can be salvaged by increasing the channel width to return the aspect ratio to its original value. Unfortunately, this approach increases gate area and hence parasitic capacitances, and so the resulting high voltage transistor is still inferior to its low voltage equivalent.

The other mechanism which leads to high voltage breakdown in MOS transistors is surface avalanche breakdown, and this phenomenon can only be overcome at a cost. As was explained previously in reference 3, this avalanche effect is caused by a region of high electric field which can lead to electrons with energy levels high enough to start a chain reaction of collisions within the silicon lattice. The electric field at the corner (ξcorner) determines whether this phenomenon will occur and reference 3 points out that ξcorner is inversely proportional to gate oxide thickness (t_{ox}). Armed with this information, initial experiments were carried out with long channel devices having t_{ox} values ranging from the standard process value of 1000Å up to a maximum possible value of 2300Å. In practice, the oxidation cycle had to be altered to allow these different oxide thicknesses to be fabricated without affecting other process parameters. As a result of these experiments, it was found that surface avalanche breakdown occurred at approximately 40V with $t_{ox} = 2300$Å. An alternative experiment involved making use of the oxide which isolates the silicon from the metal inter-connect, that known as field oxide. Field oxide is typically 8800Å thick, and hence it was felt that using this as gate oxide on long channel devices could provide the desired high voltage performance. However, field oxide MOS transistors were found to have breakdown voltages in excess of 70V, and for this reason it was decided that the VF driver outputs would be designed for a maximum voltage swing of 60V. The high breakdown voltage, however, is achieved at a cost in terms of performance. Using the basic MOS transistor equations of reference 5, and noting that increasing t_{ox} will decrease gate capacitance (C_{ox}), it is clear that low values of gain factor ($\beta \cong 1\ \mu A/V^2$), and high

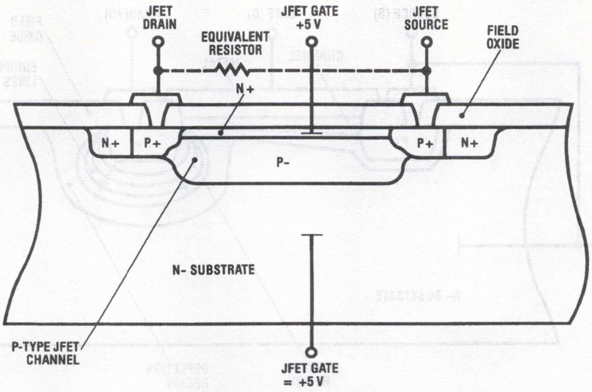

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FIGURE 6. P-Pinched Resistor

values of threshold voltage ($V_T \cong -6V$) are expected. If these performance limitations are taken into account at the design stage, then high voltage p-channel MOS transistors are feasible.

The high voltage transistors outlined above are an ideal solution to the display output problem, as their fabrication requires no additional processing stages.

HIGH VOLTAGE PULLDOWN RESISTORS

Before looking at ways in which the high voltage pulldown resistors may be realised, a definitive value for this resistor should be assigned. It is essential that the resistor value is low enough that any leakage current from the p-channel transistor does not cause the output voltage, when the output is in the off state, to be significantly higher than the display voltage. If maximum values of expected leakage current are of the order of 10 μA and if the maximum output off voltage to display voltage difference is 2 volts, then the maximum resistance value is 200 kΩ. In addition it is desirable to minimise the current taken on chip when the output is in the on state. Given that approximately 60V will appear across the resistor under these circumstances and if the maximum desired on current is 600 μA per output, then the minimum resistance value is 100 kΩ. Clearly, there is a trade off in performance between the above two requirements, and if the design is centered about a resistance value of 150 kΩ then any variation due to process spread should not cause this value to drop below 100 kΩ or rise above 200 kΩ.

Having established the value of the resistor to be designed, it only remains to decide the method by which this is to be achieved. Unfortunately, neither of the two methods outlined previously can be applied in this case. P+ diffusion resistors are not practical because the nominal resistance per square of such material is too low, typically 60Ω per square, making such resistors occupy excessive amounts of die area. A p− pinched resistor, on the other hand, will pinch-off at voltages in excess of 10V, and hence such a technique is not applicable.

Given the size of the resistor required, and in order that the die area be minimised, a technique using the p− diffusion should be sought. The problem is to ensure that a resistor of this type does not pinch-off at the voltages anticipated, and hence a method whereby the channel depletion effects may be minimised must be found. The first way in which these effects can be reduced is to increase the width of the p− resistor region. This results in an increase in the voltage required to pinch-off the channel, although in the case of pinched p− resistors an intolerably large increase in area is required to allow high voltage (in excess of 50V) operation. If, however, the n+ diffusion layer shown in *Figure 6* is removed, then the JFET channel is only depleted from three, instead of four sides. Experiments showed that if the p− was simply diffused into the native n-type substrate without an n+ covering, and if the channel was sufficiently wide, then p− resistors with pinch-off voltages in excess of 60V could be fabricated. Secondary tests showed that the p− sheet resistance doubled in this mode from its unbiased value, although this parameter is closely dependent on the drain to substrate potential.

Hence, the objective of high voltage on chip pulldown resistors has been realized with no alterations to the standard fabrication process.

DISPLAY DRIVER IMPLEMENTATION

As discussed previously, the microprocessor interface inputs are TTL compatible and the internal data handling CMOS logic operates from a 5 volt supply. The display data emerges from this logic and enters a bank of level shifters, which convert the 0 → 5V waveforms into −10 → 5V levels. In this way, a p-channel field oxide transistor can be driven. The output section is in the form of a pre-buffer followed by a display output driver and a schematic of the whole circuit is shown in *Figure 7*.

Examining the schematic in more detail, it is clear that the −10V supply to the level shifting stage (V_{ee}) is derived by means of a p− resistor ladder between V_{ss} (0V) and V_{dis} (−55V). The sizes of both the p-channel field device and the p− resistor in the pre-buffer stage are non-critical, as they merely drive the next stage, except to state that the p-channel is 16 μm long and the p-resistor is 10 μm wide. In fact, it is desirable that the p-resistor has a high resistance value as this minimises the circuit current when the display outputs are in the off state (pre-buffer is on). The output driver stage, on the other hand, demands a more structured approach. Using the design figure of 10 kΩ per square, a p− resistor size of 16 squares was used, i.e. a region of p− diffusion which was 15 μm by 240 μm. The p-channel field transistor was selected to have an output on impedance of 1.5 - 2.0 kΩ, and to achieve this a size of 300 μm by 16 μm was chosen. The low VF display currents result in this high output on impedance being accepted.

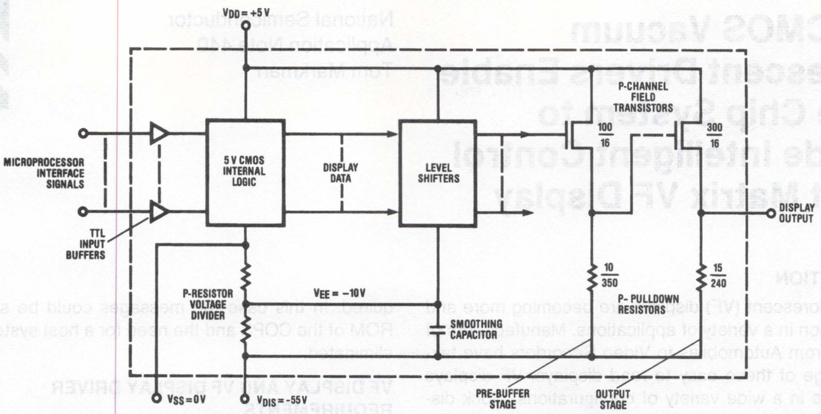
$V_{DD} = +5V$
MICROPROCESSOR INTERFACE SIGNALS
TTL INPUT BUFFERS
5V CMOS INTERNAL LOGIC
DISPLAY DATA
LEVEL SHIFTERS
P-CHANNEL FIELD TRANSISTORS
100/16
300/16
DISPLAY OUTPUT
P-RESISTOR VOLTAGE DIVIDER
$V_{EE} = -10V$
10/350
15/240
P-PULLDOWN RESISTORS
SMOOTHING CAPACITOR
PRE-BUFFER STAGE
OUTPUT STAGE
$V_{SS} = 0V$
$V_{DIS} = -55V$

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FIGURE 7. VF Display Driver Circuit Schematic

The Future

Clearly, the future for VF display drivers is highly dependent upon the way in which such displays progress over the next few years. Further experiments with high voltage p-channel transistors suggest that voltages in excess of 100V can be sustained, although this work is at present only at the initial evaluation stage. Hence, if future VF displays demand operating voltages of this order, compatible drivers should be feasible.

At present, there is considerable interest in Front Luminous VF Displays (FLVD), and it is claimed they provide better visual character recognition and a wider viewing angle. This is achieved by reversing the order of the component parts of the VF display shown in *Figure 1*. Hence, the luminous material is directly beneath the front glass, and so the light is unimpeded as it is emitted from the display. Fortunately, however, the driving requirements of FLVD are similar to those of the present VF display, and so the display drivers outlined in this paper appear adequately to meet the needs of the VF displays of today.

Conclusions

The display drivers described in this application note have demonstrated how a fabrication process, thought only to be applicable to low voltage designs, can be extended to produce high voltage circuits. This suggests that the standard processes of today may also be stretched in other directions. If closer attention is given to the mechanisms behind the circuit and process limitations, then it is possible, as in this case, that they can be overcome. Clearly, if this is achieved the rewards of a wider range of products from the same fabrication process will follow.

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New CMOS Vacuum Fluorescent Drivers Enable Three Chip System to Provide Intelligent Control of Dot Matrix VF Display

National Semiconductor
Application Note 440
Tom Markman

INTRODUCTION

Vacuum Fluorescent (VF) displays are becoming more and more common in a variety of applications. Manufacturers of everything from Automobiles to Video Recorders have taken advantage of these easy to read displays. VF displays are available in a wide variety of configurations; clock displays, calculator displays, multi-segment, and dot matrix displays are readily available at a low cost. This application note develops and covers in some detail a small CMOS system consisting of a single chip microcontroller and two display drivers which control a 20 character, 5 x 7 dot matrix VF display.

Figure 1 shows the schematic of the system. The microcontroller, a COPS™ 424C, receives a character in ASCII form from the host system, stores the ASCII value of the character in its onboard RAM, converts the ASCII value to a 5 byte data word suitable for the display drivers and displays it on the VF display. The COPS also refreshes the display continuously while performing character update, much like a dumb terminal. Not including the address decoding logic, this application requires only the onboard RAM and ROM of the COPS424C, and National's MM58341 and MM58348 VF display drivers. If a steady message or a scrolling sentence is desired, only small changes in the COPS software are required. In this case the messages could be stored in the ROM of the COPS and the need for a host system would be eliminated.

VF DISPLAY AND VF DISPLAY DRIVER REQUIREMENTS

The display used in this application was an Itron #DC205G2. This 20 segment, 5 x 7 dot matrix, multiplexed display required a filament voltage of 5.7 Vac and a filament current of 37 mAac. The anode and grid voltages were supplied by the display drivers. The voltage and current requirements vary considerably for different displays depending on the size and number of characters, and the configuration (dot matrix, 7 segment, 14 segment, etc.). To determine the voltage requirements for a particular display, a simple calculation can be made. If maximum possible brightness of the display is desired, the following equation must be true:

$E_t \geq E_b + E_k + (I_b)\,(R_{on})$ where:

E_t is the total Voltage of the display drvier or $|V_{dis}| + V_{dd}$

E_k is the display Cathode Bias Voltage

$E_b = E_c$ is the typical Anode or Grid Voltage ($V_{p\text{-}p}$)

I_b is the typical anode current (mAp-p)

R_{on} is the display driver output impedance (Ω)

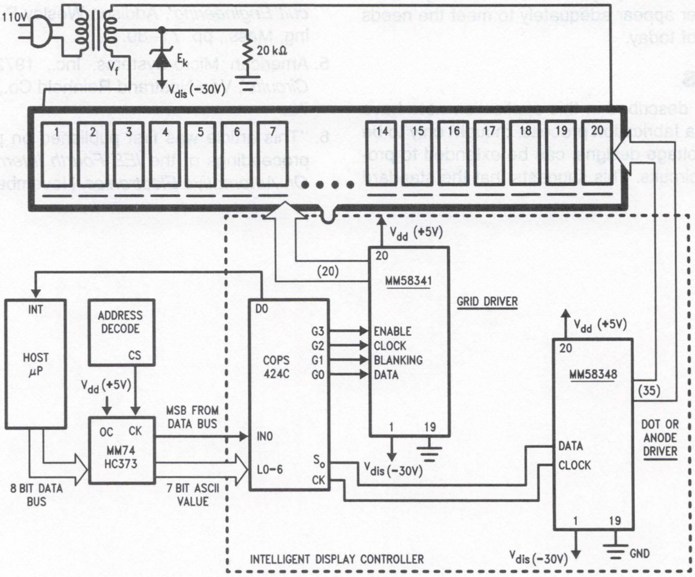
110V
V_f
E_k
20 kΩ
V_{dis} (−30V)
1
2
3
4
5
6
7
14
15
16
17
18
19
20
V_{dd} (+5V)
20
(20)
MM58341
GRID DRIVER
INT
HOST
μP
ADDRESS
DECODE
CS
V_{dd} (+5V)
OC
CK
MM74
HC373
MSB FROM
DATA BUS
D0
COPS
424C
G3
G2
G1
G0
ENABLE
CLOCK
BLANKING
DATA
IN0
L0-6
S_o
CK
1
19
V_{dis} (−30V)
V_{dd} (+5V)
20
MM58348
(35)
DOT OR
ANODE
DRIVER
DATA
CLOCK
1
19
8 BIT DATA
BUS
7 BIT ASCII
VALUE
INTELLIGENT DISPLAY CONTROLLER
V_{dis} (−30V)
GND

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FIGURE 1. System Diagram Showing the Basic 3-Chip Display Controller and the Interface to a Microprocessor System

If the maximum brightness is not desired, the following equation can be used: $(E_t)(1.2) \geq E_b + E_k + (I_b)(R_{on})$. In this application, the calculated E_t was 42.25V, however, the display was legible under normal lighting conditions, with an E_t as low as 25V. If your display requires more than the 35V output of the MM58341 and MM58348, pin for pin compatible 60V VF Display Drivers (MM58241, MM58248) are available.

Figure 2 shows the relationship between the required VF display voltages. The cut-off voltage (E_k) is set by the Zener diode on the center tap of the filament transformer. This value is given in the VF display data sheet.

Avoiding Flicker and Pulsing

There are two different conditions which may cause the display to appear to flicker. The first is the refresh rate. This is particularly a problem on displays where the micro-controller must up-date more than 25 characters. Since the human eye begins to notice flicker at about 40 Hz, a display with a refresh rate less than that will appear to be flashing on and off.

The second type of flicker occurs when the refresh rate is between 40 Hz and 90 Hz. In this case, the display will appear to be rolling rather than flashing. This condition occurs when the refresh rate and the filament frequency are close together. If a character is only on during the time when the filament voltage is negative, it will appear to be slightly brighter than the character next to it which may only be on during the positive cycle of the filament voltage. If this is the case, as it was in this application, the simplest solution is to increase the frequency of the filament. A DC oscillator circuit, such as the one shown in *Figure 3*, can be used to replace the AC voltage source. The filament frequency can be easily adjusted to eliminate this condition.

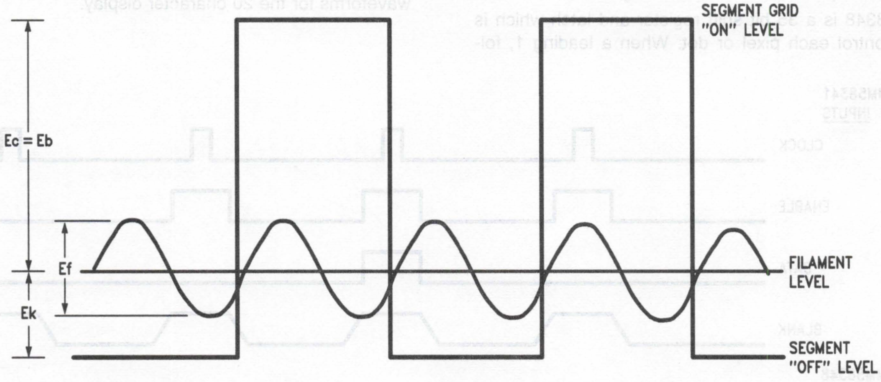

FIGURE 2. Voltage Levels for VF Display

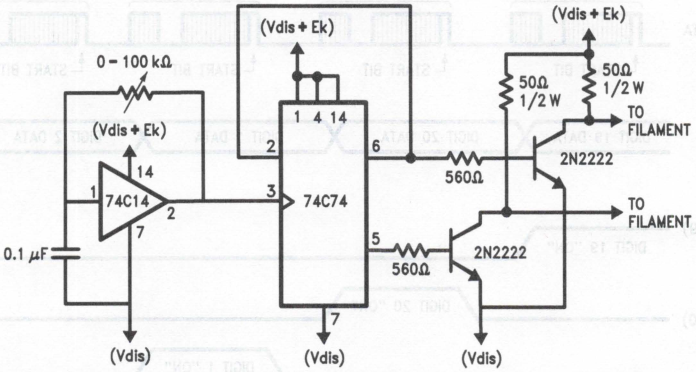

FIGURE 3. Filament Oscillator Circuit

VF Display Drivers

Two high voltage display drivers were needed to control the VF display. A MM58341, was used to control the grids and a MM58348 was used to control the individual pixels or anodes. Both of these drivers receive serial information and output 32 and 35 segments of data respectively.

The MM58341 has three control pins which make it ideal for controlling the grids of a VF display. The blanking control pin will turn off all segments of the display when a logic '1' is applied to this pin. This is particularly important for reducing ghosting, and controlling brightness. Ghosting is a condition where the last characters shadow appears behind the character being displayed. The enable pin acts as an envelope for the input signal. Only while it is at a logic '1' level will the circuit accept clock inputs. When the pin goes low, all the data is latched and displayed. A data out pin is also provided for cascading. If the display has more than 32 grids, a second grid driver can be cascaded by connecting the data out pin to the input data for the second grid driver.

The MM58348 is a 35 bit shift register and latch which is used to control each pixel or dot. When a leading 1, followed by 35 bits of data, is received, the data is latched and displayed. The chip is automatically reset upon power up.

MULTIPLEXED DISPLAY REFRESH TIMING

Considering first the digit driver (MM58341), it becomes clear that the digits must be enabled or refreshed sequentially and that this process must be continuous regardless if the display data has changed. The data for the MM58341 is simply a 1 followed by 19 zeroes where the 1 is shifted through the internal registers of the MM58341. As each digit is enabled, the corresponding segment data is displayed. To insure that no ghosting effects are seen during the transition between digits, the blanking control is activated just before the data is latched into the dot or anode driver and deactivated just after the data has been latched. During this time when the blanking control is activated, the grid driver is clocked shifting the 1 to the next location. *Figure 4* shows the micro-controller waveforms and the resultant display waveforms for the 20 character display.

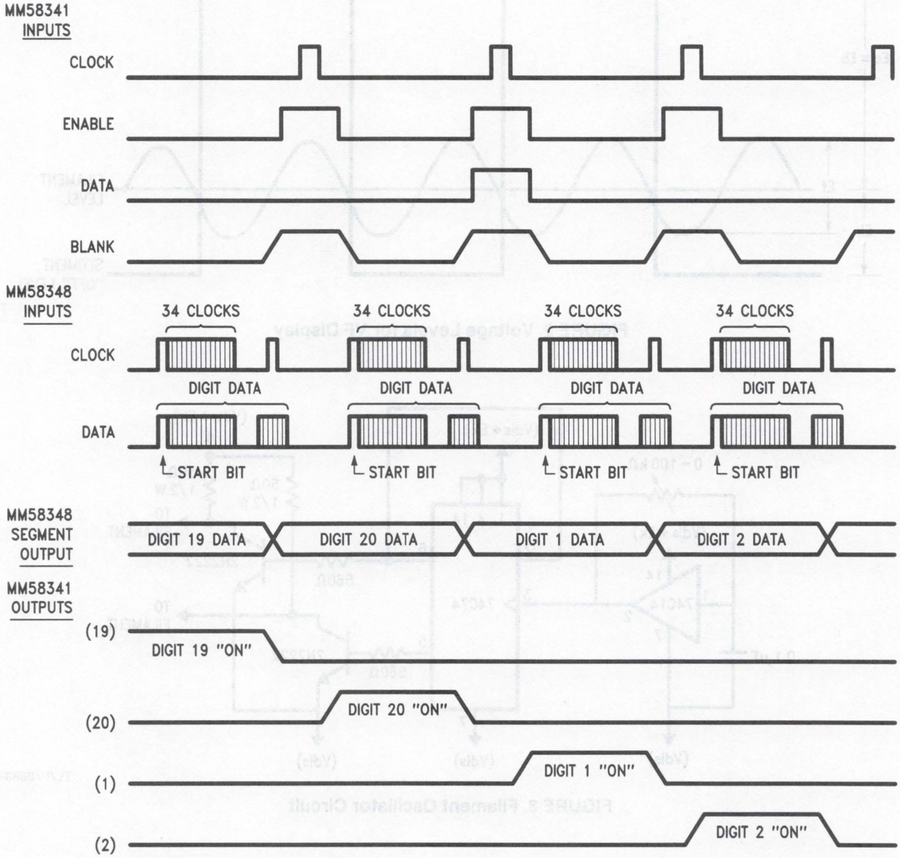
MM58341 INPUTS
CLOCK
ENABLE
DATA
BLANK
MM58348 INPUTS
34 CLOCKS
34 CLOCKS
34 CLOCKS
34 CLOCKS
CLOCK
DIGIT DATA
DIGIT DATA
DIGIT DATA
DIGIT DATA
DATA
START BIT
START BIT
START BIT
START BIT
MM58348 SEGMENT OUTPUT
DIGIT 19 DATA
DIGIT 20 DATA
DIGIT 1 DATA
DIGIT 2 DATA
MM58341 OUTPUTS
(19)
DIGIT 19 "ON"
(20)
DIGIT 20 "ON"
(1)
DIGIT 1 "ON"
(2)
DIGIT 2 "ON"

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FIGURE 4. Timing Diagram

In between digit strobes, the segment data is updated. The first 34 bits of segment data are set up in the dot driver and the blanking signal is activated to disable all 20 digits. The 35th bit of data is clocked in, updating the segments. Since the MM58348 resets its internal shift register each time the data is latched, it can accept all but the final data bit while still displaying the previous digit. The digit driver is then clocked, shifting the digit strobe to the next position. The enable is then brought low, enabling the next digit. Finally blanking control is deactivated and the data displayed.

During the time which the blanking control is high, the order in which the segments or the digits are updated is not critical. Since this occurs while the display is blank. The digit driver may be clocked first, or the segments could be changed first. In general, the philosophy for the driving this VF multiplexed display is outlined in *Figure 5*.

HOST INTERFACE AND PROGRAMMING

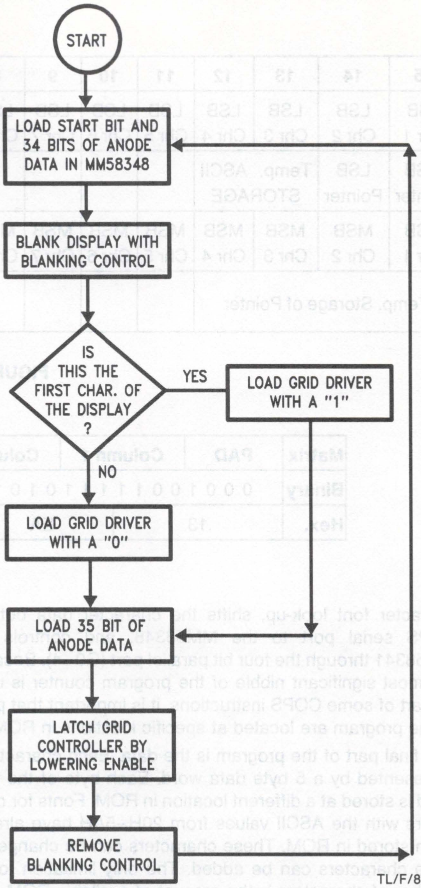
With a minimal amount of address decoding and an eight bit latch, COPS can be interfaced with a common microprocessor bus. When a character has been input into the host to be displayed, the ASCII value of that character is latched into the eight bit latch (MM74HC373) and is read on the L port (L0–6) of the COPS. The MSB of the ASCII value must be a logic 1. This MSB is the signal to the COPS that a new character is being presented. Once the character has been stored, an interrupt is sent from the COPS to the host through the D-0 port. The COPS checks for a new character being input every 200 μs. If a character is being sent, 1 ms is required to store that character in the RAM of the COPS. With the COPS controlling the display, the host microprocessor is not being tied down with character look-up and display refresh. A simple flowchart of the host requirements is shown in *Figure 6*.

COPS SOFTWARE

There are four main sections of the COPS software. The first section, the initialization of the RAM, sets up the RAM as shown in *Figure 7*. A '0' is stored in all of the LSB positions and a '2' is stored in all of the MSB positions. Since the COPS is in a constant display loop, this is necessary to insure a blank display. 20H is the ASCII value of a space. With the RAM set up in this way, a maximum of 28 characters can be stored in RAM. Since the display in this application is only 20 characters long, RAM locations M1,4 to M1,11 and M3,4 to M3,11 are not used. RAM locations 1,12 to 1,15 and 3,12 to 3,15 are used as temporary storage throughout the program and cannot be used for character storage.

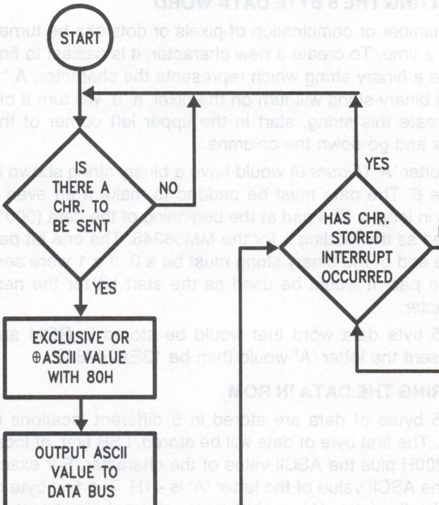
The second part of the program, stores the new characters sent by the host CPU in RAM. Once a character has been sent, this section of the program checks the ASCII value of that character to see if it is a control character or a display character. If it is a display character, the character is stored in RAM and an interrupt is sent to the host. There are three control characters which the COPS program will recognize. Cursor forward (ASCII value 08H) moves the cursor forward without destroying the data, cursor backwards (ASCII value 0CH) moves the cursor backwards without destroying the data, and return (ASCII value 0DH) will clear the display and put the cursor at the beginning of the display. To recognize and store a character, 1 ms is required.

The third part of the program, the display loop, is the heart of the program. Unless a new character has been detected, the program is always in this loop. This section does the


START
LOAD START BIT AND 34 BITS OF ANODE DATA IN MM58348
BLANK DISPLAY WITH BLANKING CONTROL
IS THIS THE FIRST CHAR. OF THE DISPLAY ?
YES
LOAD GRID DRIVER WITH A "1"
NO
LOAD GRID DRIVER WITH A "0"
LOAD 35 BIT OF ANODE DATA
LATCH GRID CONTROLLER BY LOWERING ENABLE
REMOVE BLANKING CONTROL

TL/F/8683–5

FIGURE 5. Flowchart for Display Drivers


START
IS THERE A CHR. TO BE SENT
NO
YES
HAS CHR. STORED INTERRUPT OCCURRED
YES
NO
EXCLUSIVE OR ⊕ASCII VALUE WITH 80H
OUTPUT ASCII VALUE TO DATA BUS

TL/F/8683–6

FIGURE 6. Host System Flowchart

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
LSB Chr 1	LSB Chr 2	LSB Chr 3	LSB Chr 4	LSB Chr 5	LSB Chr 6	LSB Chr 7	LSB Chr 8	LSB Chr 9	LSB Chr 10	LSB Chr 11	LSB Chr 12	LSB Chr 13	LSB Chr 14	LSB Chr 15	LSB Chr 16	M0
MSB Pointer	LSB Pointer	Temp. ASCII STORAGE										LSB Chr 17	LSB Chr 18	LSB Chr 19	LSB Chr 20	M1
MSB Chr 1	MSB Chr 2	MSB Chr 3	MSB Chr 4	MSB Chr 5	MSB Chr 6	MSB Chr 7	MSB Chr 8	MSB Chr 9	MSB Chr 10	MSB Chr 11	MSB Chr 12	MSB Chr 13	MSB Chr 14	MSB Chr 15	MSB Chr 16	M2
Temp. Storage of Pointer												MSB Chr 17	MSB Chr 18	MSB Chr 19	MSB Chr 20	M3

FIGURE 7. COPS RAM Map

Matrix	PAD	Column 1	Column 2	Column 3	Column 4	Column 5	PAD
Binary	0 0 0 1 0 0 1 1 1 1 1 0 1 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 1 1 1 1 1 0						
Hex.	13		EA	24	28	3E	

FIGURE 8

character font look-up, shifts the character data out the COPS serial port to the MM58348, and controls the MM58341 through the four bit parallel port (G0–4). Because the most significant nibble of the program counter is used as part of some COPS instructions, it is important that parts of the program are located at specific locations in ROM.

The final part of the program is the data. Each character is represented by a 5 byte data word. Each byte of the data word is stored at a different location in ROM. Fonts for characters with the ASCII values from 20H–5AH have already been stored in ROM. These characters can be changed or more characters can be added. The only limitation to the number of characters is the amount of available ROM.

CREATING THE 5 BYTE DATA WORD

Any number or combination of pixels or dots can be turned on at a time. To create a new character, it is easiest to first create a binary string which represents the character. A '1' in the binary string will turn on the pixel, a '0' will turn it off. To create this string, start in the upper left corner of the matrix and go down the columns.

The letter 'A' (*Figure 9*) would have a binary string shown in *Figure 8.* The data must be padded to make it an even 5 bytes in length. The pad at the beginning of the data (0001) is used as the leading 1 for the MM58348. The one bit pad at the end of the binary string must be a 0. If a 1 were sent as the pad, it would be used as the start bit for the next character.

The 5 byte data word that would be stored in ROM and represent the letter 'A' would then be 13EA24283E.

STORING THE DATA IN ROM

The 5 bytes of data are stored in 5 different locations in ROM. The first byte of data will be stored, LSB first, at location 200H plus the ASCII value of the character. For example, the ASCII value of the letter 'A' is 41H. The first byte of data for the letter 'A' would be stored, least significant bit first, at 241H. The second byte of data is stored at the location of the first data byte plus 60H or in this case at 2A1H. The location of the third byte is 40H plus the location of the second byte. In this case, the third byte of data would be stored at 2E1H. The fourth byte of data is stored at 300H plus the ASCII value of the character or at 341H for the letter 'A'. The final byte of data is stored 40H from the fourth byte or at 381H. Remember the LSB of each byte is stored first. Table I shows the locations in ROM and the values stored in them for the letter 'A'.

This application shows a VF display controller designed with a minimum number of IC's. If additional information about VF displays or VF display drivers is required, refer to Application Note AN-371 (The MM58348/342/341/248/242/241 direct drive Vacuum Fluorescent (VF) Displays.

TABLE I. Character Data of 'A' and Its Locations in ROM

Address In ROM	Data Stored
0241H	31
02A1H	AE
02E1H	42
0341H	82
0381H	E3

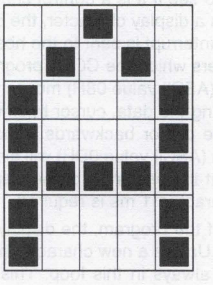


FIGURE 9. 5 x 7 Character as Stored in ROM

Section 1 of COPS Software

```
        .CHIP 424C          ;DEFINES COPS CHIP
;THIS SECTION INITIALIZES THE RAM IN THE COPS BY LOADING A
;2 IN THE MSB AND A 0 IN THE LSB LOCATIONS OF EACH CHARACTER.
;IT ALSO STOPS THE CLOCK AND SETS THE POINTER AT THE FIRST
;CHARACTER OF THE DISPLAY.

RESET:          CLRA
                LBI 3,15        ;LOADS A 2 IN ALL
                JSR CLEAR2      ;MSB LOCATIONS
                LBI 2,15        ;LOADS A 2 IN ALL
                JSR CLEAR2      ;MSB LOCATIONS
                LBI 1,15        ;LOADS A 0 IN ALL
                JSR CLEAR       ;LSB LOCATIONS
                LBI 0,15        ;LOADS A 0 IN ALL
                JSR CLEAR       ;LSB LOCATIONS

                CLRA            ;LOADS POINTER IN RAM
                XAD 1,15        ;MSB IN 1,0F
                CLRA
                AISC 15         ;LSB IN 1,0E
                XAD 1,14

                RC              ;RESETS CARRY TO
                XAS             ;   STOP CLOCK
                JMP START

CLEAR:          CLRA            ;CLEARS REGISTORS
                XDS 0
                JMP CLEAR
                RET

CLEAR2:         CLRA            ;PUTS A 2 IN REGISTORS
                AISC 02
                XDS 0
                JMP CLEAR2
                RET
```

Section 2 of COPS Software

```
;THIS SECTION OF CODE IS ONLY EXECUTED WHEN A NEW
;CHARACTER HAS BEEN ENTERED. IF THE CHARACTER IS
;A CONTROL CHARACTER, THE CURSOR IS MOVED ACCORDINGLY,
;OTHERWISE THE CHARACTER IS STORED IN THE RAM OF THE COPS.

        ;NEW CHARACTER HAS BEEN ENTERED
NEW:           LBI 1,0C        ;DUMMY POINTER
               INL             ;READS ASCII FROM
               XIS  0          ;DATA BUS
               X 0
               LDD 1,0D
               RC              ;CHAR.  MSB=0 THEN YES
               AISC 15         ;MSB<>0 THEN NO
               JMP SPECIAL
               AISC 01
               LDD 1,0E        ;STORE ASCII IN RAM
               CAB
               LDD 1,0F
               XABR
               LDD 1,0C        ;MSB IN 1,0C
               X 2
               LDD 1,0D        ;LSB IN 1, OD
               X 0
```

Section 2 of COPS Software (Continued)

```
                JSR CURFOR
                LBI 0,01        ;SENDS INTERRUPT TO
                OBD             ;  HOST.  CHAR. IS
                LBI 0,0         ;  STORED IN RAM
                OBD
                JMP START

          ;SPECIAL CHARS. (CR, LF, CLEAR DISPLAY)

CURFOR:         LDD 1,0E        ;MOVES CURSOR FORWARD ONE
                COMP            ;SPACE.  IF CURSOR IS
                AISC 01         ;MOVED BEYOND THE END OF
                JMP OK          ;DISPLAY, IT WRAPS AROUND
                AISC 0F         ;TO THE OTHER END.  DATA IS
                XAD 1,0E        ;NOT DESTROYED BY MOVING
                CLRA            ;CURSOR
                AISC 01
                LBI 1,0F
                XOR
                JMP SKIP
OK:             COMP
SKIP:           LBI 1,0E
                X 0
                RET
CURBAC:         LDD 1,0F        ;MOVES CURSOR BACK ONE
                AISC 01         ;CHARACTER.  DOES NOT
                JMP GOOD        ;DESTROY DATA AS IT IS MOVED
                LBI 1,0E        ;IF MOVED BEYOND THE
                CLRA            ;END OF THE DISPLAY IT
                AISC 01         ;WRAPS AROUND TO THE OTHER
                XOR             ;END
                X 0
                JMP START
GOOD:           XAD 1,0F
                JMP START

SPECIAL:        LDD 1,0C        ;CONTROL CHAR. HAS BEEN
                AISC 03         ;DETECTED
                JMP NOTRET
                JMP RESET       ;RETURN CLEARS DISPLAY,STARTS
                                ;PROGRAM OVER
NOTRET:         AISC 01         ;NOT RETURN, CHECK FOR CURSOR
                JMP CFOR        ;FORWARD
                JMP CURBAC      ;BY DEFAULT, CURSOR BACKWARDS

CFOR:           JSR CURFOR
                JMP START

          ;DISPLAY LOOP
```

Section 3 of COPS Software

```
;THIS IS THE DISPLAY LOOP OF THE PROGRAM. UNLESS A NEW CHARACTER
;HAS BEEN ENTERED AND IS BEING STORED, THE PROGRAM IS ALWAYS IN
;THIS DISPLAY LOOP. IT LOOKS UP THE CHARACTER FONT, SHIFTS THE
;CHARACTER DATA OUT THE SERIAL PORT AND CONTROLS THE GRID DRIVER.

START:          LBI 2,15        ;DISPLAY LOOP POINTER
                JSR HERE        ;GOTO DISPLAY LOOP
                LBI 3,03        ;SECOND DISPLAY LOOP POINTER
                JSR HERE        ;GOTO DISPLAY LOOP
                OGI 09          ;LOADS A 1 IN GRID DRIVER
                OGI OD
                OGI 09

                JMP START

          ;CHECKS FOR NEW CHAR

HERE:           RC
                ININ
                AISC 15
                JMP OLDCHR
                JMP NEW

          ;DISPLAY LOOP FOR OLD CHAR AND
          ;  LOOK UP

OLDCHR:         LD 2            ;LOOKS UP FIRST BYTE OF CHR.FONT
                JSR DATA4       ;    200H+ASCII VALUE
                AISC 06         ;ADDS 06H TO MSB OF ASCII
                JSR DATA2       ;LOOKS UP SECOND BYTE OF CHR FONT
                AISC 0A         ;ADDS 0AH TO MSB OF ASCII
                JSR DATA2       ;LOOKS UP THIRD BYTE OF CHR. FONT
                JSR DATA3       ;LOOKS UP THIRD BYTE OF CHR. FONT
                                ;    AT 300H+ASCII VALUE
                AISC 06         ;ADDS 06H TO MSB OF ASCII VALUE
                OGI 02          ;TURNS ON BLANKING CONTROL
                JSR DATA3       ;LOOKS UP LAST BYTE OF CHR. FONT
          ;CLOCKS A 0 IN GRID DRIVER

                OGI 0A          ;ENABLE,BLANKING CONTROL
                OGI 0E          ;ENABLE,BLANKING CONTROL,CLOCK
                OGI 0A          ;ENABLE,BLANKING CONTROL
                OGI 00          ;A 0 SHIFTED IN

                LD 0
                XDS 2
                JMP HERE
                RET

RIGHT:          LBI 3,15
                CQMA
                JSR SHIFT       ;OUTPUTS A
                X 0             ;NEW DATA
                JSR SHIFT       ;OUTPUTS A
                LEI 01          ;COUNTER MODE
                LDD 3,14        ;1,0 IN A
                XABR            ;A IN BR
                LDD 3,13        ;1,1 IN A
                CAB             ;A IN BD
                LD 2
                RET
```

Section 3 of COPS Software (Continued)

```
POINTER:        LEI 01          ;COUNTER MODE
                XAS             ;A IN SIO
                XABR            ;BR IN A
                AISC 02         ;ADD 2
                XAD 3,14        ;A IN 1,0
                CBA             ;BD IN A
                XAD 3,13        ;A IN 1,1
                LBI 3,15
                XAS             ;SIO IN A
                LEI 08          ;SERIAL MODE
                JMP RIGHT
          ;SHIFTS OUT SERIAL PORT

SHIFT:          LEI 08          ;THIS ROUTINE SHIFTS THE DATA
                SC              ;FROM THE SI/O REGISTER OUT
                XAS             ;THE SERIAL PORT WITH EACH
                NOP             ;CLOCK CYCLE
                NOP
                RC
                XAS
                RET

          .=0200
DATA3:          LQID
                JMP RIGHT
DATA4:          LQID
                JMP POINTER

          .=0300
DATA3:          LQID
                JMP RIGHT
```

Section 4 of COPS Software

```
;THE CHARACTER FONTS FOR THE CHARACTERS WITH ASCII VALUES BETWEEN
20H AND 5AH HAVE BEEN STORED IN THIS SECTION OF THE PROGRAM.

          ;DATA FOR FIRST 2 BYTES OF EACH
          ;     CHAR.

          .=0220
      .WORD 001, 001, 001, 021, 021, 0C1, 061, 001
      .WORD 031, 001, 041, 011, 001, 011, 001, 001
      .WORD 071, 001, 041, 081, 011, 0E1, 031, 081
      .WORD 061, 061, 001, 001, 001, 021, 001, 041
      .WORD 071, 031, 081, 071, 081, 0F1, 0F1, 071
      .WORD 0F1, 081, 081, 0F1, 0F1, 0F1, 0F1, 071
      .WORD 0F1, 071, 0F1, 061, 081, 0F1, 0F1, 0F1
      .WORD 0C1, 0C1, 081
      ;DATA FOR SECOND 2 BYTES OF EACH
      ;    CHAR.

      .=0280
.WORD 000, 000, 0C1, 0F9, 0A4, 095, 02D, 000
.WORD 088, 000, 054, 020, 000, 020, 000, 014
.WORD 01D, 082, 003, 005, 058, 045, 0AC, 001
.WORD 02D, 023, 000, 000, 020, 058, 001, 001
.WORD 00D, 0AE, 0F3, 00D, 0F3, 02F, 02F, 00D
.WORD 02E, 003, 00D, 02E, 00E, 08E, 08E, 00D
.WORD 02F, 00D, 02F, 025, 001, 00C, 008, 00C
.WORD 056, 040, 017

      ;THIRD 2 BYTES OF DATA FOR EACH CHAR.


      .=02C0
.WORD 000, 0E3, 000, 0AC, 0FB, 040, 0A5, 083
.WORD 00A, 002, 0F3, 0F1, 034, 040, 008, 040
.WORD 046, 0F7, 02E, 046, 021, 086, 046, 02E
.WORD 046, 046, 0A0, 0B4, 0A0, 0A0, 015, 022
.WORD 0E6, 042, 04E, 006, 00E, 046, 042, 046
.WORD 040, 0F7, 006, 0A0, 004, 080, 0E0, 006
.WORD 042, 026, 062, 046, 0F3, 004, 008, 034
.WORD 040, 070, 046

      ;FOURTH TWO BYTES OF DATA FOR EACH CHAR.


      .=0320
.WORD 000, 008, 007, 0F7, 0AA, 031, 028, 000
.WORD 008, 02A, 049, 080, 000, 080, 000, 001
.WORD 01D, 018, 09C, 09D, 0F7, 01D, 09C, 084
.WORD 09C, 0AC, 000, 000, 022, 041, 041, 08C
.WORD 0DC, 082, 09C, 01C, 01C, 09C, 084, 09C
.WORD 080, 01C, 0EF, 022, 018, 002, 020, 01C
.WORD 084, 02C, 0A4, 09C, 00C, 018, 028, 010
.WORD 041, 009, 01D

      ;LAST BYTES OF DATA FOR EACH CHAR.


      .=0380
.WORD 000, 000, 000, 082, 084, 064, 0A0, 000
.WORD 000, 083, 044, 001, 000, 001, 000, 004
.WORD 0C7, 020, 026, 0CC, 080, 0C9, 0C8, 00E
.WORD 0C6, 087, 000, 000, 028, 082, 001, 006
.WORD 027, 0E3, 0C6, 044, 0C7, 028, 008, 0C5
.WORD 0EF, 028, 008, 028, 020, 0EF, 0EF, 0C7
.WORD 006, 0A7, 026, 0C4, 008, 0CF, 08F, 0CF
.WORD 06C, 00C, 02C


.END
```

Section 5
Memory Support

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National Semiconductor

Memory Support

MOS memory devices today can be found in a variety of configurations, giving design engineers more flexibility than ever before. National Semiconductor offers a variety of key devices that will allow a user to easily implement memory designs which meet his or her particular requirements.

National's memory support circuits include clock drivers, 4k and 16k RAM address drivers, data I/O circuits, and timing and control drivers. Further information on the specific device types may be found in application note AN-76, "Applying Modern Clock Drivers to MOS Memories".

In addition to memory support applications, this family of products provides the versatility of general use in typical applications including level translation of TTL/CMOS input levels to high voltage (24V) outputs with high capacitive (1000 pF) drive, power drivers, relay driver and sense amplifier. Detailed features/function of this series of drivers are highlighted in the following product guide.

National
Semiconductor

Memory Support Circuits

Temperature Range		Driver/ Package	TRI-STATE®/ Strobed	Output High Voltage (V)	Propagation Delay Typ. (ns)	Capacitive Load (PS)	Supply Current (mA)	Page No.
0°C to +70°C	−55°C to +125°C							
DP84240		8	TRI-STATE	5.5	20	500	125	5-5
DP84244		8	TRI-STATE	5.5	20	500	150	5-5
DS0025C		2		20	25	1000		5-10
DS0026C	DS0026	2		20	7.5	1000	80	5-14
DS0056C	DS0056	2		20	7.5	1000	80	5-14
DS3245		4	STROBED	12	11	200	30	5-22
DS3628	DS1628	8	TRI-STATE	5.5	6.5	500	120	5-25
DS3647A		4	TRI-STATE	5.5	8	50	140	5-28
DS3648	DS1648	4	TRI-STATE	5.5	9	500	60	5-34
DS3678	DS1678	4	TRI-STATE	5.5	9	500	60	5-34
DS3649	DS1649	6	TRI-STATE	5.5	8	500	75	5-39
DS3679	DS1679	6	TRI-STATE	5.5	8	500	75	5-39
DS3651	DS1651	4	STROBED	5.5	23	50	60	5-43
DS3674	DS1674	4	STROBED	12	13	400	40	5-49
DS36149	DS16149	6	STROBED	5.5	13	500	60	5-54
DS36179	DS16179	6	STROBED	5.5	13	500	60	5-54
DS75325	DS55325	4		24	25	25	70	5-58
DS75361		2	STROBED	24	11	390	24	5-71
DS75365		4	STROBED	24	31	200	47	5-76
DS9643/ μA9643		2	STROBED	12	9	300	19	5-81

National Semiconductor

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

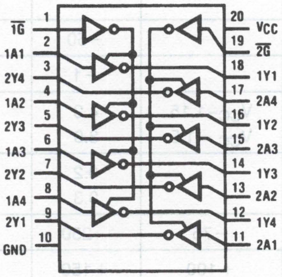
General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

Features

- t_{pd} specified with 250 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

Connection Diagram

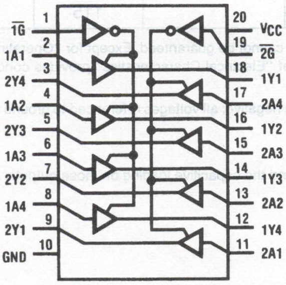


1
$\overline{1G}$
2
1A1
3
2Y4
4
1A2
5
2Y3
6
1A3
7
2Y2
8
1A4
9
2Y1
10
GND
20
VCC
19
$\overline{2G}$
18
1Y1
17
2A4
16
1Y2
15
2A3
14
1Y3
13
2A2
12
1Y4
11
2A1

TL/F/5219–1

Top View

Order Number DP84240J or DP84240N
See NS Package Numbers J20A or N20A



1
$\overline{1G}$
2
1A1
3
2Y4
4
1A2
5
2Y3
6
1A3
7
2Y2
8
1A4
9
2Y1
10
GND
20
VCC
19
$\overline{2G}$
18
1Y1
17
2A4
16
1Y2
15
2A3
14
1Y3
13
2A2
12
1Y4
11
2A1

TL/F/5219–2

Top View

Order Number DP84244J or DP84244N
See NS Package Numbers J20A or N20A

Truth Table

DP84240

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1150 mW
Molded Package	1300 mW
Lead Temperature (soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $0 \le T_A \le 70°C$. (Notes 2 and 3.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 2.7V$		0.1	20	μA
		$V_{IN} = 7.0V$			100	μA
$I_{IN(0)}$	Logical "0" Input Current	$0 \le V_{IN} \le 0.4V$		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -18$ mA		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -100$ μA $I_{OH} = -1$ mA	$V_{CC}-1.15$ $V_{CC}-1.5$	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 10$ μA $I_{OL} = 12$ mA		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	$V_{OUT} = 1.5V$	−75	−250		mA
I_{0D}	Logical "0" Drive Current	$V_{OUT} = 1.5V$	+100	+150		mA
Hi-Z	TRI-STATE Output Current	$0.4V \le V_{OUT} \le 2.7V$	−100		+100	μA
I_{CC}	Supply Current	All Outputs Open				mA
	DP84240	All Outputs High All Outputs Low All Outputs Hi-Z		16 74 80	50 125 125	
	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Characteristics

V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	*Figures 1* & *3*	CL = 250 pF C_L = 500 pF	9 10	16 20	27 33	ns
t_{PHL}	Propagation Delay from HIGH-to-LOW Output		C_L = 250 pF C_L = 500 pF	9 12	16 20	25 31	ns
t_{PLZ}	Output Disable Time from LOW	*Figures 2* & *4,* S = 1, C_L = 50 pF			11	24	ns
t_{PHZ}	Output Disable Time from HIGH	*Figures 2* & *4,* S = 2, C_L = 50 pF			12	24	ns
t_{PZL}	Output Enable Time to LOW	*Figures 2* & *4,* S = 1, C_L = 500 pF			30	45	ns
t_{PZH}	Output Enable Time to HIGH	*Figures 2* & *4,* S = 2, C_L = 500 pF			23	35	ns
t_{SKEW}	Output-to-Output Skew (Note 4)	*Figures 1* & *3,* C_L = 500 pF			3		ns

Capacitance

T_A = 25°C, f = 1 MHz, V_{CC} = 5V ±10%. (Note 3.)

Parameter	Conditions	Typ	Units
C_{IN}	All Other Inputs Tied Low	6	pF
C_{OUT}	Output in TRI-STATE Mode	20	pF

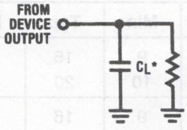
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

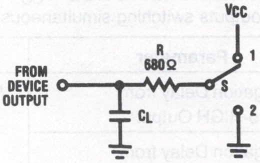
Switching Test Circuits


FROM DEVICE OUTPUT
CL*
R 2kΩ

TL/F/5219-3

*C_L INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching

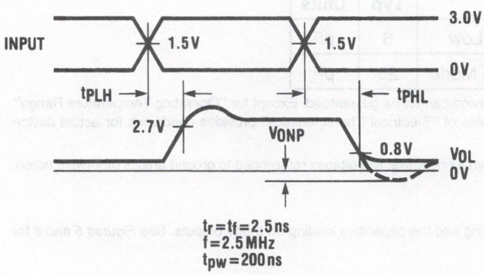

VCC
R 680Ω
1
FROM DEVICE OUTPUT
S
CL
2

TL/F/5219-4

FIGURE 2. TRI-STATE Enable/Disable

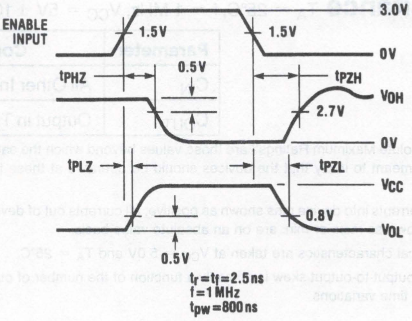
Typical Switching Characteristics

Voltage Waveforms


INPUT
1.5V
1.5V
3.0V
0V
tPLH
tPHL
2.7V
VONP
0.8V
VOL
0V
tr = tf = 2.5 ns
f = 2.5 MHz
tpw = 200 ns

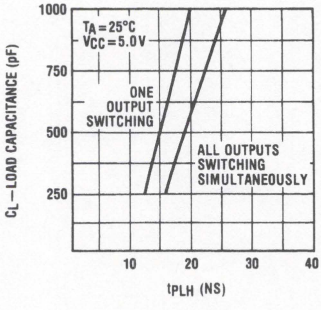
TL/F/5219-5

FIGURE 3. Output Drive Levels


ENABLE INPUT
1.5V
1.5V
3.0V
0V
tPHZ
0.5V
tPZH
VOH
2.7V
0V
tPLZ
tPZL
VCC
0.8V
VOL
0.5V
tr = tf = 2.5 ns
f = 1 MHz
tpw = 800 ns

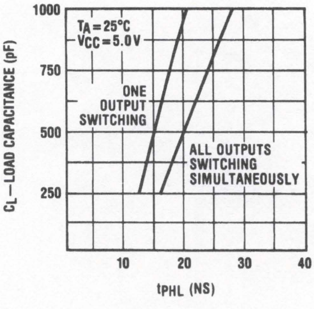
TL/F/5219-6

FIGURE 4. TRI-STATE Control Levels



TL/F/5219-7

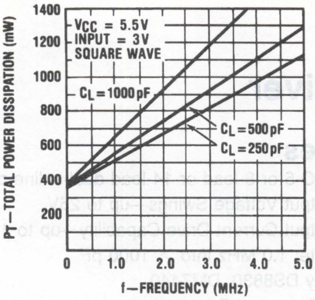
FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L



TL/F/5219-8

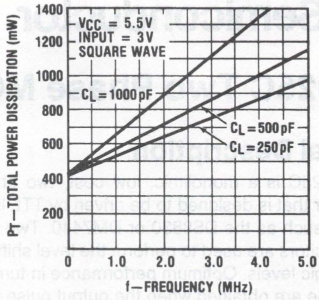
FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

Typical Switching Characteristics (Continued)



TL/F/5219-9

FIGURE 7. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

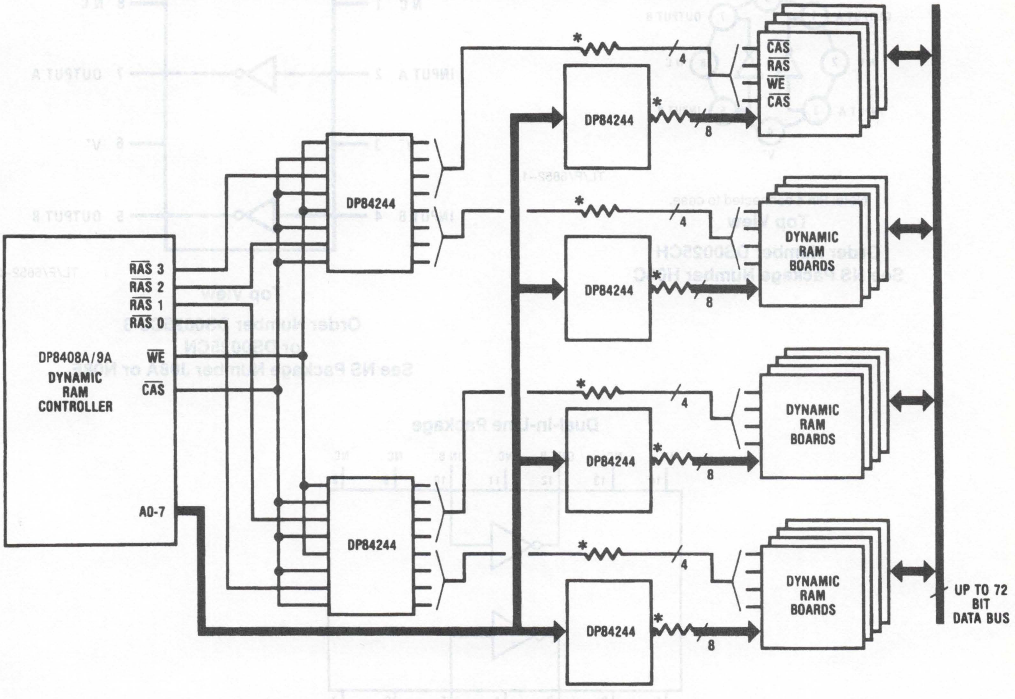


TL/F/5219-10

FIGURE 8. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)


DP8408A/9A
DYNAMIC
RAM
CONTROLLER
RAS 3
RAS 2
RAS 1
RAS 0
WE
CAS
A0-7
DP84244
DP84244
DP84244
DP84244
DP84244
DP84244
*
4
8
CAS
RAS
WE
CAS
DYNAMIC
RAM
BOARDS
DYNAMIC
RAM
BOARDS
DYNAMIC
RAM
BOARDS
UP TO 72
BIT
DATA BUS

TL/F/5219-11

National Semiconductor

PRELIMINARY

DS0025C Two Phase MOS Clock Driver

General Description

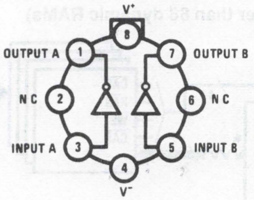
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse width may be set by selection of the input capacitor eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 25V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package


V⁺
8
OUTPUT A
1
7
OUTPUT B
NC
2
6
NC
INPUT A
3
5
INPUT B
4
V⁻

TL/F/5852-1

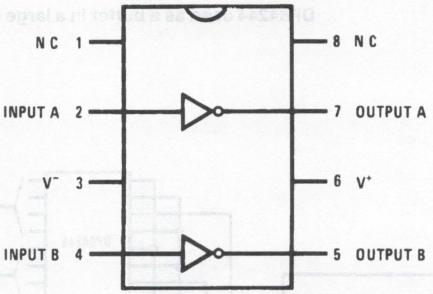
Note: Pin 4 connected to case.

Top View

Order Number DS0025CH

See NS Package Number H08C

Dual-In-Line Package


NC 1
INPUT A 2
V⁻ 3
INPUT B 4
8 NC
7 OUTPUT A
6 V⁺
5 OUTPUT B

TL/F/5852-2

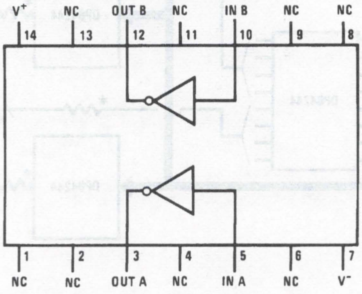
Top View

Order Number DS0025CJ-8

or DS0025CN

See NS Package Number J08A or N08E

Dual-In-Line Package


V⁺ 14
NC 13
OUT B 12
NC 11
IN B 10
NC 9
NC 8
1 NC
2 NC
3 OUT A
4 NC
5 IN A
6 NC
7 V⁻

TL/F/5852-3

Top View

Order Number DS0025CJ

See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

$(V^+ - V^-)$Voltage Differential	25V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Recommended Operating Conditions

	Min	Max
V^+ V^- Differential Voltage		20V
Temperature	0	70
Maximum Power Dissipation* at 25°C		
8-Pin Cavity Package		1150 mW
14-Pin Cavity Package		1410 mW
Molded Package		1080 mW
Metal Can (TO-5) Package		670 mW

* Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) See test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{d\ ON}$	Turn-On Delay Time	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$			15	30	ns
t_{RISE}	Rise Time	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$			25	50	ns
$t_{d\ OFF}$	Turn-Off Delay Time	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ (Note 4)			30	60	ns
t_{FALL}	Fall Time	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$	(Note 4)	60	90	120	ns
			(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$, $C_L = 0.001\ \mu F$ (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	$V_{IN} = 0V$, $I_{OUT} = -1$ mA		$V^+ - 1.0$	$V^+ - 0.7V$		V
V_{O-}	Negative Output Voltage Swing	$I_{IN} = 10$ mA, $I_{OUT} = 1$ mA			$V^- + 0.7V$	$V^- + 1.5V$	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

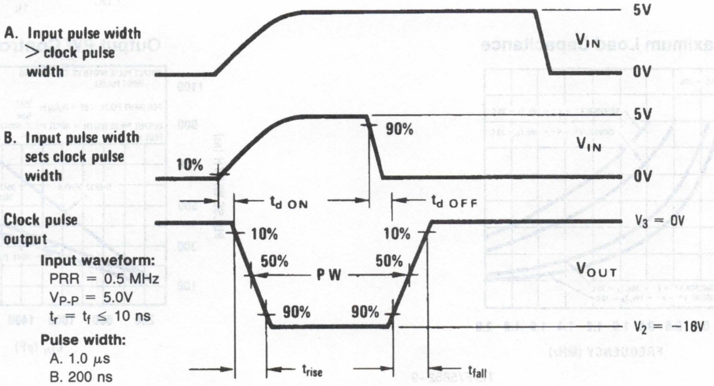
Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DS0025C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

Note 5: Parameter values for input width greater than output clock pulse width.

Timing Diagram

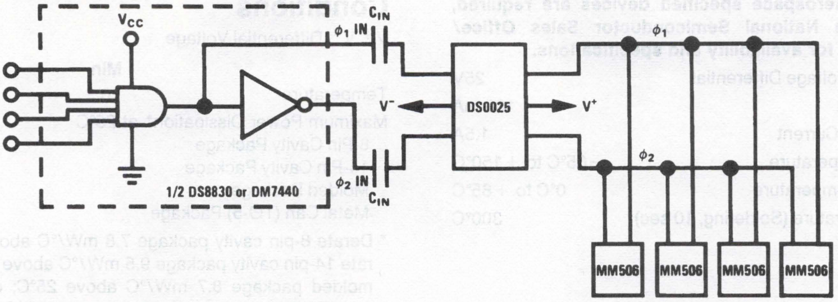


Input waveform:
PRR = 0.5 MHz
$V_{P-P} = 5.0V$
$t_r = t_f \leq 10$ ns

Pulse width:
A. 1.0 μs
B. 200 ns

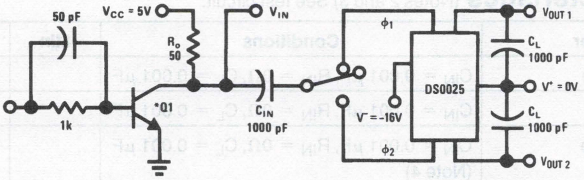
TL/F/5852-5

Typical Application


VCC
C_IN
ϕ1 IN
ϕ2 IN
C_IN
1/2 DS8830 or DM7440
V⁻
DS0025
V⁺
ϕ1
ϕ2
MM506
MM506
MM506
MM506

TL/F/5852-4

AC Test Circuit

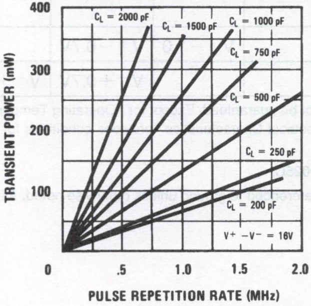

50 pF
VCC = 5V
R₀
50
V_IN
1k
*Q1
C_IN
1000 pF
ϕ1
ϕ2
V⁻ = -16V
DS0025
V_OUT 1
C_L
1000 pF
V⁺ = 0V
C_L
1000 pF
V_OUT 2

TL/F/5852-6

*Q1 is selected high speed NPN switching transistor.

Typical Performance

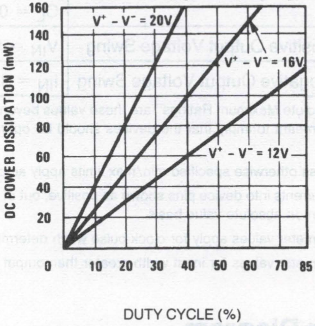
Transient Power vs Rep. Rate



TL/F/5852-7

$$P_{AC} = (V^+ - V^-)^2 f C_L$$

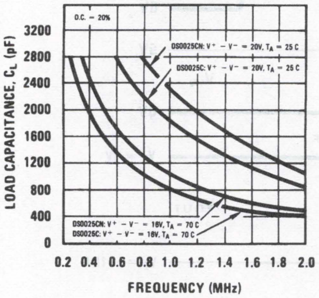
DC Power (P_{DC}) vs Duty Cycle



TL/F/5852-8

$$P_{DC} = \frac{V^+ - V^-)^2\,(DC)}{1k}$$

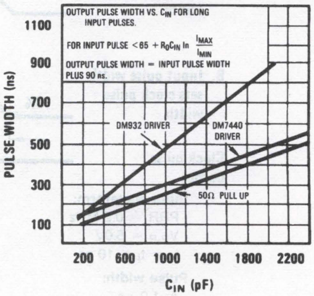
Maximum Load Capacitance



TL/F/5852-9

$$C_L < \frac{(P_{MAX})\,(1k) - (V^+ - V^-)^2\,(DC)}{(f)\,(1k)\,(V^+ - V^-)^2} < \frac{(I_{pk})\,(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



TL/F/5852-10

I_{MAX} = Peak Current delivered by driver

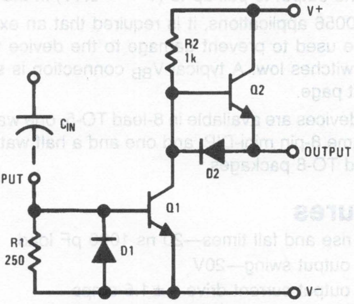
$$I_{MIN} \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE(sat)} + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.



TL/F/5852-11

FIGURE 1. DS0025 Schematic (One-Half Circuit)

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L\,(V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns. For $V^+ - V^- = 20V$, $I = 0.8A$.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, $f = 1.0$ MHz, $C_L = 1000$ pF, $P_{AC} = 400$ mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

$$= 80 \text{ mW for } V^+ - V^- = 20V,\ DC = 20\%$$

Package Power Dissipation

Total average power = transient output power + internal power.

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30–50 ns and 16V amplitude over the temperature range 0°–70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power.

385 mW = transient output power.

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

For further information please refer to National Semiconductors Application Note AN-76.

National Semiconductor

DS0026/DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

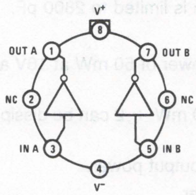
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

TO-5 Package

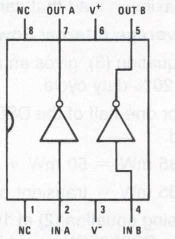

V+
8
OUT A 1
7 OUT B
NC 2
6 NC
IN A 3
5 IN B
4
V−

TL/F/5853-1

Note: Pin 4 connected to case.

Order Number
DS0026H or DS0026CH
See NS Package
Number H08C

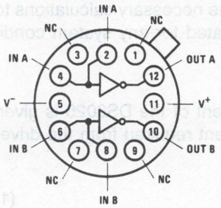
Dual-In-Line Package


NC
OUT A
V+
OUT B
8
7
6
5
1
2
3
4
NC
IN A
V−
IN B

TL/F/5853-2

Order Number DS0026CJ-8,
or DS0026CN
See NS Package Number
J08A or N08E

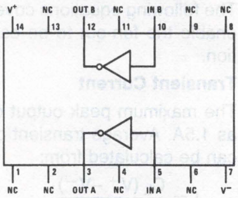
TO-8 Package


IN A
NC
NC
IN A
3
2
1
OUT A
4
12
V−
11
V+
6
10
IN B
7
8
9
OUT B
NC
NC
IN B

TL/F/5853-3

Order Number
DS0026G or DS0026CG
See NS Package
Number G12C

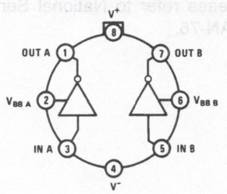
Dual-In-Line Package


V+
NC
OUT B
NC
IN B
NC
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OUT A
NC
IN A
NC
V−

TL/F/5853-4

Order Number
DS0026J or DS0026CJ
See NS Package
Number J14A

TO-5 Package

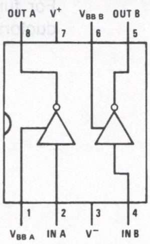

V+
8
OUT A 1
7 OUT B
$V_{BB\,A}$ 2
6 $V_{BB\,B}$
IN A 3
5 IN B
4
V−

TL/F/5853-5

Note: Pin 4 connected to case.

Order Number
DS0056H or DS0056CH
See NS Package
Number H08C

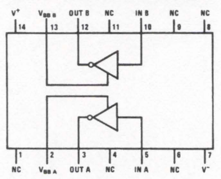
Dual-In-Line Package


OUT A
V+
$V_{BB\,B}$
OUT B
8
7
6
5
1
2
3
4
$V_{BB\,A}$
IN A
V−
IN B

TL/F/5853-6

Order Number DS0056J-8,
DS0056CJ-8 or DS0056CN
See NS Package Number
J08A or N08E

Dual-In-Line Package


V+
$V_{BB\,B}$
OUT B
NC
IN B
NC
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
$V_{BB\,A}$
OUT A
NC
IN A
NC
V−

TL/F/5853-7

Order Number DS0056J
or DS0056CJ
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
Metal Can (TO-5)	660 mW
Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_{OL} = 1$ mA			$V^- + 0.7$	$V^- + 1.0$	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{SS} \geq V^+ + 1.0V$ $I_{OH} = -1$ mA	DS0026	$V^+ - 1.0$	$V^+ - 0.8$		V
			DS0056	$V^+ - 0.3$	$V^+ - 0.1$		V
$I_{CC(ON)}$	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$	DS0026		30	40	mA
	(one side on)	(Note 6)	DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$,	70°C		10	100	μA
		$V_{IN} - V^- = 0V$	125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-Off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		15	18	ns
			$C_L = 1000$ pF		20	35	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		12	16	ns
			$C_L = 1000$ pF		17	25	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		28	35	ns
			$C_L = 1000$ pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

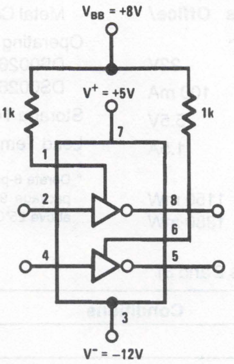
Note 4: All typical values for $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

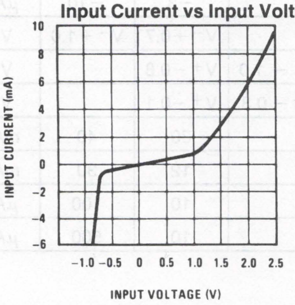
Typical V_{BB} Connection



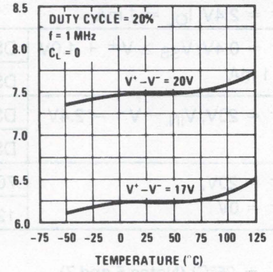
TL/F/5853-8

Typical Performance Characteristics

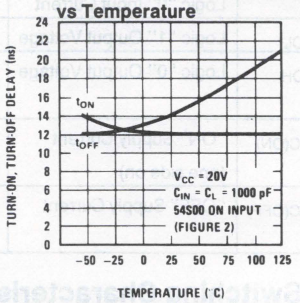
Input Current vs Input Voltage



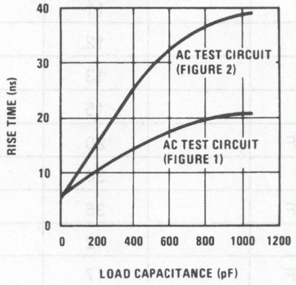
Supply Current vs Temperature



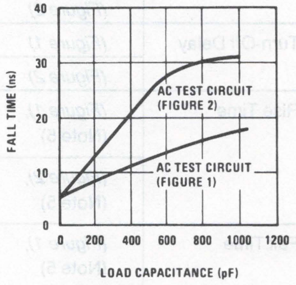
Turn-On and Turn-Off Delay vs Temperature



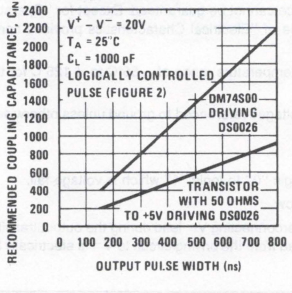
Rise Time vs Load Capacitance



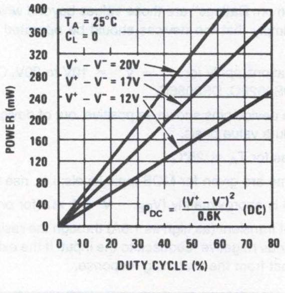
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



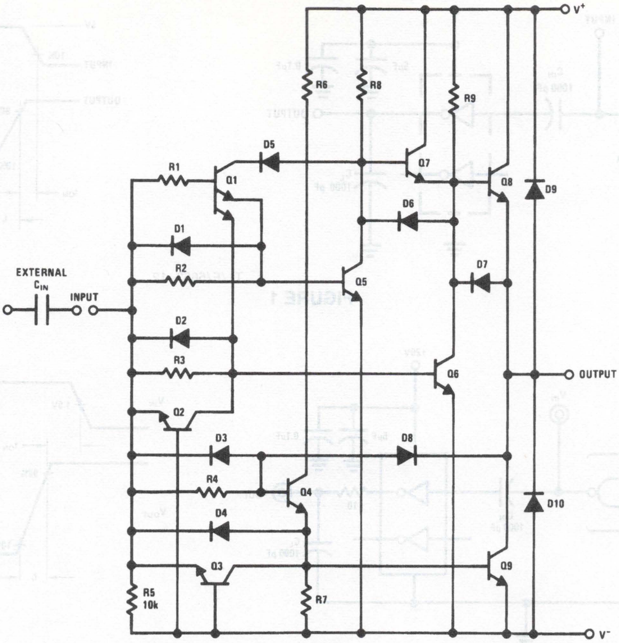
DC Power (P_{DC}) vs Duty Cycle



TL/F/5853-9

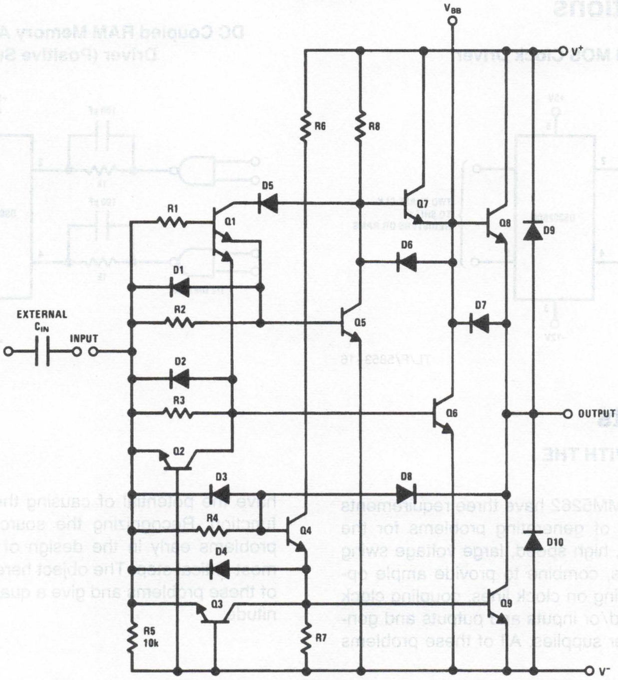
Schematic Diagrams

1/2 DS0026


V+
R6
R8
R9
D5
R1
Q1
Q7
Q8
D9
D6
D1
EXTERNAL
C_{IN}
INPUT
R2
Q5
D7
D2
R3
Q6
OUTPUT
Q2
D3
D8
R4
Q4
D10
D4
Q3
Q9
R5
10k
R7
V-

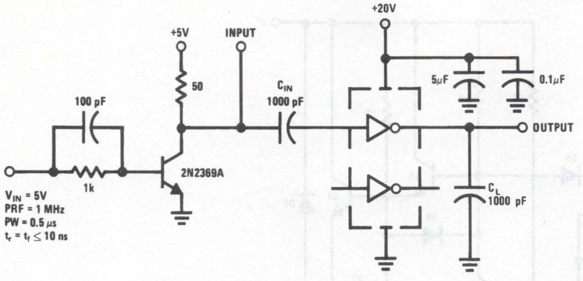
TL/F/5853-10

1/2 DS0056

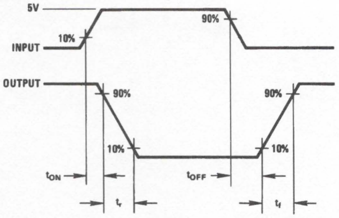

V_{BB}
V+
R6
R8
D5
R1
Q1
Q7
Q8
D9
D6
D1
EXTERNAL
C_{IN}
INPUT
R2
Q5
D7
D2
R3
Q6
OUTPUT
Q2
D3
D8
R4
Q4
D10
D4
Q3
Q9
R5
10k
R7
V-

TL/F/5853-11

AC Test Circuits and Switching Time Waveforms

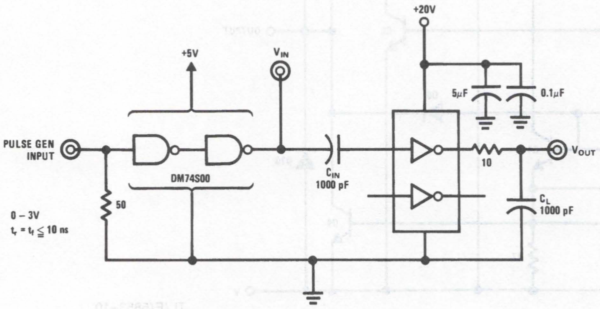

+20V
+5V
INPUT
50
100 pF
C_IN
1000 pF
5μF
0.1μF
OUTPUT
1k
2N2369A
C_L
1000 pF
V_IN = 5V
PRF = 1 MHz
PW = 0.5 μs
t_r = t_f ≤ 10 ns

TL/F/5853-12

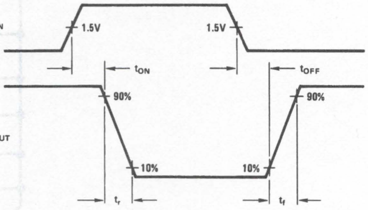

5V
INPUT
10%
90%
OUTPUT
90%
90%
10%
10%
t_ON
t_OFF
t_r
t_f

TL/F/5853-13

FIGURE 1


+20V
+5V
V_IN
5μF
0.1μF
PULSE GEN INPUT
DM74S00
C_IN
1000 pF
10
V_OUT
50
C_L
1000 pF
0 – 3V
t_r = t_f ≤ 10 ns

TL/F/5853-14

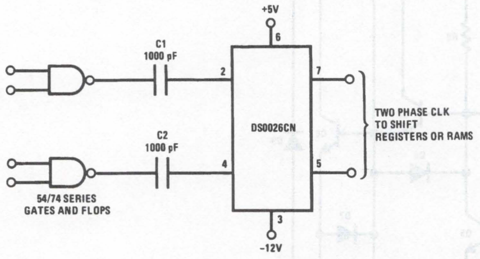

V_IN
1.5V
1.5V
t_ON
t_OFF
90%
90%
V_OUT
10%
10%
t_r
t_f

TL/F/5853-15

FIGURE 2

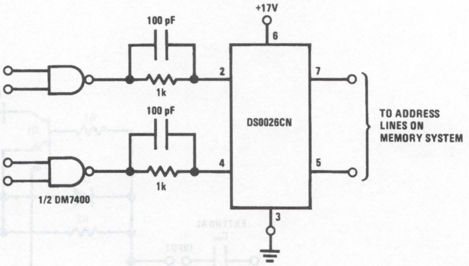
Typical Applications

AC Coupled MOS Clock Driver


+5V
6
C1
1000 pF
2
7
DS0026CN
TWO PHASE CLK TO SHIFT REGISTERS OR RAMS
C2
1000 pF
4
5
54/74 SERIES GATES AND FLOPS
3
-12V

TL/F/5853-16

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)


100 pF
+17V
6
2
7
1k
100 pF
DS0026CN
TO ADDRESS LINES ON MEMORY SYSTEM
4
5
1k
1/2 DM7400
3

TL/F/5853-17

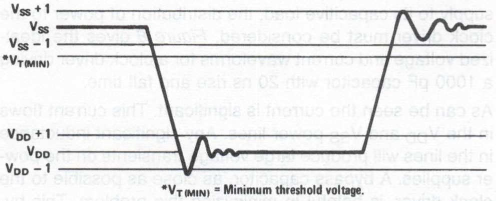
Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Application Hints (Continued)

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1\ V_{OH}$ is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to V_{SS} − 1V would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.



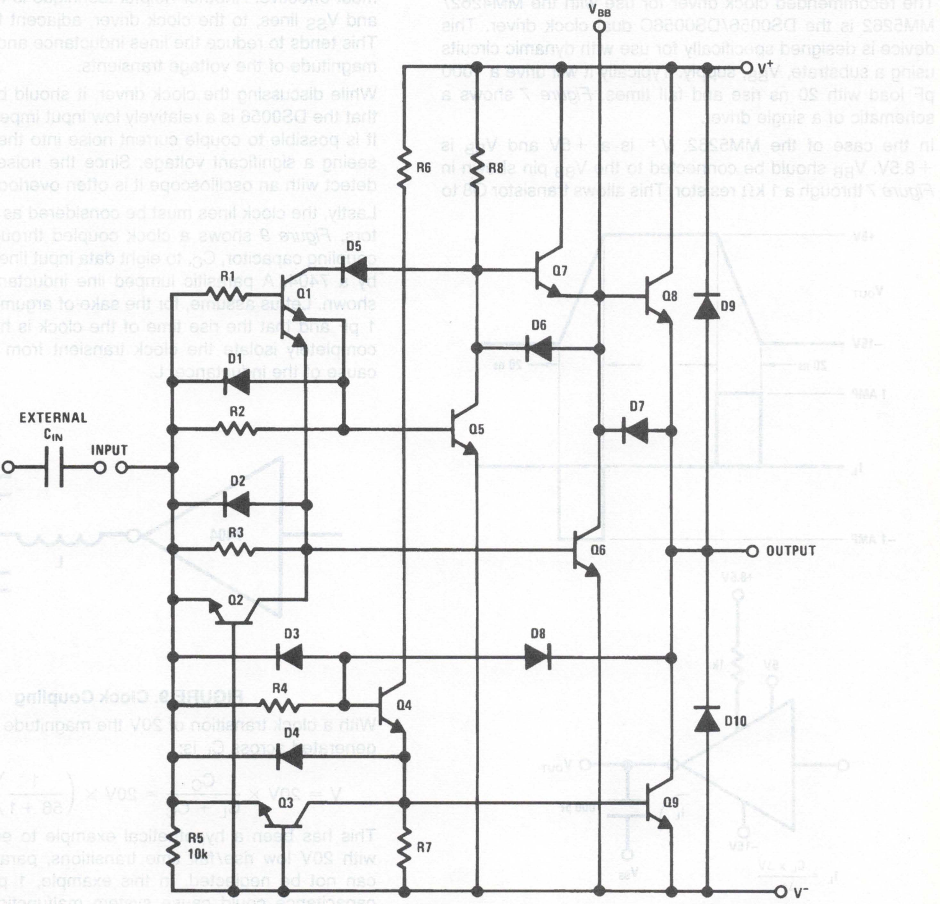
*$V_{T(MIN)}$ = Minimum threshold voltage.

TL/F/5853-18

FIGURE 6. Clock Waveform

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damp-



TL/F/5853-11

FIGURE 7. Schematic of 1/2 DS0056

Application Hints (Continued)

ing resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

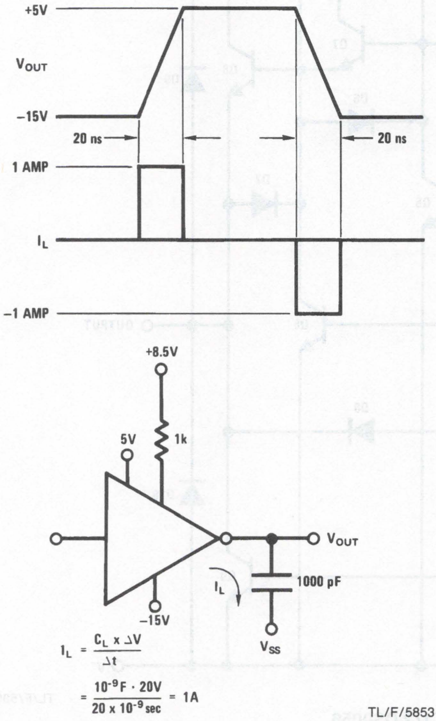
In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q8 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0V$ clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q8 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin on this line to zero.

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

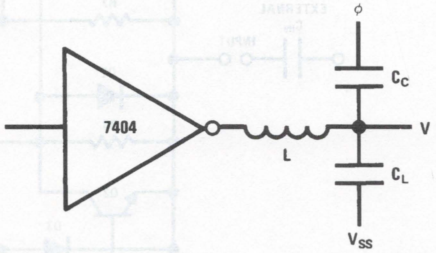
Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.



$$I_L = \frac{C_L \times \Delta V}{\Delta t} = \frac{10^{-9}F \cdot 20V}{20 \times 10^{-9}\text{sec}} = 1A$$

TL/F/5853-19

FIGURE 8. Clock Waveforms (Voltage and Current)



TL/F/5853-20

FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56 + 1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of

Application Hints (Continued)

noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1 \text{ mA}$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

National Semiconductor

DS3245 Quad MOS Clock Driver

General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

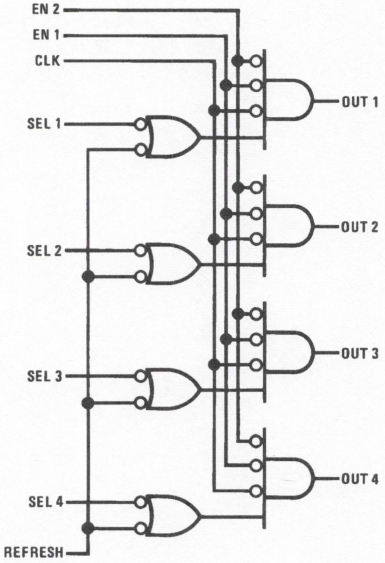
Only 2 supplies, 5 V_{DC} and 12 V_{DC}, are required without compromising the usual high V_{OH} specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

Features

- TTL compatible inputs
- Operates from 2 standard supplies: 5 V_{DC}, 12 V_{DC}
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

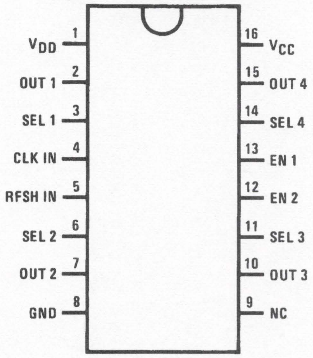
Logic and Connection Diagrams



EN 2
EN 1
CLK
SEL 1
OUT 1
SEL 2
OUT 2
SEL 3
OUT 3
SEL 4
OUT 4
REFRESH

TL/F/5873–1

Dual-In-Line Package



V_DD 1
OUT 1 2
SEL 1 3
CLK IN 4
RFSH IN 5
SEL 2 6
OUT 2 7
GND 8
16 V_CC
15 OUT 4
14 SEL 4
13 EN 1
12 EN 2
11 SEL 3
10 OUT 3
9 NC

TL/F/5873–2

Top View

Order Number DS3245J or DS3245N
See NS Package Number J16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5V to +7V
Supply Voltage, V_{DD}	−0.5V to +14V
All Input Voltages	−1.0V to V_{DD}
Outputs for Clock Driver	−1.0V to V_{DD} + 1V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Supply Voltage, V_{DD}	11.4	12.6	V
Operating Temperature 9T_A	0	75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{FD}	Select Input Load Current	$V_F = 0.45V$			−0.25	mA
I_{FE}	Enable Input Load Current	$V_F = 0.45V$			−1.0	mA
I_{RD}	Select Input Leakage Current	$V_R = 5V$			10	μA
I_{RE}	Enable Input Leakage Current	$V_R = 5V$			40	μA
V_{OL}	Output Low Voltage	$I_{OL} = 5$ mA, $V_{IH} = 2V$			0.45	V
		$I_{OL} = -5$ mA	1.0			
V_{OH}	Output High Voltage	$I_{OH} = -1$ mA, $V_{IL} = 0.8V$	$V_{DD} - 0.50$			V
		$I_{OH} = 5$ mA			$V_{DD} + 1.0$	V
V_{IL}	Input Low Voltage, All Inputs				0.8	V
V_{IH}	Input High Voltage, All Inputs		2			V
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, $I_{IN} = -12$ mA		−1.0	−1.5	V

Power Supply Current Drain

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Current from V_{CC} Output in High State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		26	34	mA
I_{DD}	Current from V_{DD} Output in High State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		23	30	mA
I_{CC}	Current from V_{CC} Output in Low State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		29	39	mA
I_{DD}	Current from V_{DD} Output in Low State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +°C range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$ and $V_{DD} = 12V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Switching Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Conditions	Min(1)	Typ(2,4)	Max(3)	Units
t_{-+}	Input to Output Delay	$R_{SERIES} = 0$	5	11		ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 0$		20	32	ns
t_{+-}	Input to Output Delay	$R_{SERIES} = 0$	3	7		ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\Omega$	10	17	25	ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 20\Omega$		27	38	ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 20\Omega$		25	38	ns

Capacitance $T_A = 25°C$(5)

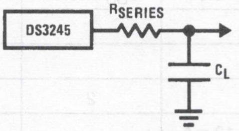
Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance, $\overline{I_1}$, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$			5	8	pF
C_{IN}	Input Capacitance, $\overline{R}$, $\overline{C}$, $\overline{E1}$, $\overline{E2}$			8	12	pF

Note 1: $C_L = 150$ pF
Note 2: $C_L = 200$ pF } These values represent a range of total stray plus clock capacitance for nine 4k RAMs.
Note 3: $C_L = 250$ pF

Note 4: Typical values are measured at 25°C.

Note 5: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

AC Test Circuit and Switching Time Waveforms

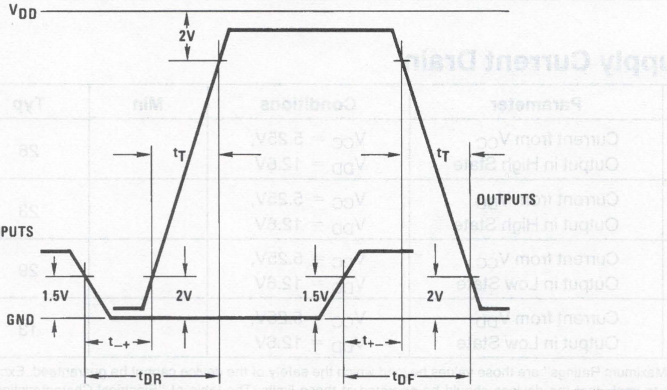


Input pulse amplitudes: 3V

Input pulse rise and fall times:
5 ns between 1V and 2V

Measurements points: see waveforms

TL/F/5873-3



TL/F/5873-4

National Semiconductor

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

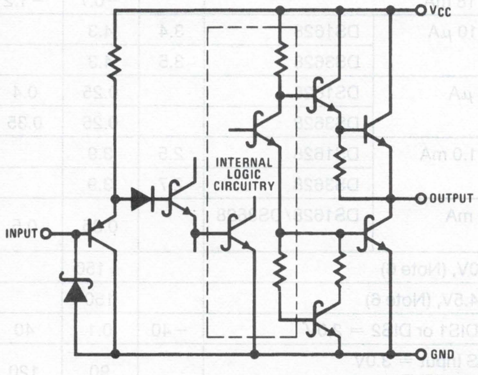
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

Features

- High speed capabilities
  - Typical 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4V min)
- High density
  - Eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams

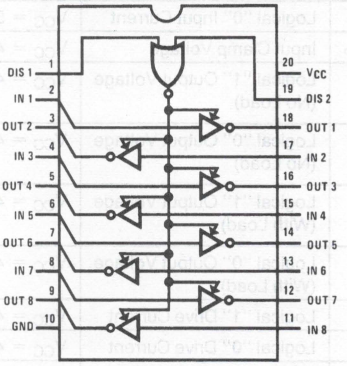


VCC
INTERNAL LOGIC CIRCUITRY
OUTPUT
INPUT
GND

TL/F/5875–1

(Equivalent Input/Output Circuit)

Dual-In-Line Package



DIS 1 1
IN 1 2
OUT 2 3
IN 3 4
OUT 4 5
IN 5 6
OUT 6 7
IN 7 8
OUT 8 9
GND 10
20 VCC
19 DIS 2
18 OUT 1
17 IN 2
16 OUT 3
15 IN 4
14 OUT 5
13 IN 6
12 OUT 7
11 IN 8

Top View

TL/F/5875–2

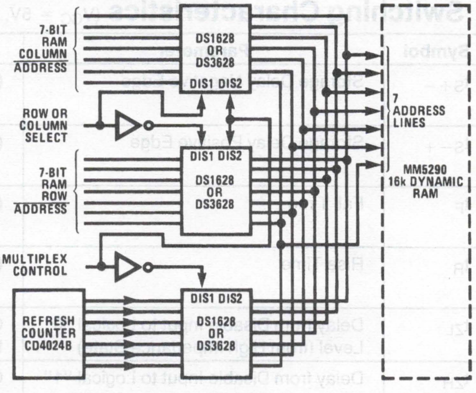
Order Number
DS1628J, DS3628J, DS3628N
See NS Package Number J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



7-BIT RAM COLUMN ADDRESS
DS1628 OR DS3628
DIS1 DIS2
ROW OR COLUMN SELECT
7-BIT RAM ROW ADDRESS
DIS1 DIS2
DS1628 OR DS3628
MULTIPLEX CONTROL
REFRESH COUNTER CD4024B
DIS1 DIS2
DS1628 OR DS3628
7 ADDRESS LINES
MM5290 16k DYNAMIC RAM

TL/F/5875–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5.5V$ $V_{IN} = 5.5V$			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5.5V$ $V_{IN} = 5.5V$			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_{IN} = -18$ mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	$V_{CC} = 4.5V$, $I_{OH} = -10$ μA	DS1628	3.4	4.3		V
			DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	$V_{CC} = 4.5V$, $I_{OL} = 10$ μA	DS1628		0.25	0.4	V
			DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	$V_{CC} = 4.5V$, $I_{OH} = -1.0$ mA	DS1628	2.5	3.9		V
			DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	$V_{CC} = 4.5V$, $I_{OL} = 20$ mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	$V_{CC} = 4.5V$, $V_{OUT} = 0V$, (Note 6)			−150		mA
I_{OD}	Logical "0" Drive Current	$V_{CC} = 4.5V$, $V_{OUT} = 4.5V$, (Note 6)			150		mA
Hi-Z	TRI-STATE Output Current	$V_{OUT} = 0.4V$ to 2.4V, DIS1 or DIS2 = 2.0V		−40	0.1	40	μA
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$	One DIS Input = 3.0V All Other Inputs = X, Outputs at Hi-Z		90	120	mA
			DIS1, DIS2 = 0V, Others = 3V Outputs on		70	100	mA
			All Inputs = 0V, Outputs Off		25	50	mA

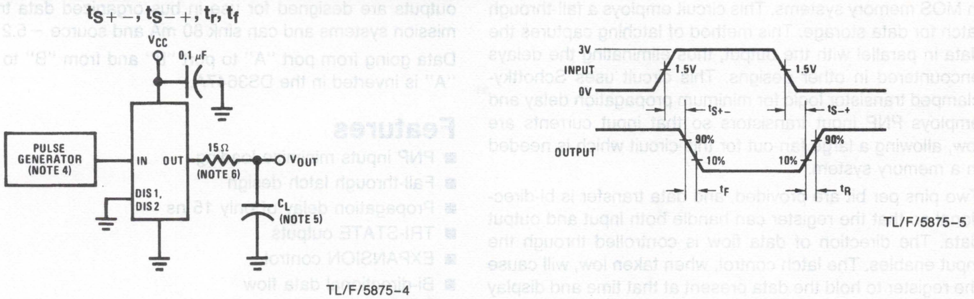
Switching Characteristics ($V_{CC} = 5V$, $T_A = 25°C$) (Note 6)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{S+-}	Storage Delay Negative Edge	(*Figure 1*)	$C_L = 50$ pF		4.0	5.0	ns
			$C_L = 500$ pF		6.5	8.0	
t_{S-+}	Storage Delay Positive Edge	(*Figure 1*)	$C_L = 50$ pF		4.2	5.0	ns
			$C_L = 500$ pF		6.5	8.0	
t_F	Fall Time	(*Figure 1*)	$C_L = 50$ pF		4.2	6.0	ns
			$C_L = 500$ pF		19	22	
t_R	Rise Time	(*Figure 1*)	$C_L = 50$ pF		5.2	7.0	ns
			$C_L = 500$ pF		20	24	
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	$C_L = 50$ pF to GND	$R_L = 2$ kΩ to V_{CC} (*Figure 2*)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$C_L = 50$ pF to GND	$R_L = 2$ kΩ to GND (*Figure 2*)		13	20	ns

Switching Characteristics (Continued) (V_{CC} = 5V, T_A = 25°C) (Note 6)

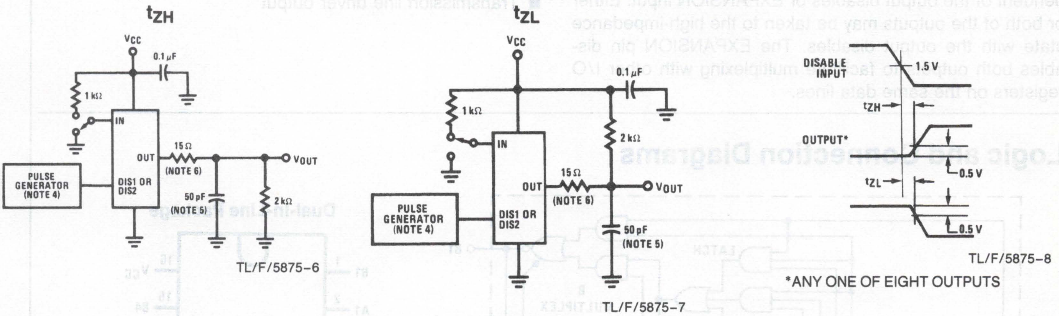
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to GND	R_L = 400Ω to V_{CC} (*Figure 3*)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to GND	R_L = 400Ω to GND (*Figure 3*)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms



t_{S+-}, t_{S-+}, t_r, t_f
VCC
0.1 µF
PULSE GENERATOR (NOTE 4)
IN
OUT
15Ω
(NOTE 6)
VOUT
DIS 1, DIS 2
CL (NOTE 5)
TL/F/5875-4
3V
INPUT
0V
1.5V
1.5V
tS+-
tS-+
90%
10%
90%
10%
OUTPUT
tF
tR
TL/F/5875-5

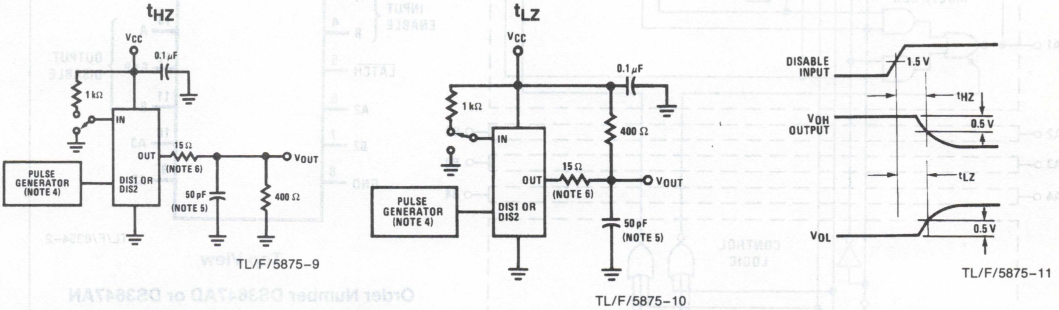
FIGURE 1



tZH
VCC
0.1 µF
1 kΩ
IN
OUT
15Ω
(NOTE 6)
VOUT
PULSE GENERATOR (NOTE 4)
DIS1 OR DIS2
50 pF (NOTE 5)
2 kΩ
TL/F/5875-6
tZL
VCC
0.1 µF
1 kΩ
2 kΩ
IN
OUT
15Ω
(NOTE 6)
VOUT
PULSE GENERATOR (NOTE 4)
DIS1 OR DIS2
50 pF (NOTE 5)
TL/F/5875-7
DISABLE INPUT
1.5 V
tZH
OUTPUT*
0.5 V
tZL
0.5 V
TL/F/5875-8

*ANY ONE OF EIGHT OUTPUTS

FIGURE 2



tHZ
VCC
0.1 µF
1 kΩ
IN
OUT
15Ω
(NOTE 6)
VOUT
PULSE GENERATOR (NOTE 4)
DIS1 OR DIS2
50 pF (NOTE 5)
400 Ω
TL/F/5875-9
tLZ
VCC
0.1 µF
1 kΩ
400 Ω
IN
OUT
15Ω
(NOTE 6)
VOUT
PULSE GENERATOR (NOTE 4)
DIS1 OR DIS2
50 pF (NOTE 5)
TL/F/5875-10
DISABLE INPUT
1.5 V
tHZ
VOH OUTPUT
0.5 V
tLZ
VOL
0.5 V
TL/F/5875-11

FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 mHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15Ω resistor should be placed in series with each output.

National Semiconductor

DS3647A Quad TRI-STATE® MOS Memory I/O Register

General Description

The DS3647A is a 4-bit I/O buffer register intended for use in MOS memory systems. This circuit employs a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. This circuit uses Schottky-clamped transistor logic for minimum propagation delay and employs PNP input transistors so that input currents are low, allowing a large fan-out for this circuit which is needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

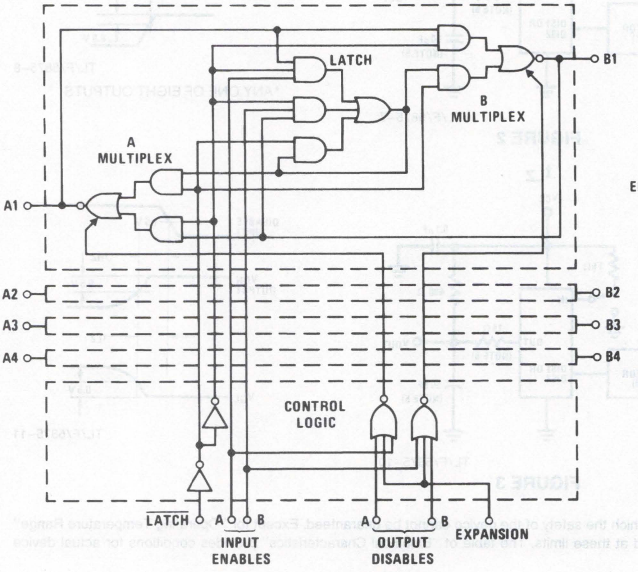
The DS3647A features TRI-STATE outputs. The "B" port outputs are designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA.

Data going from port "A" to port "B" and from "B" to port "A" is inverted in the DS3647A.

Features

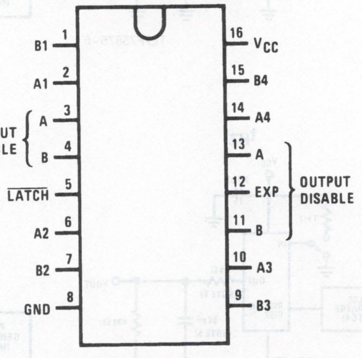
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams


LATCH
B
MULTIPLEX
A
MULTIPLEX
A1
B1
A2
A3
A4
B2
B3
B4
CONTROL
LOGIC
LATCH
A
B
INPUT
ENABLES
A
B
OUTPUT
DISABLES
EXPANSION

TL/F/8354–1

Dual-In-Line Package


B1 1
A1 2
INPUT ENABLE A 3
B 4
LATCH 5
A2 6
B2 7
GND 8
16 VCC
15 B4
14 A4
13 A
12 EXP
11 B
OUTPUT DISABLE
10 A3
9 B3

TL/F/8354–2

Top View

Order Number DS3647AD or DS3647AN
See NS Package Number D16C or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65° to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.0 mW/° C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS3647A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	$V_{CC}=5.5V$, $V_{IN}=5.5V$	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	$V_{CC}=5.5V$, $V_{IN}=0.5V$	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	$V_{CC}=4.5V$, $I_{IN}=-18$ mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	$V_{CC}=4.5V$, $I_{OL}=20$ mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	$V_{CC}=4.5V$	$I_{OL}=30$ mA		0.3	0.4	V
			$I_{OL}=50$ mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	$I_{OH}=-1$ mA	$V_{CC}=5V$	3.0	3.4		V
			$V_{CC}=4.5V$	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	$I_{OH}=-5.2$ mA, (Note 4)	$V_{CC}=5V$	2.9	3.3		V
			$V_{CC}=4.5V$	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	$V_{CC}=4.5V$ to 5.5V, $V_{OUT}=0V$, (Note 4)		−50	−80	−120	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	$V_{CC}=4.5V$ to 5.5V, $V_{OUT}=0V$, (Note 4)		−70	−120	−180	mA
I_{CC}	Power Supply Current	Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS3647A		100	140	mA
		Enable A, Latch = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS3647A		70	105	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for $V_{CC}=5V$ and $T_A=25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Switching Characteristics (V_{CC}=5V, T_A=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA TRANSFER B PORT TO A PORT						
t_{pd0}	Propagation Delay to a Logic "0"	CL = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS3647A						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS3647A						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before Latch Goes Low		5	0		ns
t_{HOLD}	Hold Time of Data Input After Latch Goes Low		10	5		ns

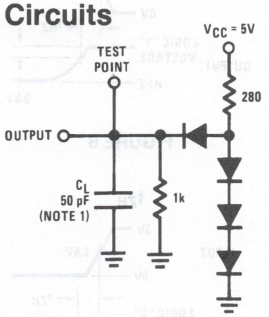
Product Description

Device Number	B Port To A Port Function	A Port To B Port Function	A Port Outputs	B Port Outputs
DS3647A	Inverting	Inverting	TRI-STATE	TRI-STATE

Truth Table

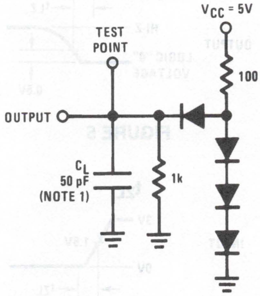
Input Enables		$\overline{\text{Latch}}$	Output Disables		Expansion	A Ports A1-A4	B Ports B1-B4	Comments
A	B		A	B				
1	0	1	0	0	0	Hi-Z	$\overline{A}$	Data in on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Data in on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	x	0	1	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on A, may be latched
0	1	x	1	0	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on B, may be latched
x	x	x	x	x	1	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits


V_{CC} = 5V
TEST POINT
280
OUTPUT
C_L
50 pF
(NOTE 1)
1k

TL/F/8354-3

FIGURE 1. A Port Load


V_{CC} = 5V
TEST POINT
100
OUTPUT
C_L
50 pF
(NOTE 1)
1k

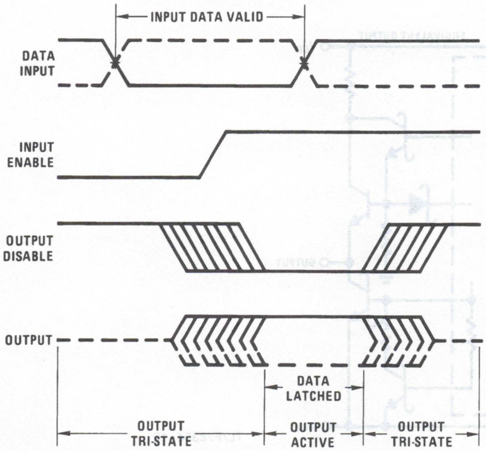
TL/F/8354-4

FIGURE 2. B Port Load

Note 1: C_L includes probe and jig capacitance.

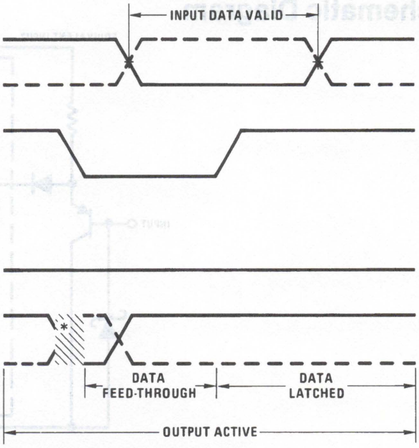
Operating Waveforms

Using TRI-STATE


INPUT DATA VALID
DATA INPUT
INPUT ENABLE
OUTPUT DISABLE
OUTPUT
DATA LATCHED
OUTPUT TRI-STATE
OUTPUT ACTIVE
OUTPUT TRI-STATE

TL/F/8354-5

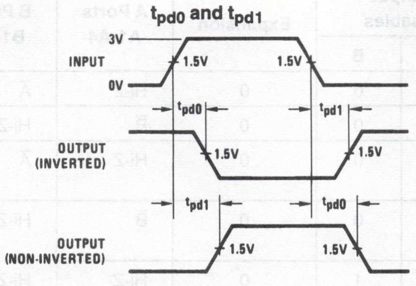
TRI-STATE Disabled


INPUT DATA VALID
*
DATA FEED-THROUGH
DATA LATCHED
OUTPUT ACTIVE

TL/F/8354-6

*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

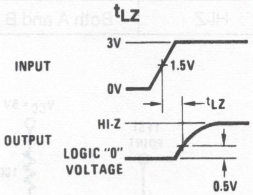
Switching Time Waveforms


t_{pd0} and t_{pd1}
3V
INPUT
0V
1.5V
1.5V
t_{pd0}
t_{pd1}
OUTPUT
(INVERTED)
1.5V
1.5V
t_{pd1}
t_{pd0}
OUTPUT
(NON-INVERTED)
1.5V
1.5V

TL/F/8354-7

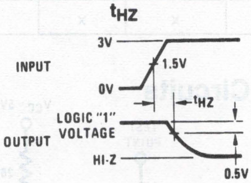
Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4


t_{LZ}
3V
INPUT
1.5V
0V
t_{LZ}
HI-Z
OUTPUT
LOGIC "0"
VOLTAGE
0.5V

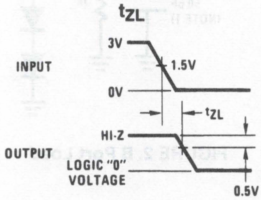
TL/F/8354-8

FIGURE 5


t_{HZ}
3V
INPUT
1.5V
0V
t_{HZ}
LOGIC "1"
VOLTAGE
OUTPUT
HI-Z
0.5V

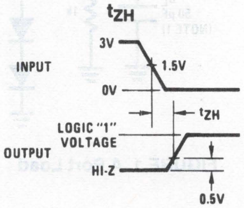
TL/F/8354-10

FIGURE 6


t_{ZL}
3V
INPUT
1.5V
0V
t_{ZL}
HI-Z
OUTPUT
LOGIC "0"
VOLTAGE
0.5V

TL/F/8354-9

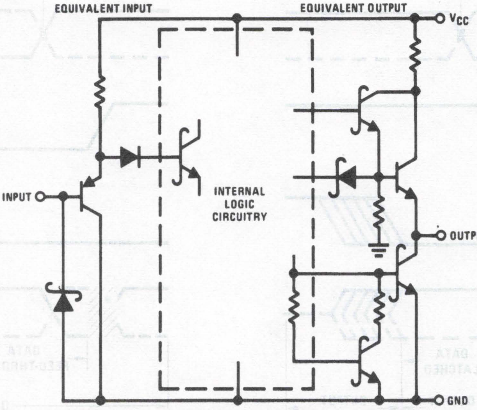
FIGURE 7


t_{ZH}
3V
INPUT
1.5V
0V
t_{ZH}
LOGIC "1"
VOLTAGE
OUTPUT
HI-Z
0.5V

TL/F/8354-11

FIGURE 8

Schematic Diagram

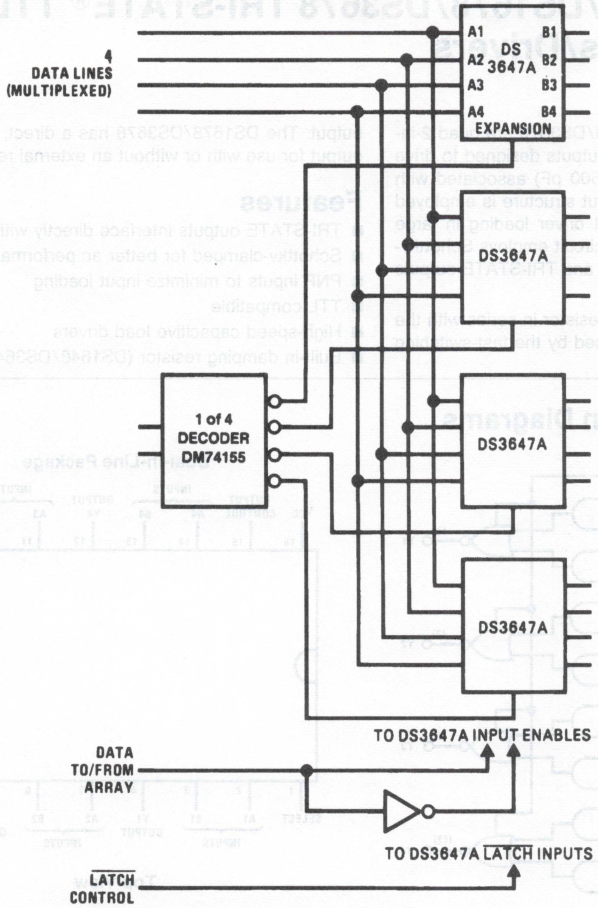

EQUIVALENT INPUT
EQUIVALENT OUTPUT
V_{CC}
INPUT
INTERNAL
LOGIC
CIRCUITRY
OUTPUT
GND

TL/F/8354-12

Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3647A can be used as a register capable of multiplexing data lines.


A1
B1
DS
3647A
A2
B2
A3
B3
A4
B4
EXPANSION
4
DATA LINES
(MULTIPLEXED)
DS3647A
16
DATA LINES
TO MOS
MEMORY
ARRAY
1 of 4
DECODER
DM74155
DS3647A
DS3647A
TO DS3647A INPUT ENABLES
DATA
TO/FROM
ARRAY
TO DS3647A $\overline{\text{LATCH}}$ INPUTS
$\overline{\text{LATCH}}$
CONTROL

TL/F/8354-13

National Semiconductor

DS1648/DS3648/DS1678/DS3678 TRI-STATE® TTL to MOS Multiplexers/Drivers

General Description

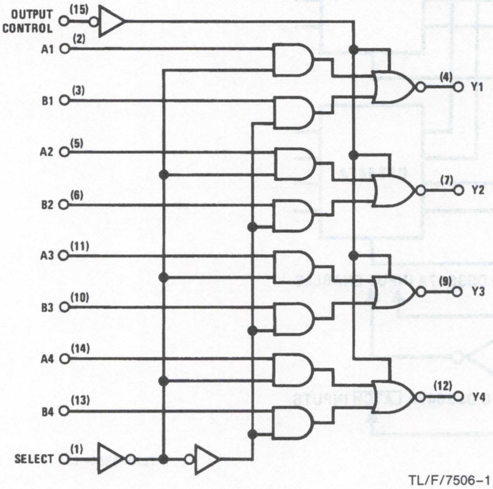
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

Features

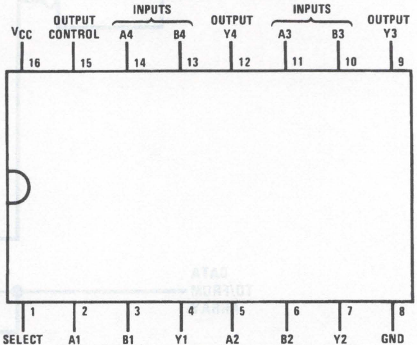
- TRI-STATE outputs interface directly with system-bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams


OUTPUT CONTROL (15)
A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
SELECT (1)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/7506–1

Dual-In-Line Package


INPUTS
INPUTS
V_{CC} 16
OUTPUT CONTROL 15
A4 14
B4 13
OUTPUT Y4 12
A3 11
B3 10
OUTPUT Y3 9
SELECT 1
A1 2
B1 3
Y1 OUTPUT 4
A2 5
B2 6
Y2 OUTPUT 7
GND 8
INPUTS
INPUTS

TL/F/7506–2

Top View

Order Number DS1648J, DS3648J, DS1678J DS3678J, DS3648N or DS3678N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 5.5V$			0.1	40	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.5V$			−50	−250	µA
V_{CLAMP}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	$V_{CC} = 4.5V$, $I_{OH} = -10$ µA	DS1648/DS1678	2.7	3.6		V
			DS3648/DS3678	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	$V_{CC} = 4.5V$, $I_{OL} = 10$ µA	DS1648/DS1678		0.25	0.4	V
			DS3648/DS3678		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	$V_{CC} = 4.5V$, $I_{OH} = -1.0$ mA	DS1648	2.4	3.5		V
			DS1678	2.5	3.5		V
			DS3648	2.6	3.5		V
			DS3678	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	$V_{CC} = 4.5V$, $I_{OL} = 20$ mA	DS1648		0.6	1.1	V
			DS1678		0.4	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	$V_{CC} = 4.5V$, $V_{OUT} = 0V$, (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	$V_{CC} = 4.5V$, $V_{OUT} = 4.5V$, (Note 4)			150		mA
$I_{Hi\text{-}Z}$	TRI-STATE Output Current	$V_{OUT} = 0.4V$ to 2.4V, Output Control = 2.0V		−40		40	µA
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$	Output Control = 3V All Other Inputs at 0V		42	60	mA
			All Inputs at 0V		20	32	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values for $T_A = 25°C$ and $V_{CC} = 5V$.

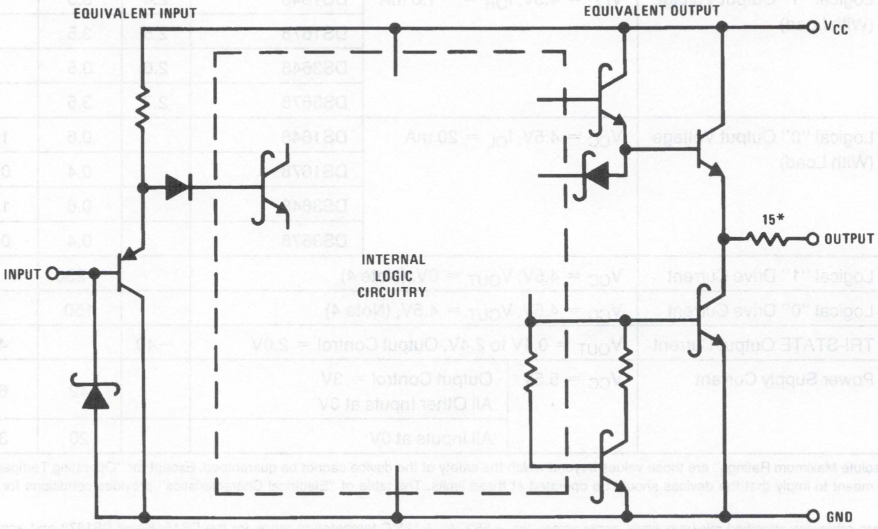
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$ (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	*(Figure 1)*	$C_L = 50\ pF$		5	7	ns
			$C_L = 500\ pF$		9	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	*(Figure 1)*	$C_L = 50\ pF$		6	8	ns
			$C_L = 500\ pF$		9	13	ns
t_F	Fall Time	*(Figure 1)*	$C_L = 50\ pF$		5	8	ns
			$C_L = 500\ pF$		22	35	ns
t_R	Rise Time	*(Figure 1)*	$C_L = 50\ pF$		6	9	ns
			$C_L = 500\ pF$		22	35	ns
t_{ZL}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	$C_L = 50\ pF, R_L = 2\ k\Omega$ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	$C_L = 50\ pF, R_L = 2\ k\Omega$ to GND *(Figure 2)*			8	15	ns
t_{LZ}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	$C_L = 50\ pF, R_L = 400\Omega$ to V_{CC}, *(Figure 3)*			15	25	ns
t_{HZ}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	$C_L = 50\ pF, R_L = 400\Omega$ to GND, *(Figure 3)*			10	25	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects A	$C_L = 50\ pF$, *(Figure 1)*			12	15	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects A	$C_L = 50\ pF$, *(Figure 1)*			14	17	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects B	$C_L = 50\ pF$, *(Figure 1)*			16	20	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects B	$C_L = 50\ pF$, *(Figure 1)*			14	20	ns

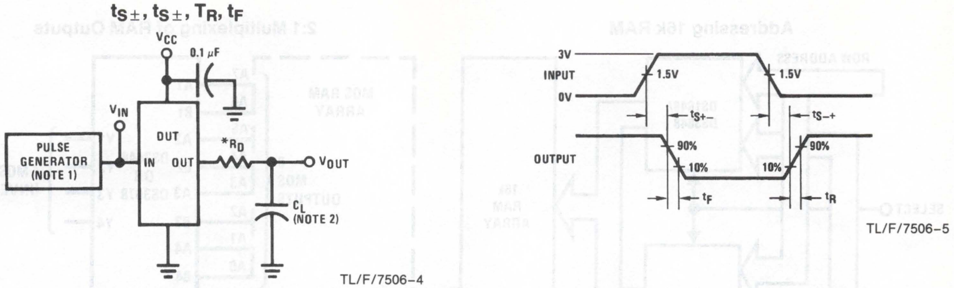
Schematic Diagram



TL/F/7506-3

*DS1648/DS3648 only

AC Test Circuits and Switching Time Waveforms


tS±, tS±, TR, tF
VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
IN
OUT
OUT
*RD
VOUT
CL (NOTE 2)
3V
INPUT
0V
1.5V
1.5V
tS+−
tS−+
OUTPUT
90%
10%
10%
90%
tF
tR

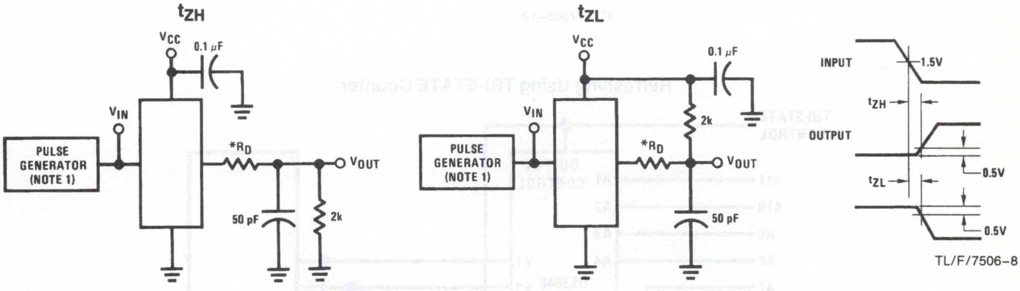
TL/F/7506-4

TL/F/7506-5

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

FIGURE 1


tZH
VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
*RD
VOUT
50 pF
2k
tZL
VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
2k
*RD
VOUT
50 pF
INPUT
1.5V
tZH
OUTPUT
0.5V
tZL
0.5V

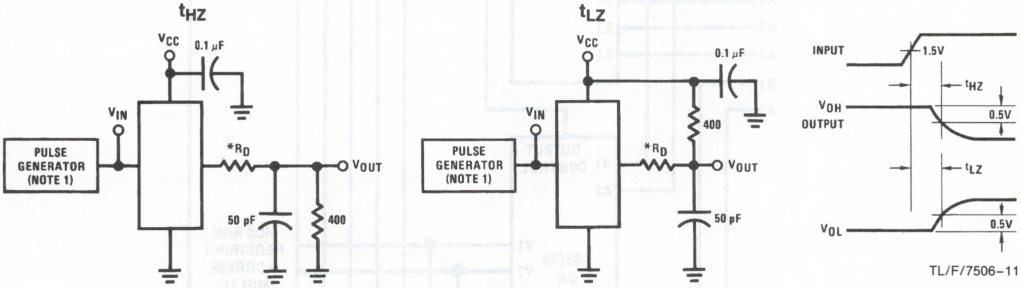
TL/F/7506-6

TL/F/7506-7

TL/F/7506-8

*Internal on DS1648 and DS3648

FIGURE 2


tHZ
VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
*RD
VOUT
50 pF
400
tLZ
VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
400
*RD
VOUT
50 pF
INPUT
1.5V
tHZ
VOH
OUTPUT
0.5V
tLZ
VOL
0.5V

TL/F/7506-9

TL/F/7506-10

TL/F/7506-11

*Internal on DS1648 and DS3648

FIGURE 3

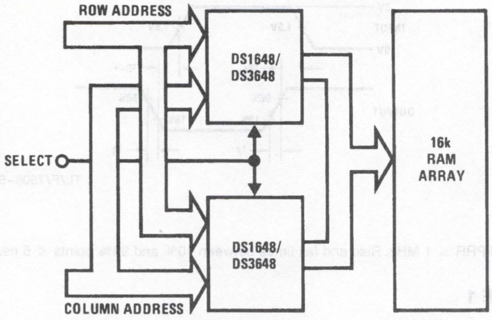
Truth Table

Output Control	Inputs			Outputs
	Select	A	B	
H	X	X	X	Hi-Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
L = Low level
X = Don't care
Hi-Z = TRI-STATE mode

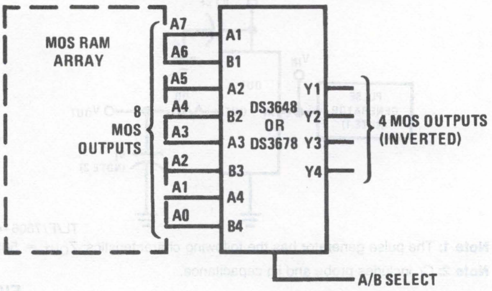
Typical Applications

Addressing 16k RAM


ROW ADDRESS
DS1648/
DS3648
SELECT
DS1648/
DS3648
COLUMN ADDRESS
16k
RAM
ARRAY

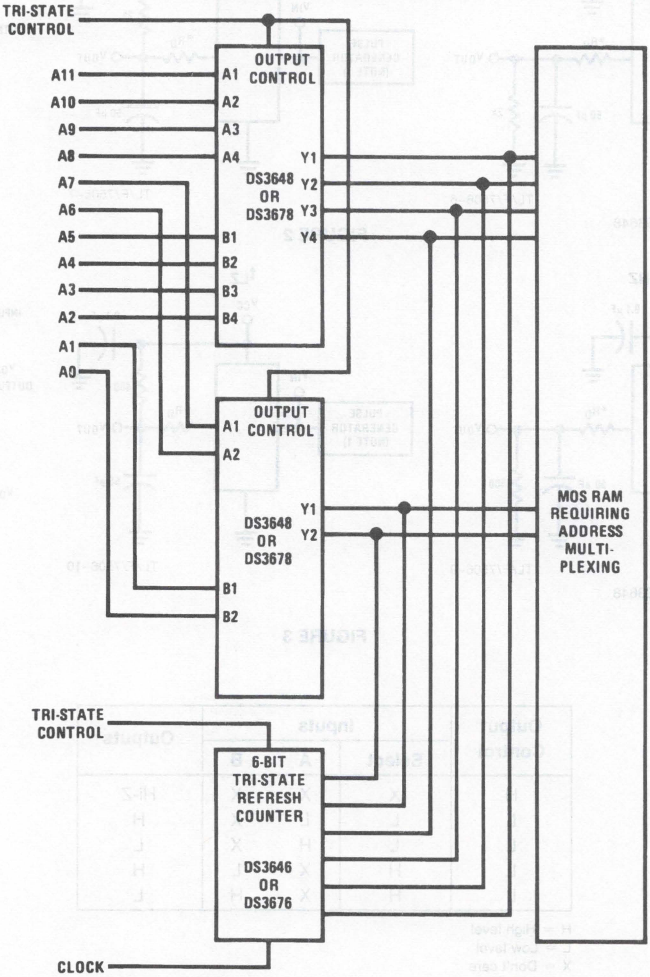
TL/F/7506-12

2:1 Multiplexing of RAM Outputs


MOS RAM
ARRAY
8
MOS
OUTPUTS
A7
A6
A5
A4
A3
A2
A1
A0
A1
B1
A2
B2
A3
B3
A4
B4
DS3648
OR
DS3678
Y1
Y2
Y3
Y4
4 MOS OUTPUTS
(INVERTED)
A/B SELECT

TL/F/7506-14

Refreshing Using TRI-STATE Counter


TRI-STATE
CONTROL
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
OUTPUT
CONTROL
A1
A2
A3
A4
DS3648
OR
DS3678
B1
B2
B3
B4
Y1
Y2
Y3
Y4
OUTPUT
CONTROL
A1
A2
DS3648
OR
DS3678
B1
B2
Y1
Y2
MOS RAM
REQUIRING
ADDRESS
MULTI-
PLEXING
TRI-STATE
CONTROL
6-BIT
TRI-STATE
REFRESH
COUNTER
DS3646
OR
DS3676
CLOCK

TL/F/7506-13

National Semiconductor

DS1649/DS3649/DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

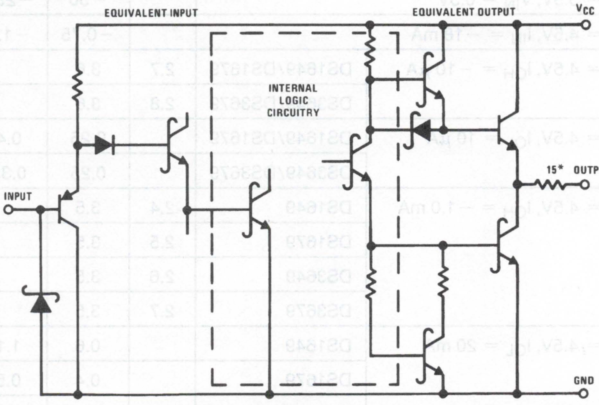
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram


EQUIVALENT INPUT
EQUIVALENT OUTPUT
V_{CC}
INTERNAL LOGIC CIRCUITRY
INPUT
15* OUTPUT
GND

*DS1649/DS3649 only

TL/F/7515–1

Truth Table

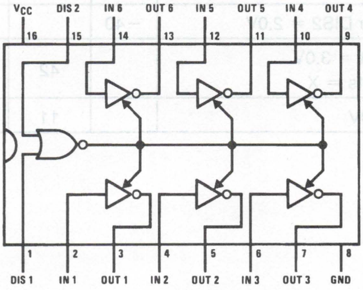
Disable Input		Input	Output
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care

Hi-Z = TRI-STATE mode

Connection Diagram

Dual-In-Line Package

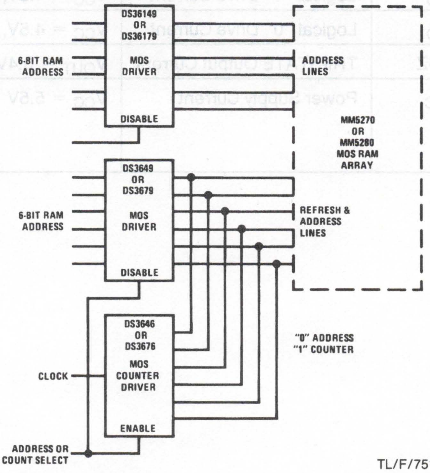

V_{CC}
DIS 2
IN 6
OUT 6
IN 5
OUT 5
IN 4
OUT 4
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
DIS 1
IN 1
OUT 1
IN 2
OUT 2
IN 3
OUT 3
GND

TL/F/7515–2

Top View

Order Number DS1649J, DS3649J, DS1679J, DS3679J, DS3649N or DS3679N
See NS Package Number J16A or N16A

Typical Application


DS36149 OR DS36179
MOS DRIVER
DISABLE
6-BIT RAM ADDRESS
ADDRESS LINES
MM5270 OR MM5280 MOS RAM ARRAY
DS3649 OR DS3679
MOS DRIVER
DISABLE
6-BIT RAM ADDRESS
REFRESH & ADDRESS LINES
DS3646 OR DS3676
MOS COUNTER DRIVER
ENABLE
CLOCK
ADDRESS OR COUNT SELECT
"0" ADDRESS
"1" COUNTER

TL/F/7515–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	−55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Note 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5.5V, V_{IN} = 5.5V$			0.1	40	µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5.5V, V_{IN} = 0.5V$			−50	−250	µA
V_{CLAMP}	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN} = -18$ mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OH} = -10$ µA	DS1649/DS1679	2.7	3.6		V
			DS3649/DS3679	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OL} = 10$ µA	DS1649/DS1679		0.25	0.4	V
			DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OH} = -1.0$ mA	DS1649	2.4	3.5		V
			DS1679	2.5	3.5		V
			DS3649	2.6	3.5		V
			DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OL} = 20$ mA	DS1649		0.6	1.1	V
			DS1679		0.4	0.5	V
			DS3649		0.6	1.0	V
			DS3679		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 0V$ (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 4.5V$ (Note 4)			150		mA
Hi-Z	TRI-STATE Output Current	$V_{OUT} = 0.4V$ to 2.4V, DIS1 or DIS2 = 2.0V		−40		40	µA
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$	One DIS Input = 3.0V All Other Inputs = X		42	75	mA
			All Inputs = 0V		11	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
$t_{S\pm}$	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to V_{CC} (*Figure 2*)			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to GND (*Figure 2*)			8	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF R_L = 400Ω to V_{CC} (*Figure 3*)			15	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF R_L = 400Ω to GND (*Figure 3*)			10	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

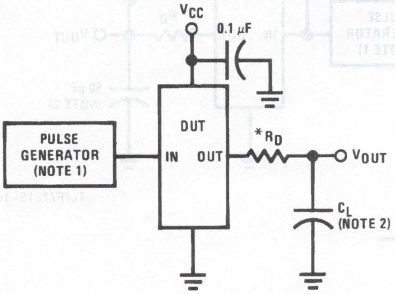
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

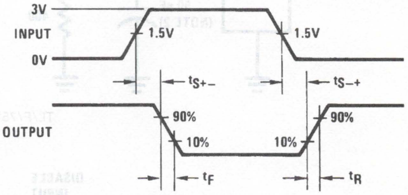
Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

$t_{S\pm}$, $t_{S\mp}$, t_R, t_F



TL/F/7515–4



TL/F/7515–5

FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)

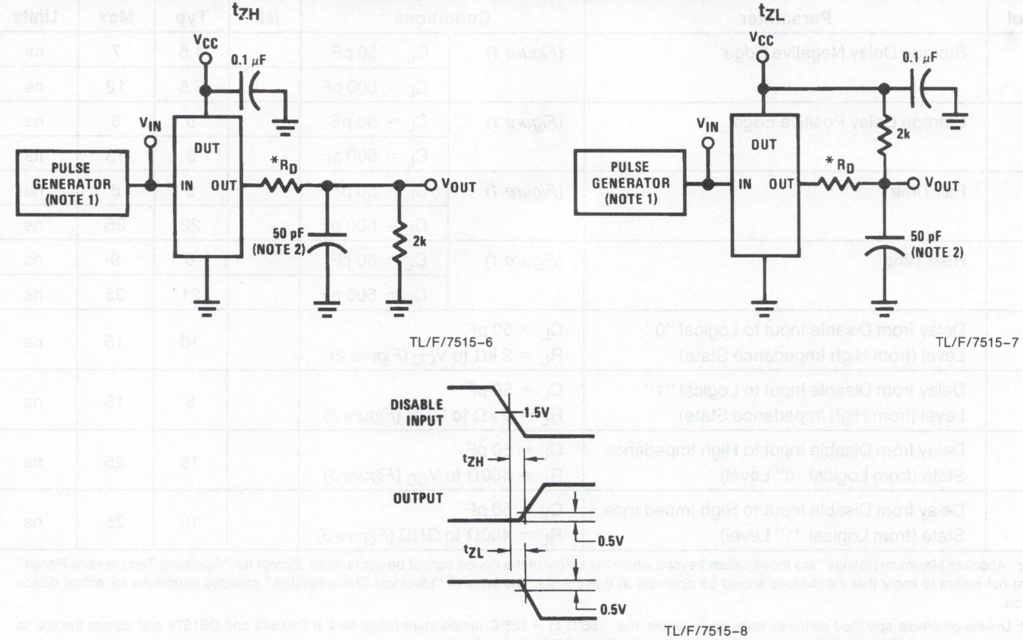
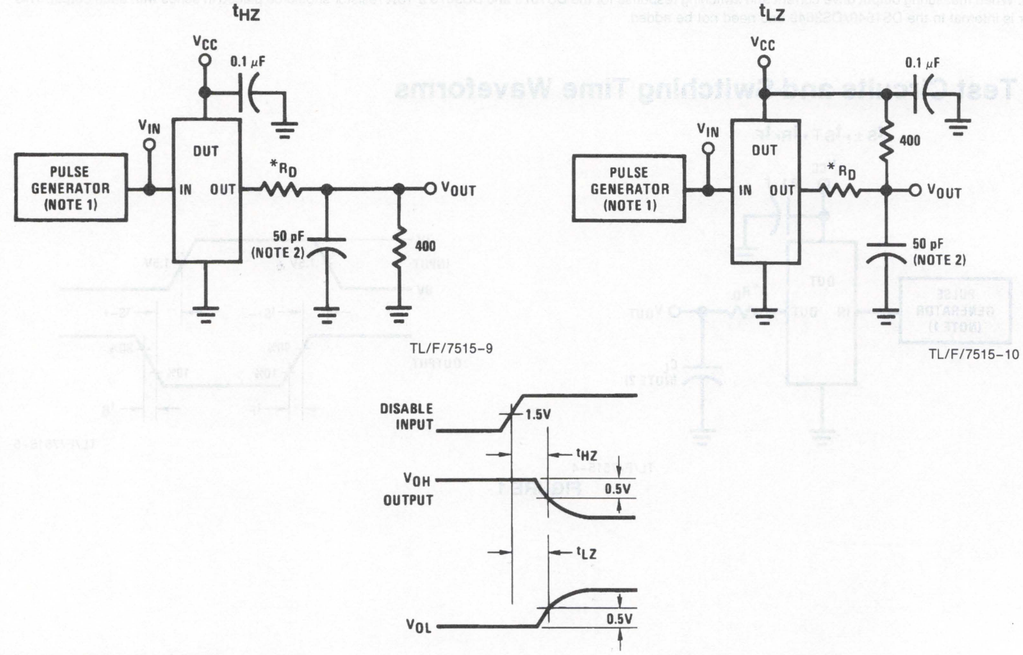

t_{ZH}
V_{CC}
0.1 µF
V_{IN}
PULSE GENERATOR (NOTE 1)
DUT
IN
OUT
*R_D
V_{OUT}
50 pF (NOTE 2)
2k
TL/F/7515-6
t_{ZL}
V_{CC}
0.1 µF
V_{IN}
PULSE GENERATOR (NOTE 1)
DUT
IN
OUT
2k
*R_D
V_{OUT}
50 pF (NOTE 2)
TL/F/7515-7
DISABLE INPUT
1.5V
t_{ZH}
OUTPUT
t_{ZL}
0.5V
0.5V
TL/F/7515-8

FIGURE 2


t_{HZ}
V_{CC}
0.1 µF
V_{IN}
PULSE GENERATOR (NOTE 1)
DUT
IN
OUT
*R_D
V_{OUT}
50 pF (NOTE 2)
400
TL/F/7515-9
t_{LZ}
V_{CC}
0.1 µF
V_{IN}
DUT
400
PULSE GENERATOR (NOTE 1)
IN
OUT
*R_D
V_{OUT}
50 pF (NOTE 2)
TL/F/7515-10
DISABLE INPUT
1.5V
t_{HZ}
V_{OH}
OUTPUT
0.5V
t_{LZ}
V_{OL}
0.5V

*Internal on DS1649 and DS3649

TL/F/7515-11

FIGURE 3

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS1651/DS3651
Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 is TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

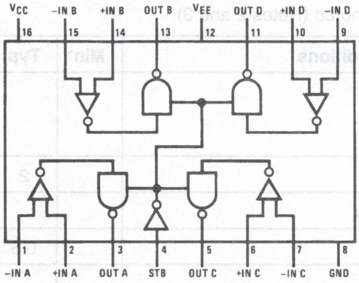
The DS1651/DS3651 has active pull-up outputs and offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430

Connection Diagram

Dual-In-Line Package


VCC
−IN B
+IN B
OUT B
VEE
OUT D
+IN D
−IN D
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
−IN A
+IN A
OUT A
STB
OUT C
+IN C
−IN C
GND

Top View

TL/F/7528–1

Order Number DS1651J, DS3651J or DS3651N
See NS Package Number J16A or N16A

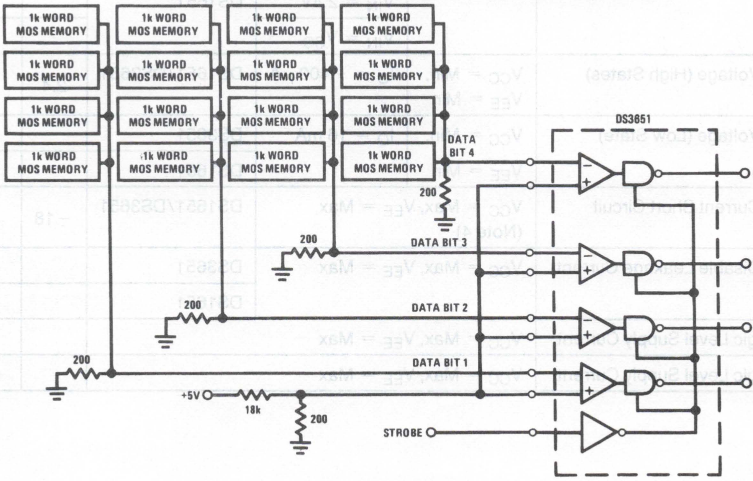
Truth Table

Input	Strobe	Output DS3651
$V_{ID} \geq 7$ mV T_A = 0°C to +70°C	L H	H Open
−7 mV ≤ V_{ID} ≤ +7 mV T_A = 0°C to +70°C	L H	X Open
$V_{ID} \geq -7$ mV T_A = 0°C to +70°C	L H	L Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

Typical Applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices


1k WORD MOS MEMORY
DATA BIT 4
DATA BIT 3
DATA BIT 2
DATA BIT 1
200
200
200
200
200
+5V
18k
200
STROBE
DS3651
DATA BIT 4
DATA BIT 3
DATA BIT 2
DATA BIT 1

Note: Only 4 devices are required for a 4k word by 16-bit memory system.

TL/F/7528–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	$+7\ V_{DC}$
V_{EE}	$-7\ V_{DC}$
Differential-Mode Input Signal Voltage Range, V_{IDR}	$\pm6\ V_{DC}$
Common-Mode Input Voltage Range, V_{ICR}	$\pm5\ V_{DC}$
Strobe Input Voltage, $V_{I(S)}$	$5.5\ V_{DC}$
Strobe Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temp. (Soldering, 10 seconds)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})			
DS1651	4.5	5.5	V
DS3651	4.75	5.25	V
Supply Voltage (V_{EE})			
DS1651	−4.5	−5.5	V
DS3651	−4.75	−5.25	V
Operating Temperature (T_A)			
DS1651	−55	+125	°C
DS3651	0	+70	°C
Output Load Current, (I_{OL})		16	mA
Differential Mode Input Voltage Range, (V_{IDR})	−5.0	+5.0	V
Common-Mode Input Voltage Range, (V_{ICR})	−3.0	+3.0	V
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V

Electrical Characteristics

$V_{CC} = 5\ V_{DC}$, $V_{EE} = -5\ V_{DC}$, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range) VICR = $-3V \le V_{IN} \le +3V$)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	µA
I_{IO}	Input Offset Current					0.5		µA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IL(S)}$	Strobe Current (High State)	V_{CC} = Max,	V_{IN} = 2.4V	DS3651			40	µA
		V_{EE} = Max	V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651			100	µA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High States)	V_{CC} = Min, V_{EE} = Min	I_O = −400 µA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min,	I_O = 16 mA	DS3651			0.45	V
		V_{EE} = Min		DS1651			0.50	
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 4)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	µA
				DS1651			100	µA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

Switching Characteristics $V_{CC} = 5\ V_{DC}$, $V_{EE} = -5\ V_{DC}$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 2*)	DS1651/ DS3651		23	45	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 2*)	DS1651/ DS3651		22	55	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		14	29	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

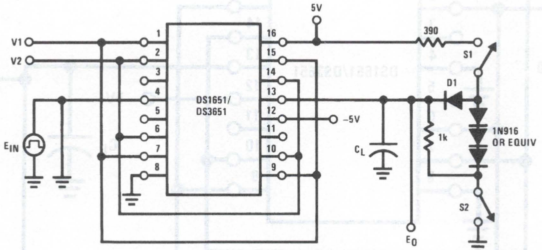
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651 and across the −55°C to +125°C range for the DS1651. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{EE} = -5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651 and DS3651 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differiential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Time Waveform



TL/F/7528-3

Note: Output of channel B shown under test, other channels are tested similarly.

Delay	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

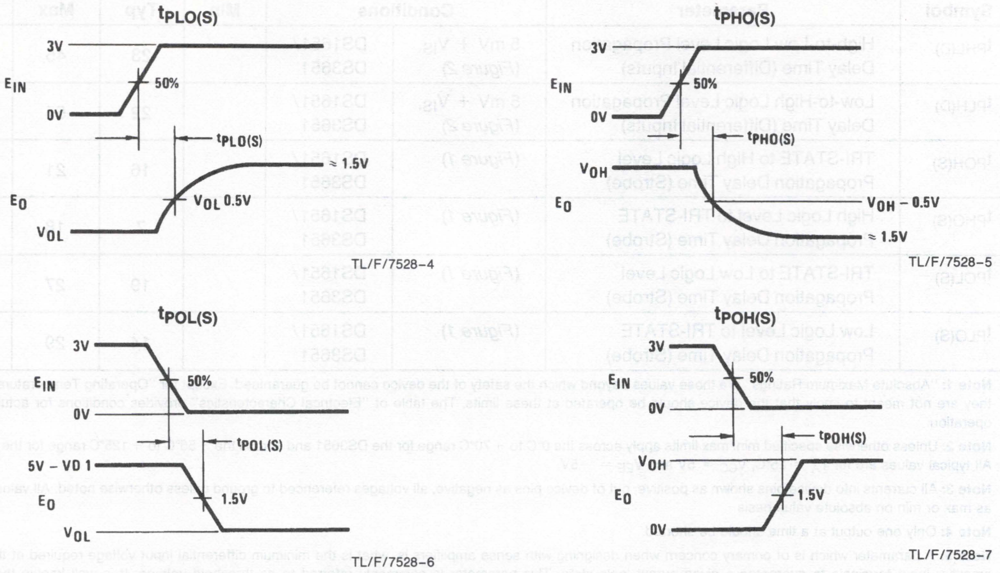
C_L includes jig and probe capacitance.

E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%

PRR = 1 MHz

Duty cycle = 50%

AC Test Circuits


tPLO(S)
3V
EIN
50%
0V
tPLO(S)
≈ 1.5V
EO
VOL 0.5V
VOL
tPHO(S)
3V
EIN
50%
0V
tPHO(S)
VOH
EO
VOH − 0.5V
≈ 1.5V
tPOL(S)
3V
EIN
50%
0V
tPOL(S)
5V − VD 1
EO
1.5V
VOL
tPOH(S)
3V
EIN
50%
0V
tPOH(S)
VOH
EO
1.5V
0V

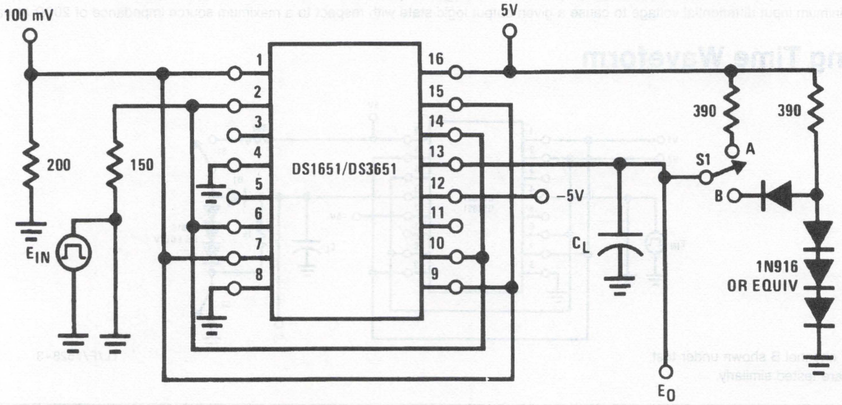
TL/F/7528–4

TL/F/7528–5

TL/F/7528–6

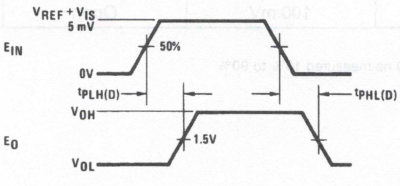
TL/F/7528–7

FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$


100 mV
5V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200
150
EIN
DS1651/DS3651
−5V
390
390
A
S1
B
CL
1N916
OR EQUIV
EO

TL/F/7528–10

Note: Output of channel B shown under test, other channels are tested similarly.
S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651


VREF + VIS
5 mV
EIN
50%
0V
tPLH(D)
tPHL(D)
VOH
EO
1.5V
VOL

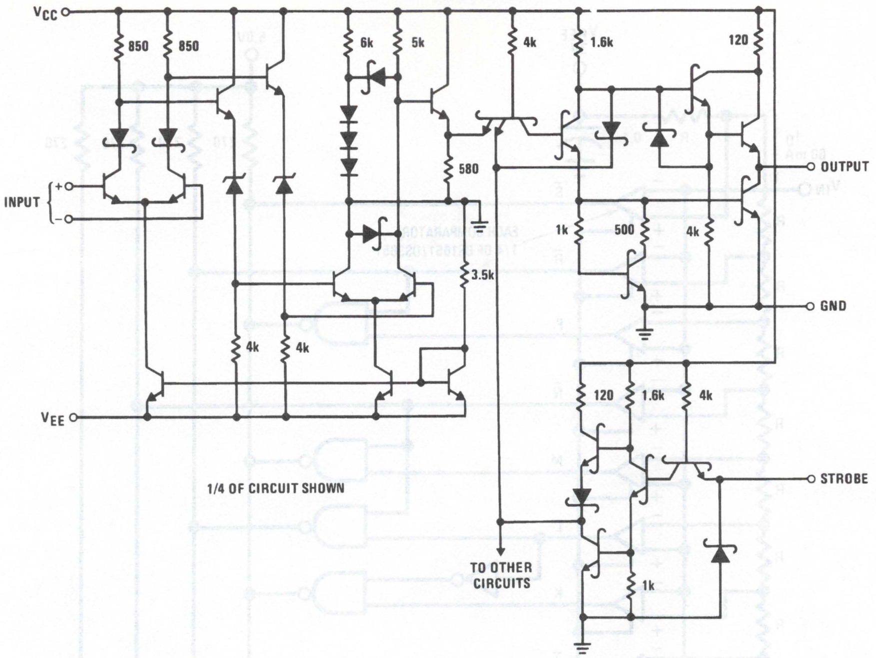
TL/F/7528–11

E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

Schematic Diagrams

DS1651/DS3651

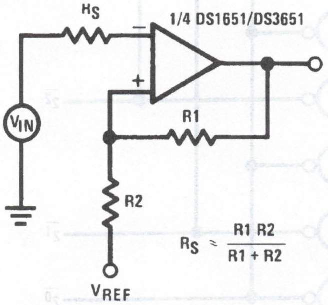


V_CC
850
850
6k
5k
4k
1.6k
120
OUTPUT
INPUT
+
−
580
1k
500
4k
GND
3.5k
4k
4k
V_EE
120
1.6k
4k
STROBE
1/4 OF CIRCUIT SHOWN
TO OTHER CIRCUITS
1k

TL/F/7528-12

Typical Applications

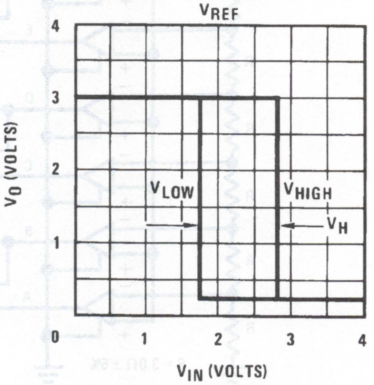
Level Detector with Hysteresis



R_S
1/4 DS1651/DS3651
−
+
V_IN
R1
R2
V_REF
R_S ≈ R1 R2 / (R1 + R2)

TL/F/7528-15

Transfer Characteristics and Equations for Level Detector with Hysteresis



TL/F/7528-16

$$V_{HIGH} = V_{REF} + \frac{R2\,[V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

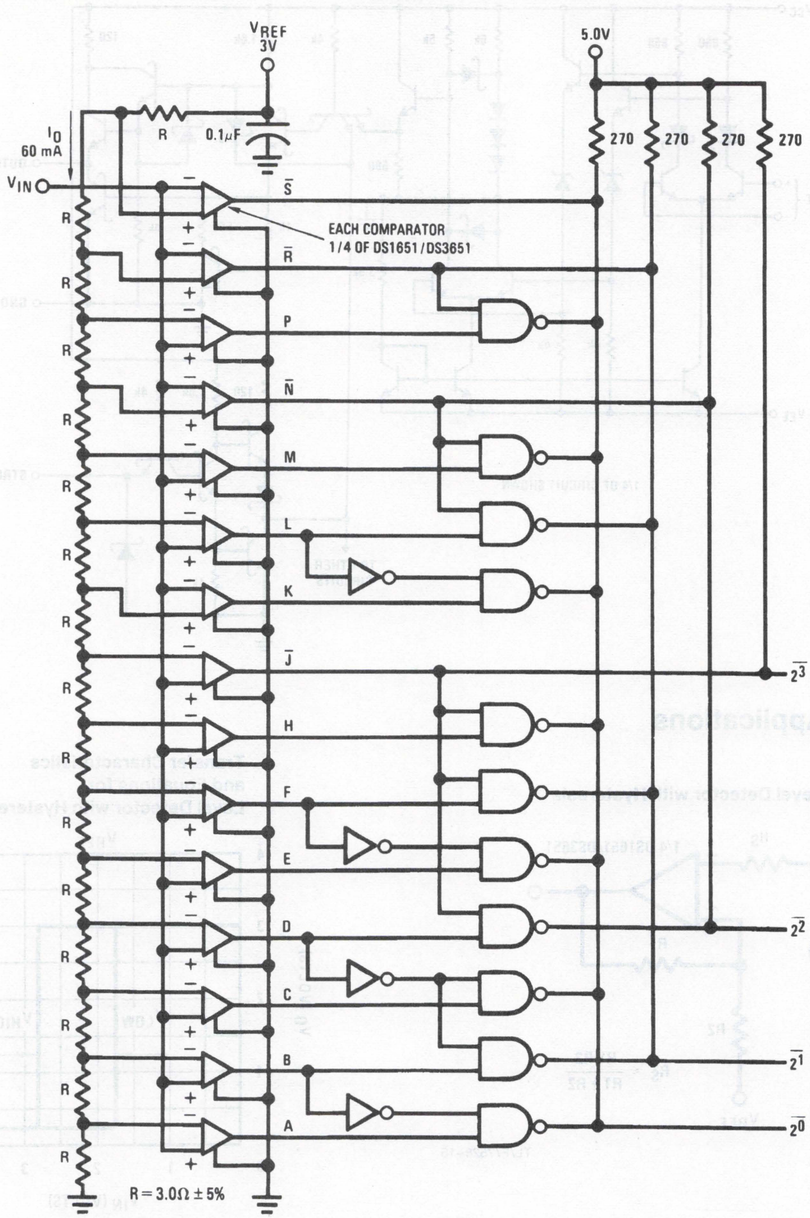
$$V_{LOW} = V_{REF} + \frac{R2\,[V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\,[V_{O(MAX)} - V_{O(MIN)}]$$

Typical Applications (Continued)

4-Bit Parallel A/D Converter


V_{REF}
3V
I_O
60 mA
V_{IN}
R
0.1μF
5.0V
270
270
270
270
$\overline{S}$
EACH COMPARATOR
1/4 OF DS1651/DS3651
$\overline{R}$
P
$\overline{N}$
M
L
K
$\overline{J}$
H
F
E
D
C
B
A
$\overline{2^3}$
$\overline{2^2}$
$\overline{2^1}$
$\overline{2^0}$
+
−
R = 3.0Ω ± 5%

TL/F/7528-14

$\overline{2^0} = (\overline{A} + B)\ (\overline{C} + D)\ (\overline{E} + F)\ (\overline{H} + J)\ (\overline{K} + L)\ (\overline{M} + N)\ (\overline{P} + R)\ (\overline{S})$

$\overline{2^1} = (\overline{B} + D)\ (\overline{F} + J)\ (\overline{L} + N)\ (\overline{R})$

$\overline{2^2} = (\overline{D} + J)\ (\overline{N})$

$\overline{2^3} = \overline{J}$

Conversion time ≅ 50 ns

National Semiconductor

DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1674/DS3674 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transisitors are used on all inputs thereby minimizing input loading.

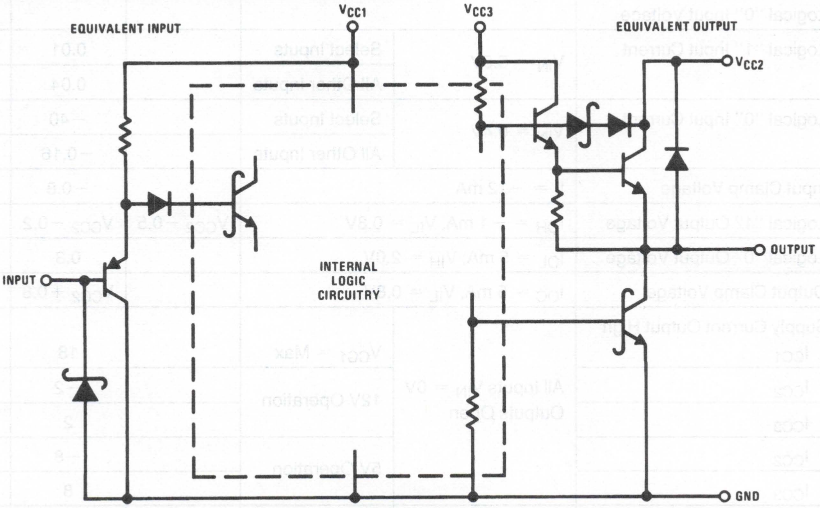
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

- TTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235

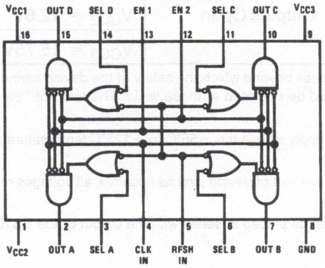
Schematic and Connection Diagrams



EQUIVALENT INPUT
VCC1
VCC3
EQUIVALENT OUTPUT
VCC2
INPUT
INTERNAL LOGIC CIRCUITRY
OUTPUT
GND

TL/F/5876-1

Dual-In-Line Package



VCC1
OUT D
SEL D
EN 1
EN 2
SEL C
OUT C
VCC3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
VCC2
OUT A
SEL A
CLK IN
RFSH IN
SEL B
OUT B
GND

TL/F/5876-2

Top View

Order Number DS3674J or DS3674N

See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC1}			
DS1674	4.5	5.5	V
DS3674	4.75	5.25	V
V_{CC2}			
DS1674	4.5	13.2	V
DS3674	4.75	12.6	V
V_{CC3}			
DS1674	V_{CC2}	16.5	V
DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1674	−55	+125	°C
DS3674	0	+70	°C

Electrical Characteristics

5V operation, ($V_{CC1} = V_{CC2} = 5V$, $V_{CC3} = 12V$); 12V operation, ($V_{CC1} = 5V$, $V_{CC2} = 12V$, $V_{CC3} = V_{CC2} + (3V \pm 10\%)$); DS1674, ±10% power supply tolerances; DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	$V_{IN} = 5.5V$	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	$I_I = -12$ mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -1$ mA, $V_{IL} = 0.8V$		$V_{CC2} - 0.5$	$V_{CC2} - 0.2$		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 5$ mA, $V_{IH} = 2.0V$			0.3	0.5	V
V_{OC}	Output Clamp Voltage	$I_{OC} = 5$ mA, $V_{IL} = 0.8V$			$V_{CC2} + 0.8$	$V_{CC2} + 1.5$	V
I_{CCH}	Supply Current Output High	All Inputs $V_{IN} = 0V$ Outputs Open					
	I_{CC1}		V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low	All Inputs $V_{IN} = 5V$ Outputs Open					
	I_{CC1}		$V_{CC1} = 5.25V$		25	40	mA
	I_{CC2}		$V_{CC2} = 12.6V$			3	mA
	I_{CC3}		$V_{CC3} = 15.75V$		16	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1674 and across the 0°C to +70°C range for the DS3674. All typicals are given for $T_A = 25°C$.

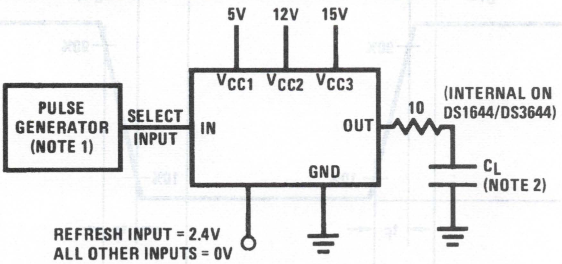
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674.

Switching Characteristics T_A = 25°C unless otherwise noted, (Note 4), (*Figures 1, 2, 3 and 4*)

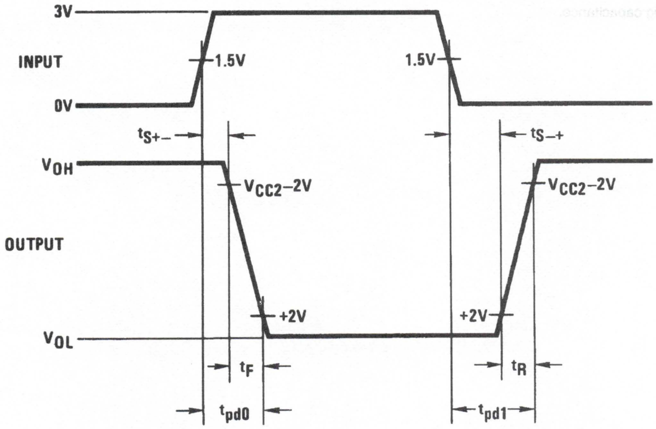
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{s+-}	Storage Delay Negative Edge	$R_D = 10\Omega$	$C_L = 100$ pF		8	11	ns
			$C_L = 400$ pF		12	16	ns
t_{s-+}	Storage Delay Positive Edge	$R_D = 10\Omega$	$C_L = 100$ pF		10	13	ns
			$C_L = 400$ pF		13	16	ns
t_F	Fall Time	$R_D = 10\Omega$	$C_L = 100$ pF		9	16	ns
			$C_L = 400$ pF		17	24	ns
t_R	Rise Time	$R_D = 10\Omega$	$C_L = 100$ pF		8	12	ns
			$C_L = 400$ pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_D = 10\Omega$	$C_L = 100$ pF		17	27	ns
			$C_L = 400$ pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	$R_D = 10\Omega$	$C_L = 100$ pF		18	25	ns
			$C_L = 400$ pF		26	35	ns

AC Test Circuits and Switching Time Waveforms


5V
12V
15V
V_{CC1}
V_{CC2}
V_{CC3}
PULSE GENERATOR (NOTE 1)
SELECT INPUT
IN
OUT
10
(INTERNAL ON DS1644/DS3644)
C_L (NOTE 2)
GND
REFRESH INPUT = 2.4V
ALL OTHER INPUTS = 0V

TL/F/5876-3

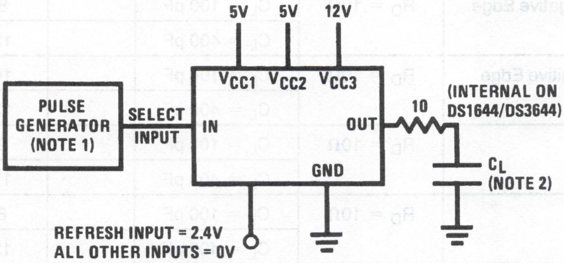
FIGURE 1. 12V Operation


3V
INPUT
0V
1.5V
1.5V
t_{S+-}
t_{S-+}
V_{OH}
$V_{CC2}-2V$
$V_{CC2}-2V$
OUTPUT
+2V
+2V
V_{OL}
t_F
t_R
t_{pd0}
t_{pd1}

TL/F/5876-4

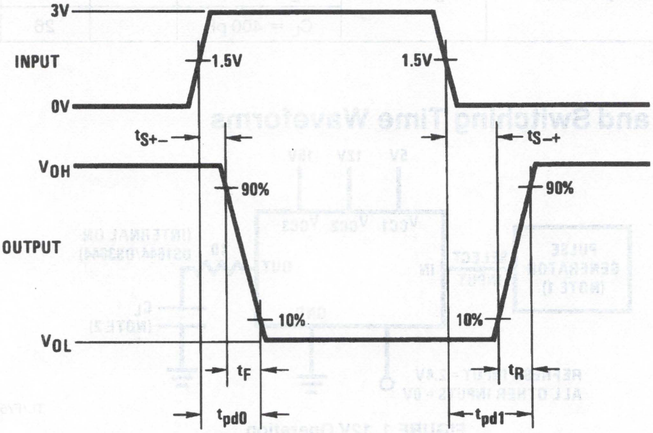
FIGURE 2. 12V Operation

AC Test Circuits and Switching Time Waveforms (Continued)


5V
5V
12V
V_{CC1}
V_{CC2}
V_{CC3}
PULSE GENERATOR (NOTE 1)
SELECT INPUT
IN
OUT
10
(INTERNAL ON DS1644/DS3644)
GND
C_L (NOTE 2)
REFRESH INPUT = 2.4V
ALL OTHER INPUTS = 0V

TL/F/5876–5

FIGURE 3. 5V Operation


3V
INPUT
1.5V
1.5V
0V
t_{S+-}
t_{S-+}
V_{OH}
90%
90%
OUTPUT
10%
10%
V_{OL}
t_F
t_R
t_{pd0}
t_{pd1}

TL/F/5876–6

FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Truth Table

Input					Output
Enable 1	Enable 2	Select Input	Clock Input	Refresh Input	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

National Semiconductor

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

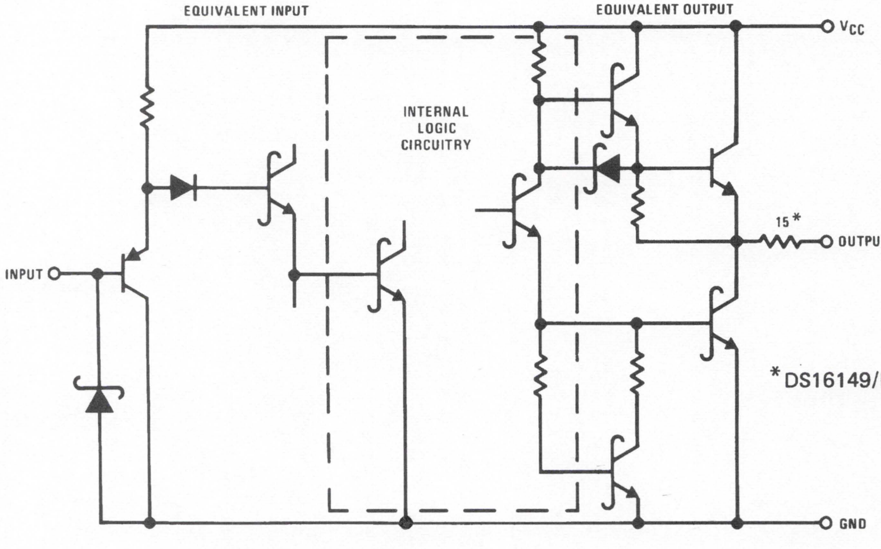
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS16149/DS36149 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS16149/DS36149 only.

TL/F/7553-1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 m/W°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS16149, DS16179	−55	+125	°C
DS36149, DS36179	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN}(1)$	Logical "1" Input Voltage			2.0			V
$V_{IN}(0)$	Logical "0" Input Voltage					0.8	V
$I_{IN}(1)$	Logical "1" Input Current	$V_{CC} = 5.5V, V_{IN} = 5.5V$			0.1	40	μA
$I_{IN}(0)$	Logical "0" Input Current	$V_{CC} = 5.5V, V_{IN} = 0.5V$			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN} = -18\ mA$			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OH} = -10\ \mu A$	DS16149/DS16179	3.4	4.3		V
			DS36149/DS36179	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OL} = 10\ \mu A$	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OH} = -1.0\ mA$	DS16149	2.4	3.5		V
			DS16179	2.5	3.5		V
			DS36149	2.6	3.5		V
			DS36179	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OL} = 20\ mA$	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 0V$, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 4.5V$, (Note 4)			150		mA
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$	Disable Inputs = 0V All Other Inputs = 3V		33	60	mA
			All Inputs = 0V	14		20	mA

Switching Characteristics ($V_{CC} = 5V, T_A = 25°C$) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	*(Figure 1)*	$C_L = 50\ pF$		4.5	7	ns
			$C_L = 500\ pF$		7.5	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	*(Figure 1)*	$C_L = 50\ pF$		5	8	ns
			$C_L = 500\ pF$		8	13	ns
t_F	Fall Time	*(Figure 1)*	$C_L = 50\ pF$		5	8	ns
			$C_L = 500\ pF$		22	35	ns

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	ns
t_{LH}	Delay from Disable Input to Logical "1"	R_L = 2 kΩ to Gnd, C_L = 50 pF, (*Figure 2*)			15	22	ns
t_{HL}	Delay from Disable Input to Logical "0"	R_L = 2 kΩ to V_{CC}, C_L = 50 pF, (*Figure 3*)			11	18	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

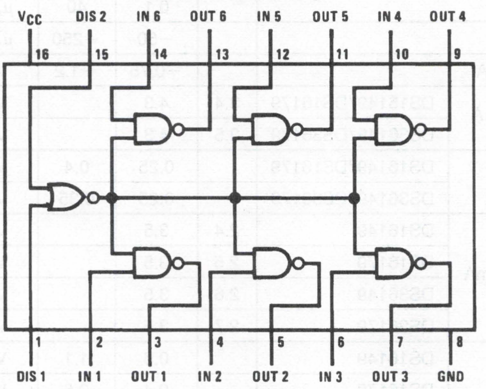
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

Connection Diagram

Dual In-Line Package


VCC
DIS 2
IN 6
OUT 6
IN 5
OUT 5
IN 4
OUT 4
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
DIS 1
IN 1
OUT 1
IN 2
OUT 2
IN 3
OUT 3
GND

TL/F/7553-2

Top View

Order Number DS16149J, DS36149J, DS16179J, DS36179J, DS36149N or DS36179N
See NS Package Number J16A or N16A

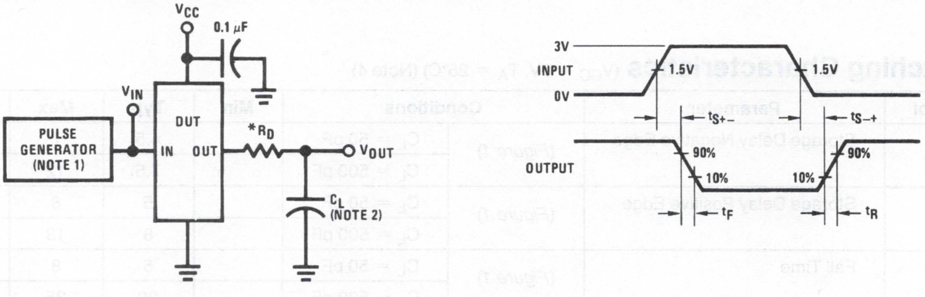
Truth Table

Disable Input		Input	Output
DIS 1	DIS2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

AC Test Circuits and Switching Time Waveforms

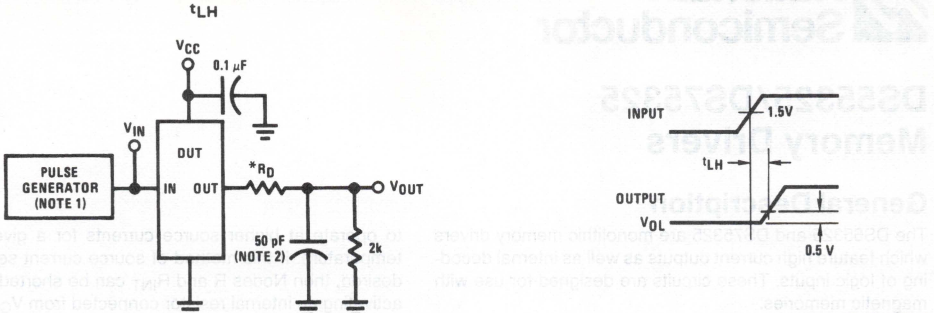
$t_{S\pm}$, $t_{S\pm}$, t_R, t_F


VCC
0.1 μF
VIN
PULSE GENERATOR (NOTE 1)
DUT
IN
OUT
*RD
VOUT
CL (NOTE 2)
3V
INPUT
0V
1.5V
1.5V
tS+−
tS−+
OUTPUT
90%
90%
10%
10%
tF
tR

TL/F/7553-3

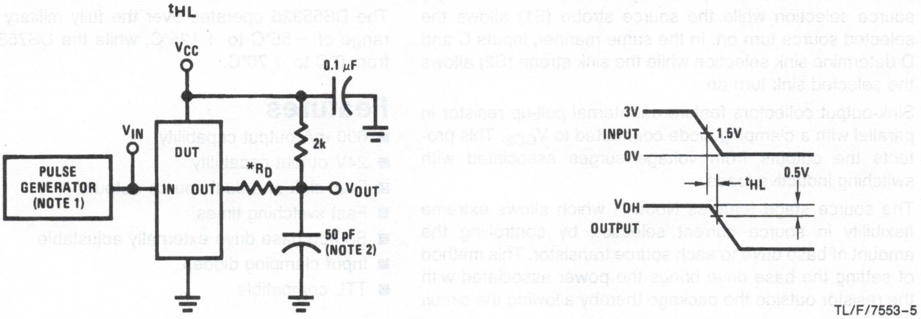
FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)


tLH
VCC
0.1 µF
VIN
PULSE GENERATOR (NOTE 1)
DUT
IN
OUT
*RD
VOUT
50 pF (NOTE 2)
2k
INPUT
1.5V
tLH
OUTPUT
VOL
0.5 V

TL/F/7553-4

FIGURE 2


tHL
VCC
0.1 µF
VIN
2k
DUT
PULSE GENERATOR (NOTE 1)
IN
OUT
*RD
VOUT
50 pF (NOTE 2)
3V
INPUT
1.5V
0V
0.5V
tHL
VOH
OUTPUT

TL/F/7553-5

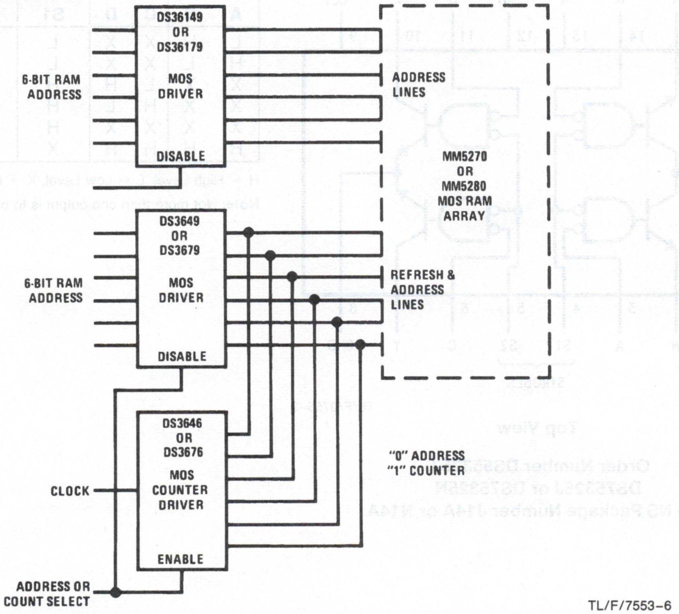
FIGURE 3

*Internal on DS16149 and DS36149

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Typical Applications


DS36149 OR DS36179
6-BIT RAM ADDRESS
MOS DRIVER
DISABLE
ADDRESS LINES
MM5270 OR MM5280 MOS RAM ARRAY
DS3649 OR DS3679
6-BIT RAM ADDRESS
MOS DRIVER
DISABLE
REFRESH & ADDRESS LINES
DS3646 OR DS3676
MOS COUNTER DRIVER
ENABLE
CLOCK
"0" ADDRESS
"1" COUNTER
ADDRESS OR COUNT SELECT

TL/F/7553-6

National Semiconductor

DS55325/DS75325 Memory Drivers

General Description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally, activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with $V_{CC2} = 15V$ or 600 mA with $V_{CC2} = 24V$.

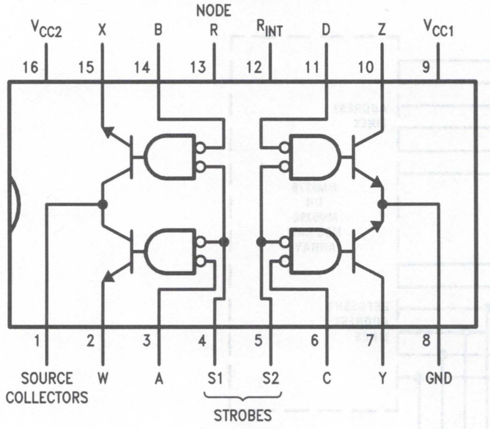
The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS75325 operates from 0°C to +70°C.

Features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- TTL compatible

Connection Diagram

Dual-In-Line Package



TL/F/9755-2

Top View

Order Number DS55325J, DS75325J or DS75325N
See NS Package Number J14A or N14A

Truth Table

Address Inputs				Strobe Inputs		Outputs			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = High Level, L = Low Level, X = Irrelevant

Note: Not more than one output is to be on at any one time.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate Cavity Package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DS55325	−55	+125	°C
DS75325	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	$V_{CC1} = 4.5V$, $V_{CC2} = 24V$, $I_{IN} = -12$ mA $T_A = 25°C$ *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "Off" State Current	$V_{CC1} = 4.5V$, $V_{CC2} = 24V$ *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			$T_A = 25°C$	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	$V_{CC1} = 4.5V$, $V_{CC2} = 24V$, $I_{OUT} = 0$ mA *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	$V_{CC1} = 4.5V$, $V_{CC2} = 15V$, $R_L = 24\Omega$, $I_{SOURCE} \approx -600$ mA *(Figure 3)* (Notes 4 and 6)	Full Range				0.9	V
			$T_A = 25°C$	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	$V_{CC1} = 4.5V$, $V_{CC2} = 15V$, $R_L = 24\Omega$, $I_{SINK} \approx 600$ mA *(Figure 4)* (Notes 4 and 6)	Full Range				0.9	V
			$T_A = 25°C$	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 5.5V$ *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 2.4V$ *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 0.4V$ *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\ OFF}$	Supply Current, All Sources and Sinks "Off"	V_{CC1} 5.5V, $V_{CC2} = 24V$, $T_A = 25°C$ *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current from V_{CC1}, Either Sink "On"	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $I_{SINK} = 50$ mA, $T_A = 25°C$ *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source "On"	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $I_{SOURCE} = -50$ mA $T_A = 25°C$ *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

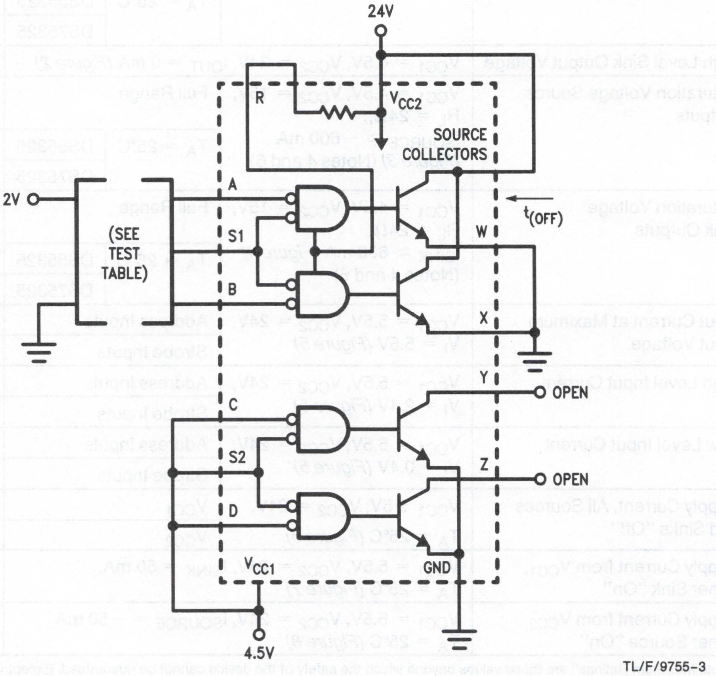
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. $t_W = 200\ \mu s$, duty cycle $\leq 2\%$.

Switching Characteristics $V_{CC1} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 25$ pF	Source Outputs, $V_{CC2} = 20V, R_L = 1\ k\Omega$ *(Figure 10)*		55		ns
			Sink Outputs, $V_{CC2} = 15V, R_L = 24\Omega$ *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 25$ pF	Source Outputs, $V_{CC2} = 20V, R_L = 1\ k\Omega$ *(Figure 10)*		7		ns
			Sink Outputs, $V_{CC2} = 15V, R_L = 24\Omega$ *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*			15	30	ns

DC Test Circuits

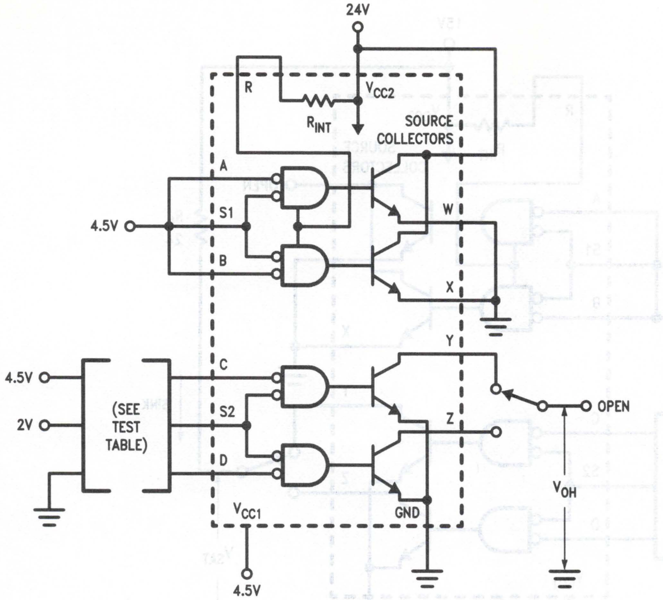

24V
R
V_{CC2}
SOURCE COLLECTORS
2V
A
(SEE TEST TABLE)
S1
B
W
$t_{(OFF)}$
X
Y
OPEN
C
S2
Z
OPEN
D
V_{CC1}
GND
4.5V
TL/F/9755-3

Test Table

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

DC Test Circuits (Continued)

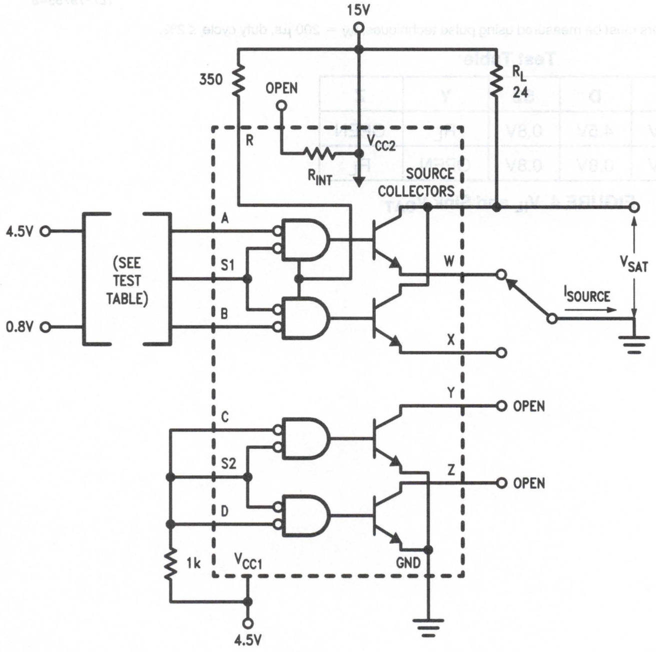

24V
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
A
S1
B
W
X
4.5V
Y
C
S2
D
Z
4.5V
2V
(SEE TEST TABLE)
OPEN
V_{OH}
V_{CC1}
GND
4.5V

Test Table

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

TL/F/9755–4

FIGURE 2. V_{IH} and V_{OH}


15V
350
OPEN
R_L 24
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
4.5V
0.8V
(SEE TEST TABLE)
A
S1
B
W
X
V_{SAT}
I_{SOURCE}
Y
OPEN
C
S2
D
Z
OPEN
1k
V_{CC1}
GND
4.5V

Test Table

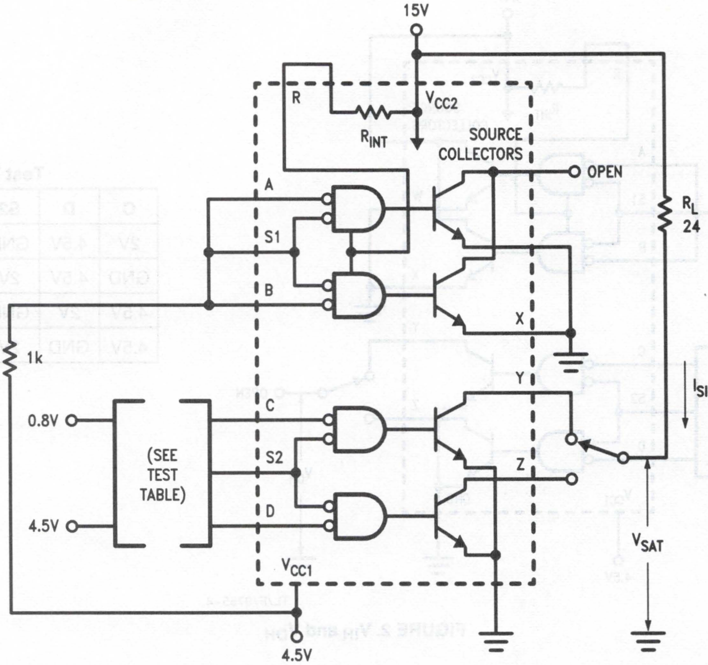
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

TL/F/9755–5

Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, $t_W = 200\ \mu s$, duty cycle $\leq 2\%$.

FIGURE 3. V_{IL} and Source V_{SAT}

DC Test Circuits (Continued)


15V
R
R_{INT}
V_{CC2}
SOURCE COLLECTORS
OPEN
A
S1
B
R_L 24
X
1k
Y
I_{SINK}
C
0.8V
(SEE TEST TABLE)
S2
Z
4.5V
D
V_{SAT}
V_{CC1}
4.5V

TL/F/9755-6

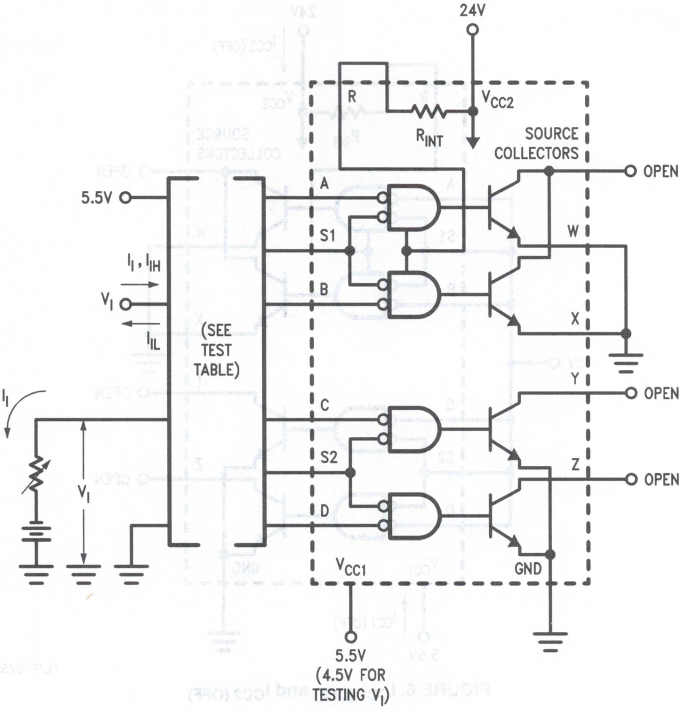
Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, $t_W = 200\ \mu s$, duty cycle $\leq 2\%$.

Test Table

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}

DC Test Circuits (Continued)


24V
R
R_{INT}
V_{CC2}
SOURCE COLLECTORS
OPEN
5.5V
A
S1
W
I_I, I_{IH}
B
V_I
X
(SEE TEST TABLE)
I_{IL}
Y
OPEN
I_I
C
V_I
S2
Z
OPEN
D
V_{CC1}
GND
5.5V (4.5V FOR TESTING V_I)

TL/F/9755-7

Test Tables

I_I, I_{IH}

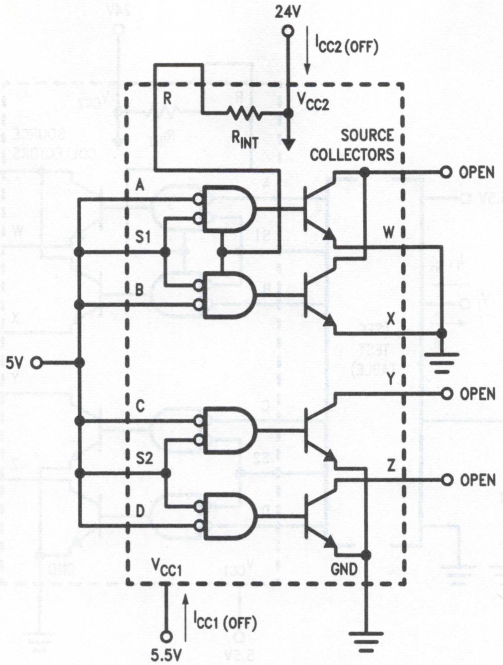
Apply V_I = 5.5V Measure I_I	Ground	Apply 5.5V
Apply V_I = 2.4V Measure I_{IH}		
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

Apply V_I = 0.4V Measure I_{IL}	Apply 5.5V
Apply I_I = −10 mA Measure V_I	
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH} and I_{IL}

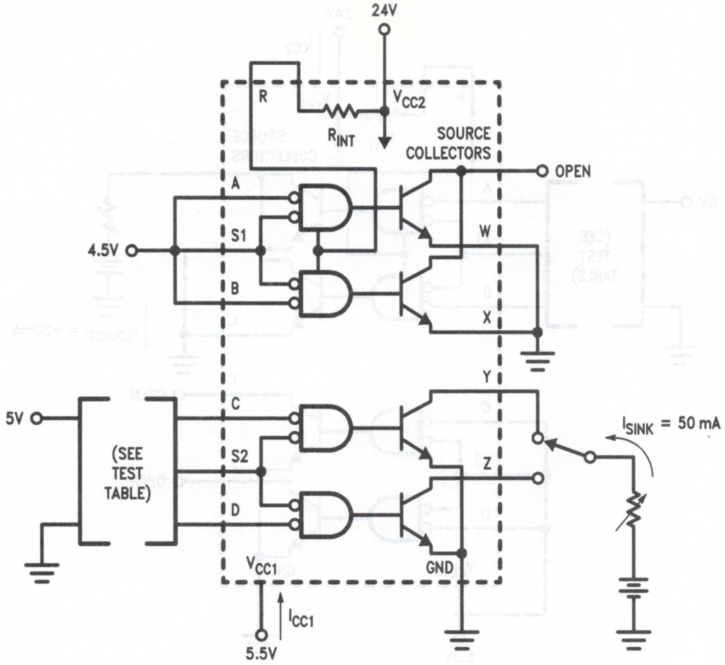
DC Test Circuits (Continued)


24V
$I_{CC2\,(OFF)}$
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
OPEN
A
S1
W
B
X
5V
Y
OPEN
C
S2
Z
OPEN
D
V_{CC1}
GND
$I_{CC1\,(OFF)}$
5.5V

TL/F/9755-8

FIGURE 6. $I_{CC1\,(OFF)}$ and $I_{CC2\,(OFF)}$

DC Test Circuits (Continued)


24V
R
R_INT
V_CC2
SOURCE COLLECTORS
OPEN
A
S1
4.5V
W
B
X
Y
5V
C
(SEE TEST TABLE)
S2
D
I_SINK = 50 mA
Z
V_CC1
GND
I_CC1
5.5V

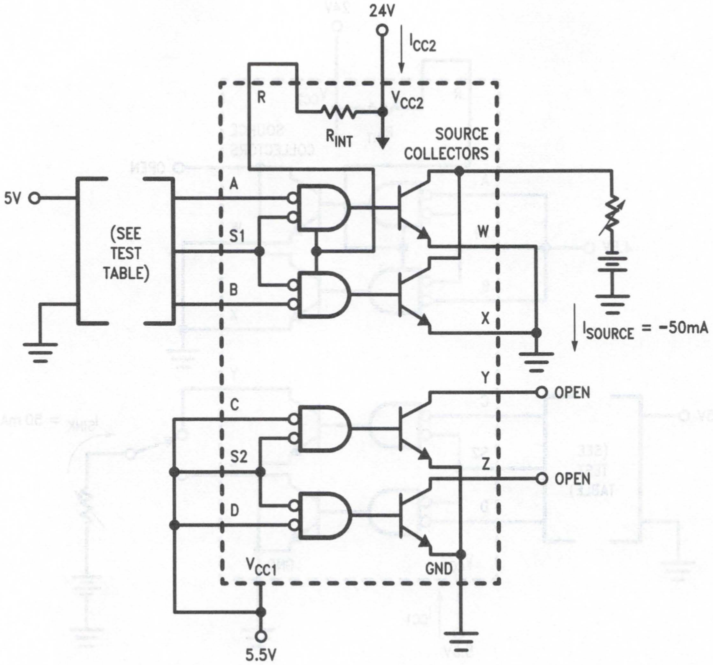
TL/F/9755-9

Test Table

C	D	S2	Y	Z
GND	5V	GND	I_{SINK}	OPEN
5V	GND	GND	OPEN	I_{SINK}

FIGURE 7. I_{CC1}, Either Sink On

DC Test Circuits (Continued)


24V
I_{CC2}
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
5V
(SEE TEST TABLE)
A
S1
B
W
X
I_{SOURCE} = −50mA
Y
OPEN
C
S2
Z
OPEN
D
V_{CC1}
GND
5.5V

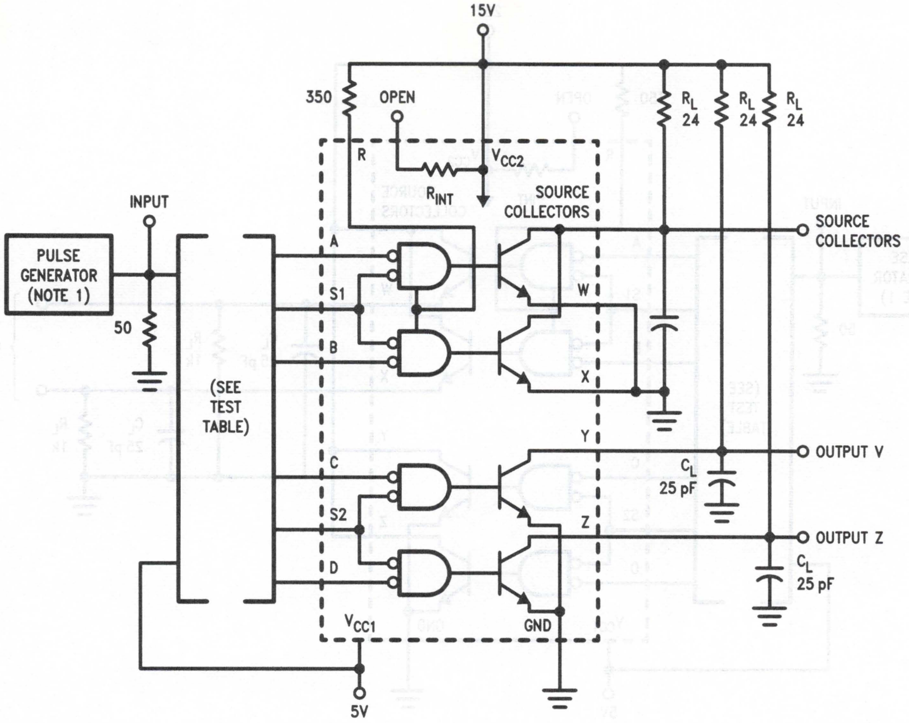
TL/F/9755-10

Test Table

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

DC Test Circuits (Continued)

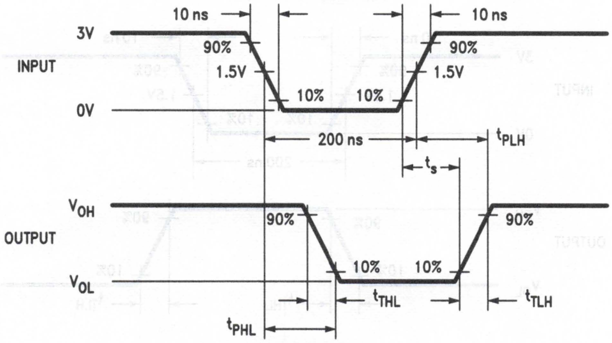

15V
350
OPEN
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
R_L 24
R_L 24
R_L 24
INPUT
PULSE GENERATOR (NOTE 1)
50
(SEE TEST TABLE)
A
S1
B
W
X
Y
C
S2
D
Z
SOURCE COLLECTORS
OUTPUT V
C_L 25 pF
OUTPUT Z
C_L 25 pF
V_{CC1}
GND
5V

TL/F/9755-11

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms


10 ns
10 ns
3V
INPUT
0V
90%
1.5V
10%
10%
90%
1.5V
200 ns
t_{PLH}
t_s
V_{OH}
OUTPUT
V_{OL}
90%
10%
10%
90%
t_{THL}
t_{TLH}
t_{PHL}

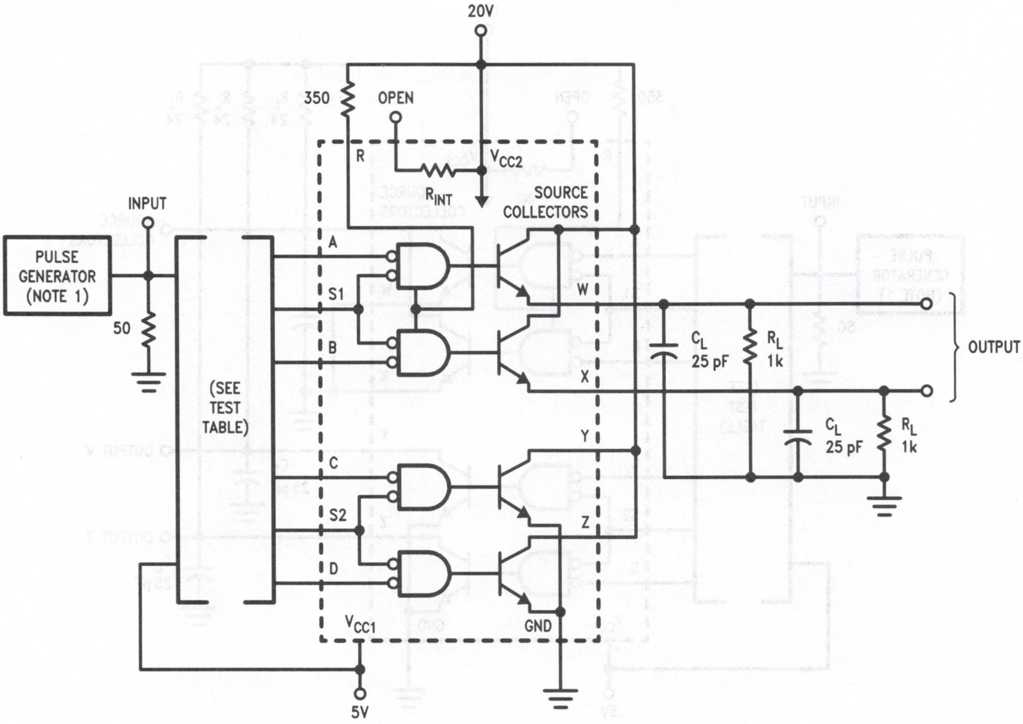
TL/F/9755-12

Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{PLH} and t_{PHL}	Source Collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} and t_S	Sink Output Y	C and S2	A, B, D and S1
	Sink Output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times

DC Test Circuits (Continued)

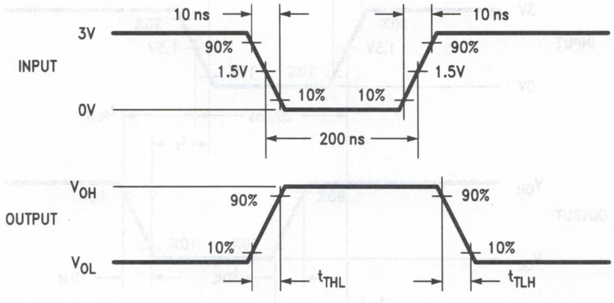

20V
350
OPEN
R
V_{CC2}
R_{INT}
SOURCE COLLECTORS
INPUT
PULSE GENERATOR (NOTE 1)
50
A
S1
B
W
X
(SEE TEST TABLE)
C
S2
D
Y
Z
V_{CC1}
GND
5V
C_L 25 pF
R_L 1k
OUTPUT

TL/F/9755–13

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, duty cycle $\leq$ 1%.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms


10 ns
10 ns
3V
INPUT
0V
90%
1.5V
10%
10%
90%
1.5V
200 ns
V_{OH}
OUTPUT
V_{OL}
90%
10%
90%
10%
t_{THL}
t_{TLH}

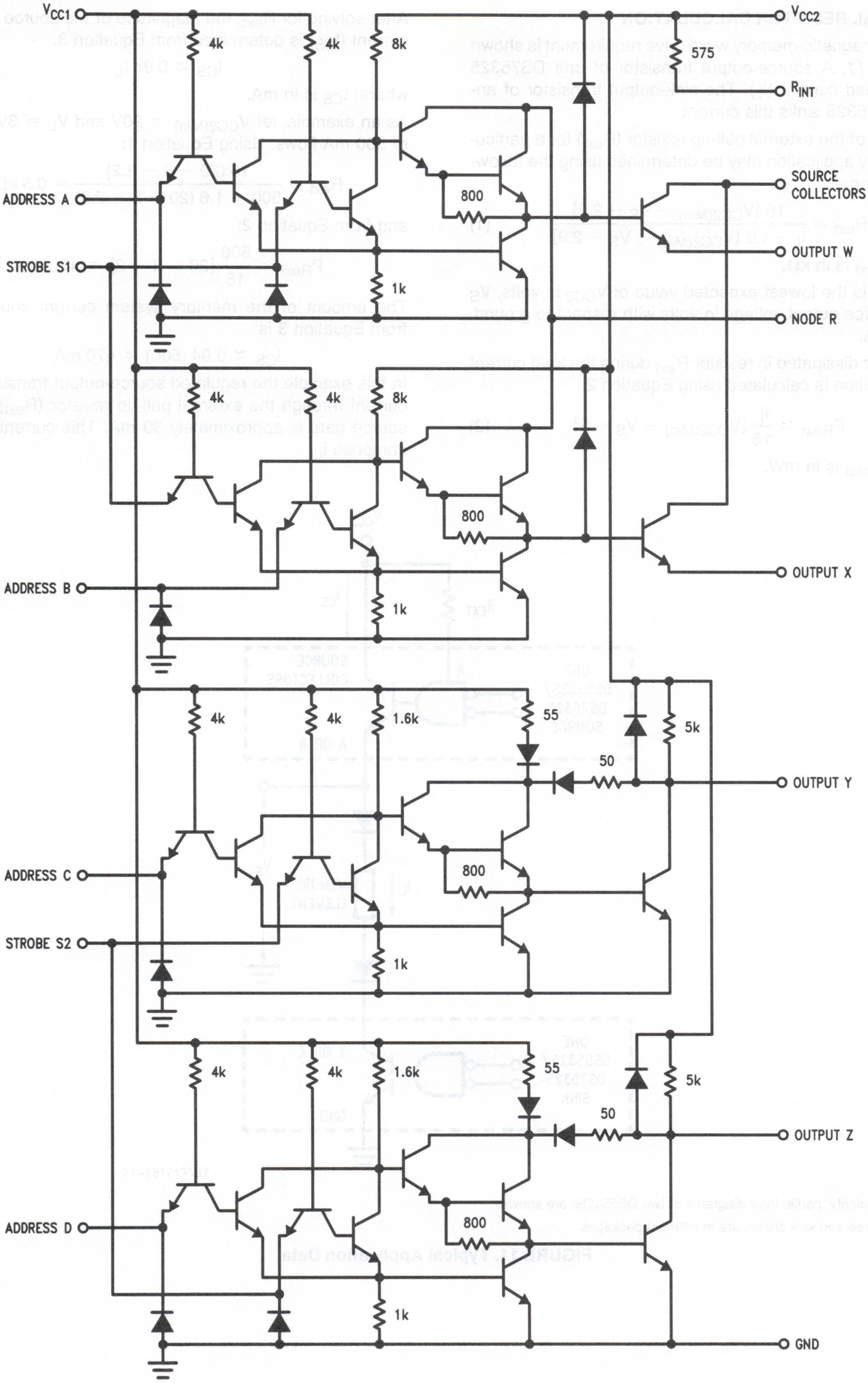
TL/F/9755–14

Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{TLH} and t_{THL}	Source Output W	A and S1	B, C, D and S2
	Source Output X	B and S1	A, C, D and S2

FIGURE 10. Transition Times of Source Outputs

Schematic Diagram


V_CC1
4k
4k
8k
V_CC2
575
R_INT
SOURCE COLLECTORS
ADDRESS A
800
OUTPUT W
STROBE S1
1k
NODE R
4k
4k
8k
800
OUTPUT X
ADDRESS B
1k
4k
4k
1.6k
55
5k
50
OUTPUT Y
ADDRESS C
800
STROBE S2
1k
4k
4k
1.6k
55
5k
50
OUTPUT Z
ADDRESS D
800
1k
GND

TL/F/9755-1

Applications

EXTERNAL RESISTOR CALCULATION

A typical magnetic-memory word drive requirement is shown in *Figure 11*. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(Min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(Min)} - V_S - 2.9]} \qquad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(Min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(Min)} - V_S - 2] \qquad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\,I_L \qquad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(Min)} = 20V$ and $V_L = 3V$ while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ \text{k}\Omega$$

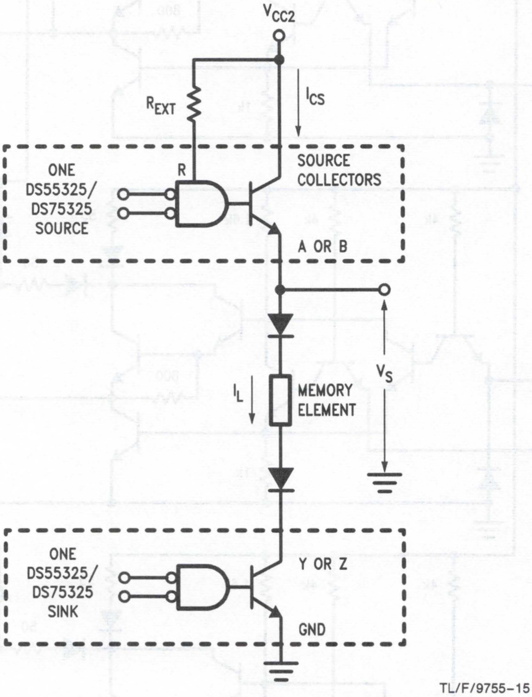
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ \text{mW}$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ \text{mA}$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1: For clarity, partial logic diagrams of two DS55325s are shown.

Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

National Semiconductor

DS75361 Dual TTL-to-MOS Driver

General Description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

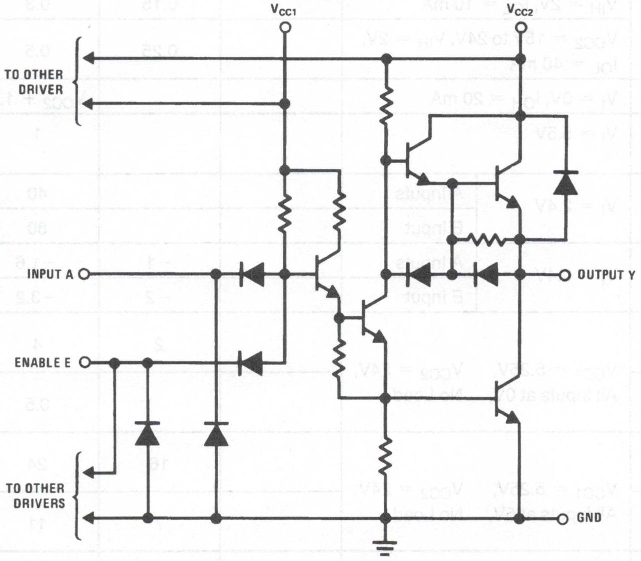
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

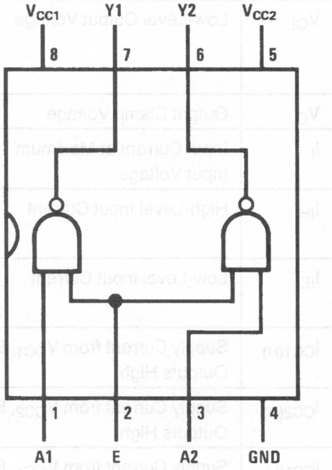
Schematic and Connection Diagrams

(1/2 shown)



TL/F/7557-3

Dual-In-Line Package



TL/F/7557-1

Top View

Order Number DS75361J or DS75361N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Range of V_{CC1} (Note 1)	−0.5 to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature 1/16 inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 inch from Case for 10 Seconds: N or P Package	200°C

*Derate molded package 8.2 mW/° above about 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{IL} = 0.8V, I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{IL} = 0.8V, I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V, I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC2} = 15V$ to $24V, V_{IH} = 2V,$ $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V, I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	$V_{CC1} = 5.25V,$ All Inputs at 0V,	$V_{CC2} = 24V,$ No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	$V_{CC1} = 5.25V,$ All Inputs at 5V,	$V_{CC2} = 24V,$ No Load		16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V,$ All Inputs at 5V,	$V_{CC2} = 24V,$ No Load			0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$.

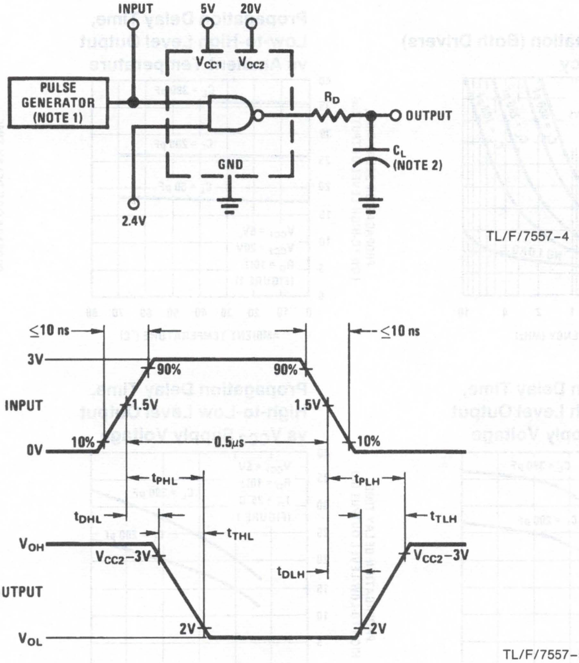
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between the A input of either driver and the common E input.

Switching Characteristics $V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	$C_L = 390$ pF, $R_D = 10\Omega$ *(Figure 1)*		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
tPLH	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

AC Test Circuit and Switching Time Waveforms


INPUT
5V
20V
VCC1
VCC2
PULSE GENERATOR (NOTE 1)
RD
OUTPUT
CL (NOTE 2)
GND
2.4V
TL/F/7557-4
≤10 ns
≤10 ns
3V
90%
90%
INPUT
1.5V
1.5V
10%
10%
0V
0.5μs
tPHL
tPLH
tDHL
tTHL
tTLH
tDLH
VOH
VCC2−3V
VCC2−3V
OUTPUT
VOL
2V
2V
TL/F/7557-5

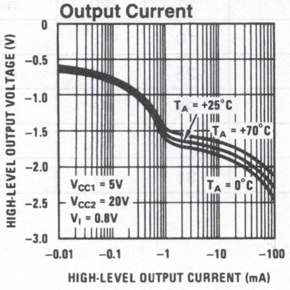
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

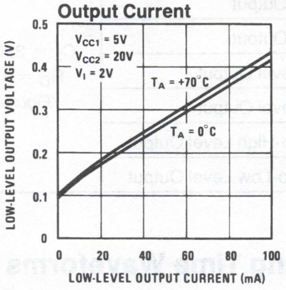
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

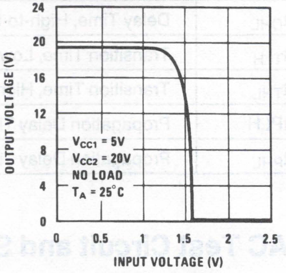
High-Level Output Voltage vs Output Current



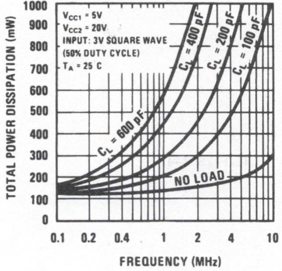
Low-Level Output Voltage vs Output Current



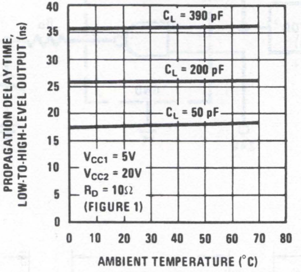
Voltage Transfer Characteristics



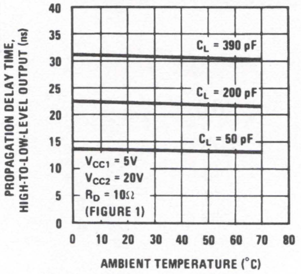
Total Dissipation (Both Drivers) vs Frequency



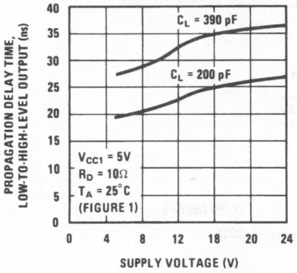
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



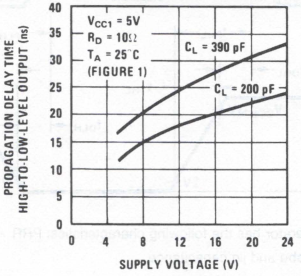
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



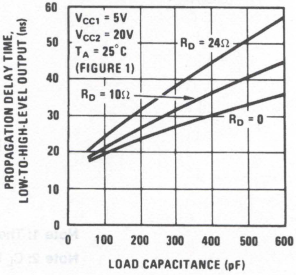
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



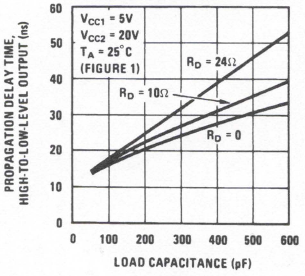
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



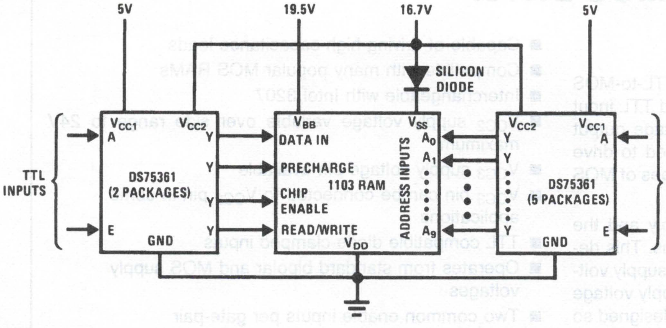
Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



TL/F/7557–2

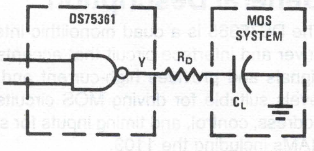
Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.



TL/F/7557–6

FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM



TL/F/7557–7

Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\text{ mA}}{2}\right) + (20V)\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16\text{ mA}}{2}\right) + (20V)\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$$P_{DC(AV)} = 47\text{ mW per channel}$$

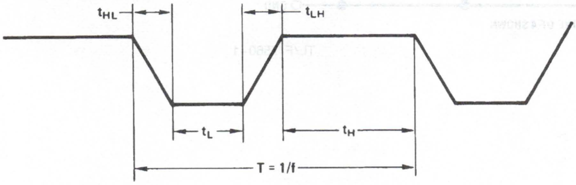
$$P_{C(AV)} \approx (200\text{ pF})(19.2V)^2(2\text{ MHz})$$

$$P_{C(AV)} \approx 148\text{ mW per channel.}$$

For the total device dissipation of the two channels:

$$P_{T(AV)} \approx 2(47 + 148)$$

$$P_{T(AV)} \approx 390\text{ mW typical for total package.}$$



TL/F/7557–8

FIGURE 4. Output Voltage Waveform

National Semiconductor

PRELIMINARY

DS75365 Quad TTL-to-MOS Driver

General Description

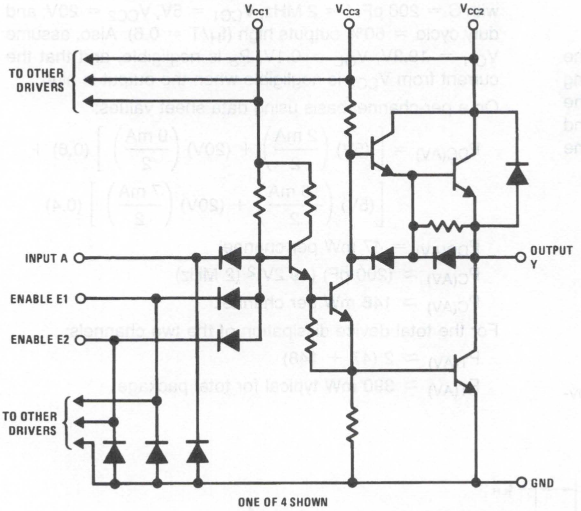
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} to the V_{CC2} pin.

Features

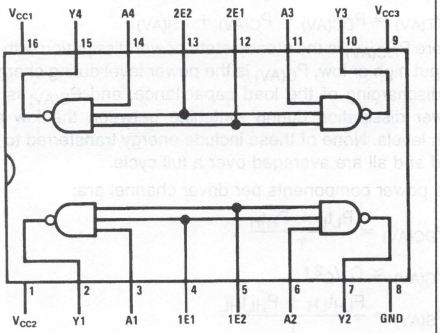
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over side range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



TL/F/7560-1

Dual-In-Line Package



TL/F/7560-2

Top View

Positive Logic: $Y = \overline{A \bullet E1 \bullet E2}$

Order Number DS75365J or DS75365N

See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\ \mu A$		$V_{CC2} - 0.3$	$V_{CC2} - 0.1$		V
		$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 1.2$	$V_{CC2} - 0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to $28V$, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA

Electrical Characteristics (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-By Condition	$V_{CC1} = 0V, V_{CC2} = 24V$ $V_{CC3} = 24V$, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-By Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

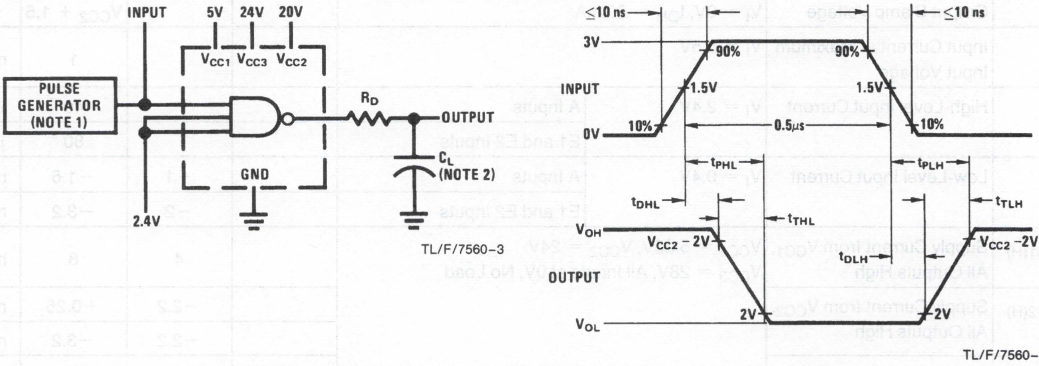
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics $V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	$C_L = 200$ pF $R_D = 24\Omega$ *(Figure 1)*		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms



TL/F/7560-3

TL/F/7560-4

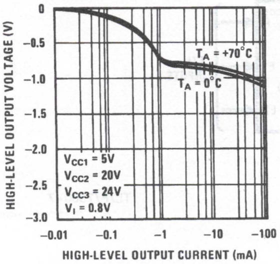
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} = 58\Omega$.

Note 2: C_L includes probe and jig capacitance.

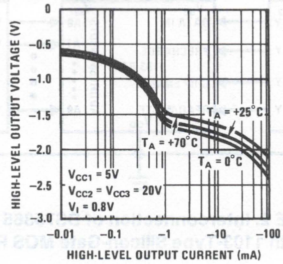
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

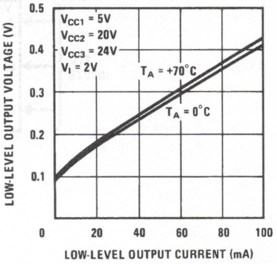
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

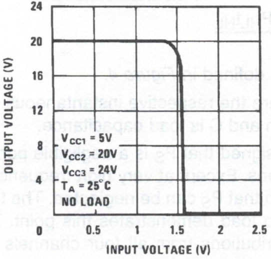


Low-Level Output Voltage Output Current

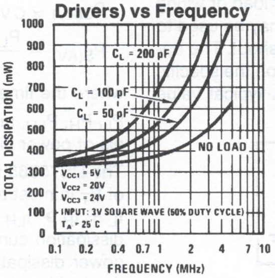


TL/F/7560–5

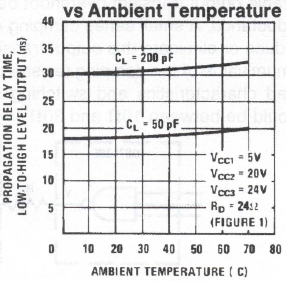
Voltage Transfer Characteristics



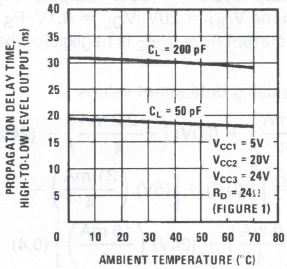
Total Dissipation (All Four Drivers) vs Frequency



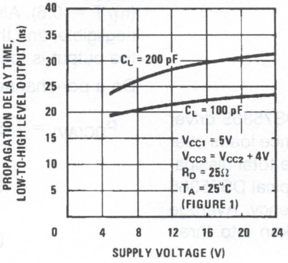
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



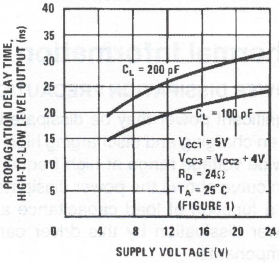
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



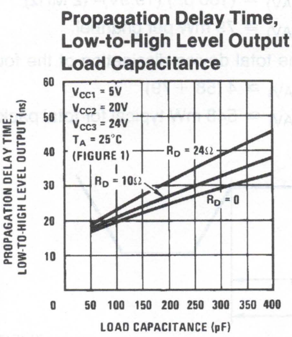
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



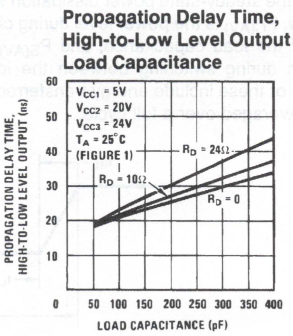
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



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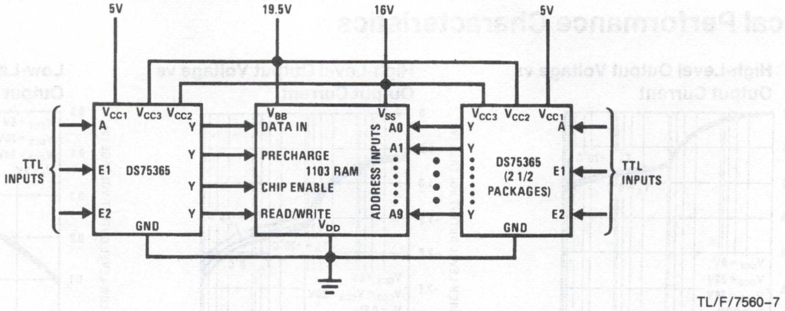
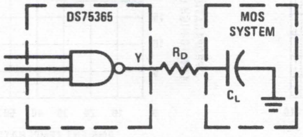


FIGURE 2. Interconnection of DS75365 Devices with 1103-Type Silicon-Gate MOS RAM

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω (*Figure 3*).



Note: $R_D \cong$ 10Ω to 30Ω (Optional)

TL/F/7560-8

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \cong C\,V_C{}^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \cong (100\text{ pF})(19.9V)^2(2\text{ MHz})$

$P_{C(AV)} \cong$ 79 mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \cong 4\,(58 + 79)$

$P_{T(AV)} \cong$ 548 mW typical for total package.

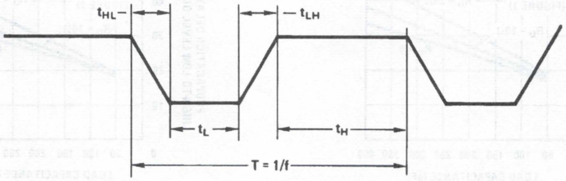


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FIGURE 4. Output Voltage Waveform

National Semiconductor

DS9643/μA9643 Dual TTL to MOS/CCD Driver

General Description

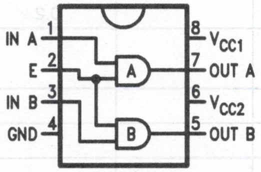
The DS9643/μA9643 is a dual positive logic "AND" TTL-to-MOS driver. The DS9643/μA9643 is a functional replacement for the SN75322 with one important exception: the two external PNP transistors are no longer needed for operation. The DS9643/μA9643 is also a functional replacement for the 75363 with the important exception that the V_{CC3} supply is not needed. The lead connections normally used for the external PNP transistors are purposely not internally connected to the DS9643/μA9643.

Features

- Satisfies CCD memory and delay line requirements
- Dual positive logic TTL to MOS driver
- Operates from standard bipolar and MOS supply voltages
- High speed switching
- TTL and DTL compatible inputs
- Separate drivers address inputs with common strobe
- V_{OH} and V_{OL} compatible with popular MOS RAMs
- Does not require external PNP transistors or V_{CC3}
- V_{OH} minimum is $V_{CC2} - 0.5V$

Connection Diagram

8-Lead DIP



TL/F/9646–1

Top View

Order Number DS9643N/μA9643TC
See NS Package Number N08E

Truth Table

Input	Enable	Output
L	L	L
L	H	L
H	L	L
H	H	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Molded Package	930 mW
Supply Voltage	
Range of V_{CC1}	−0.5V to +7.0V
Range of V_{CC2}	−0.5V to +15V
Input Voltage	5.5V

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC1})	4.75	5.0	5.25	V
Supply Voltage (V_{CC2})	11.4	12	12.6	V
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

over recommended operating temperatures and V_{CC1}, V_{CC2} ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -400\ \mu A$		$V_{CC2} - 0.5$	$V_{CC2} - 0.2$		V
V_{OL}	Output Voltage LOW	$I_{OL} = 10$ mA			0.4	0.5	V
		$I_{OL} = 1.0$ mA			0.2	0.3	
I_I	Input Current at Maximum Input Voltage	$V_{CC1} = 5.25V$, $V_{CC2} = 11.4V$ $V_I = 5.25V$				0.1	mA
I_{IH}	Input Current HIGH	$V_I = 2.4V$	A Inputs			40	μA
			E Inputs			80	
I_{IL}	Input Current LOW	$V_I = 0.4V$	A Inputs			−0.5	mA
			E Inputs			−1.0	
$I_{CC1(L)}$	Supply Current from V_{CC1} All Outputs LOW	$V_{CC1} = 5.25V$, $V_{CC2} = 12.6V$			15	19	mA
$I_{CC2(L)}$	Supply Current from V_{CC2} All Outputs LOW	$V_{CC1} = 5.25V$, $V_{CC2} = 12.6V$			5.5	9.5	mA
$I_{CC1(H)}$	Supply Current from V_{CC1} All Outputs HIGH	$V_{CC1} = 5.25V$, $V_{CC2} = 12.6V$			9.0	13	mA
$I_{CC2(H)}$	Supply Current from V_{CC2} All Outputs HIGH	$V_{CC1} = 5.25V$, $V_{CC2} = 12.6V$			5.5	9.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS9643. All typicals are given for $V_{CC1} = 5V$, $V_{CC2} = 12V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Switching Characteristics $V_{CC1} = 5.0V, V_{CC2} = 12V, T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{DLH}	Delay Time		$C_L = 300$ pF	5.0	9.0	17	ns
t_{DHL}	Delay Time			5.0	9.0	17	ns
t_{TLH}	Rise Time	$R_{SERIES} = 0$	$C_L = 300$ pF	6.0	11	17	ns
t_{THL}	Fall Time			6.0	11	17	ns
t_{TLH}	Rise Time	$R_{SERIES} = 10\Omega$	$C_L = 300$ pF	8.0	14	20	ns
t_{THL}	Fall Time			8.0	14	20	ns
$t_{PLHA}-$ t_{PLHB} $t_{PHLA}-$ t_{PHLB}	Skew between Outputs A and B				0.5		ns

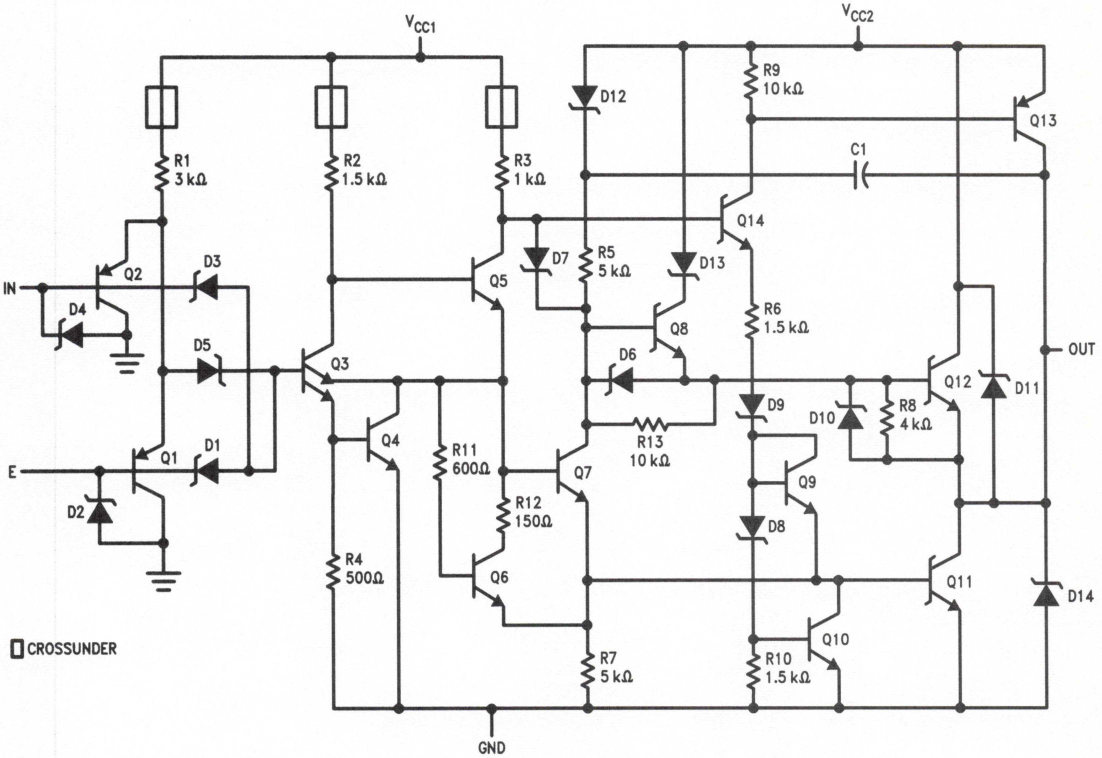

VCC1
VCC2
R1 3 kΩ
R2 1.5 kΩ
R3 1 kΩ
R4 500Ω
R5 5 kΩ
R6 1.5 kΩ
R7 5 kΩ
R8 4 kΩ
R9 10 kΩ
R10 1.5 kΩ
R11 600Ω
R12 150Ω
R13 10 kΩ
C1
IN
E
OUT
GND
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
CROSSUNDER

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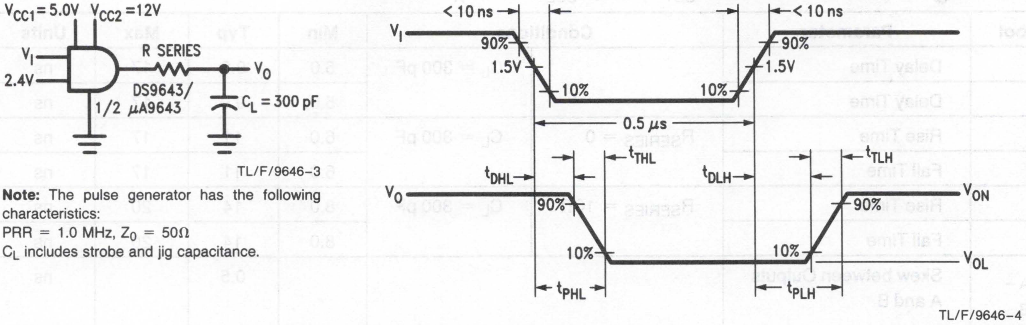
FIGURE 1. Equivalent Circuit (½ of Circuit)


V_{CC1} = 5.0V
V_{CC2} = 12V
V_I
2.4V
R SERIES
V_O
DS9643/
1/2 μA9643
C_L = 300 pF
TL/F/9646-3
< 10 ns
< 10 ns
V_I
90%
1.5V
10%
10%
1.5V
90%
0.5 μs
t_{DHL}
t_{THL}
t_{DLH}
t_{TLH}
V_O
90%
10%
10%
90%
V_{ON}
V_{OL}
t_{PHL}
t_{PLH}
TL/F/9646-4

Note: The pulse generator has the following characteristics:
PRR = 1.0 MHz, Z_0 = 50Ω
C_L includes strobe and jig capacitance.

FIGURE 2. AC Test Circuit and Waveforms

Applying Modern Clock Drivers to MOS Memories

National Semiconductor
Application Note 76
B. Siegel
M. Scott

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input waveforms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAMs (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage gold doped process utilizing a collector sinker to minimize $V_{CE\ SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		15	ns
t_{OFF}	$C_{IN} = 0.0022\ \mu F$, $R_{IN} = 0\Omega$	30	ns
t_r	$C_L = 0.0001\ \mu F$, $R0 = 50\Omega$	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^- = 0V$, $I_{OUT} = -1\ mA$	$V^+ - 0.7$	V
Negative Output Voltage Swing	$I_{IN} = 10\ mA$, $I_{OUT} = 1\ mA$	$V^- + 1.0$	V
On Supply Current (V^+)	$I_{IN} = 10\ mA$	17	mA

TABLE II. DS0026 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		7.5	ns
t_{OFF}	$C_{IN} = 0.001\ \mu F$, $R_{IN} = 0\Omega$	7.5	ns
t_r	$R0 = 50\Omega$, $C_L = 1000\ pF$	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^- = 0V$, $I_{OUT} = -1\ mA$	$V^+ - 0.7$	V
Negative Output Voltage Swing	$I_{IN} = 10\ mA$, $I_{OUT} = 1\ mA$	$V^- + 0.5$	V
On Supply Current (V^+)	$I_{IN} = 10\ mA$	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent—derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \tag{1}$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \tag{2}$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

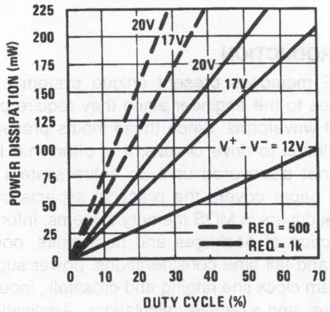
Req = Equivalent device resistance in the "ON" state

$= V^+ - V^- / I_{S(ON)}$ (3)

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time} + \text{"OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.



TL/F/7322-1

FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \tag{4}$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

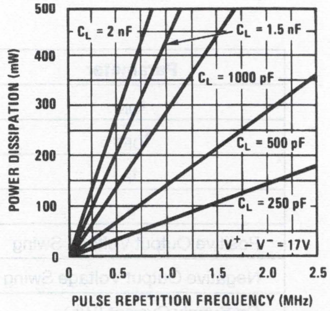


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FIGURE 2. P_{AC} vs PRF

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n\,(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \tag{5}$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$C_L \leq$ 1340 pF (each driver)

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or approximately 20 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2* and *AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver; and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise".

Power Supply Decoupling

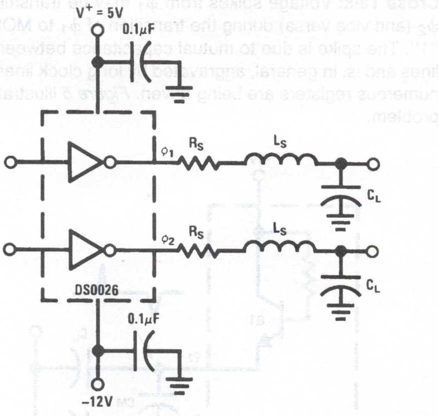
Although power supply decoupling is a wide spread and accepted practice, the question often rises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1 μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long or has significant dc resistance, the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3*. In this instance, a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$



TL/F/7322-3

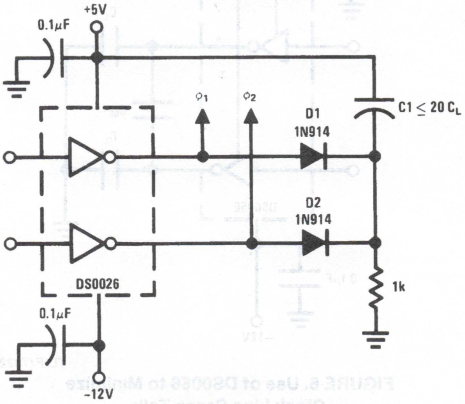
FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S\ C_L \qquad (7)$$

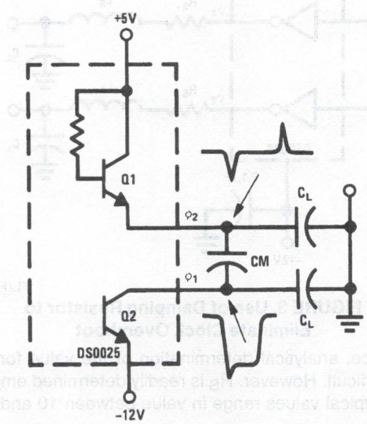
One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2\ fC_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.



TL/F/7322-4

FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

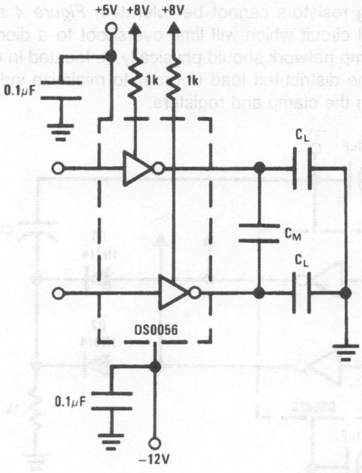


TL/F/7322-5

FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.



TL/F/7322-6

FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

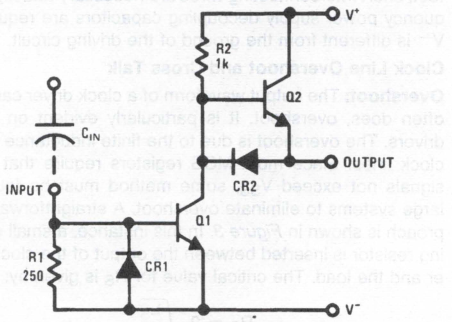
REFERENCES

1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.
2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.
3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.
4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.
5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.
6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.
7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.
8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure 7*. With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V+ supply.



TL/F/7322-7

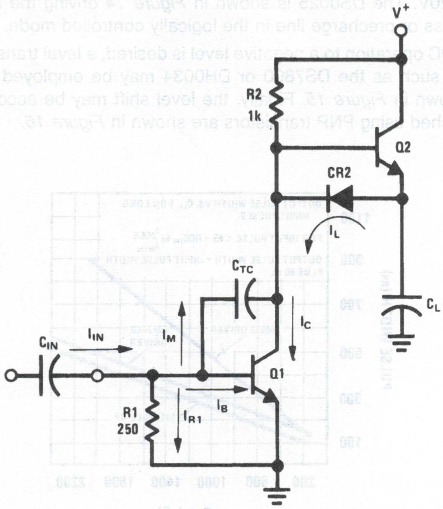
FIGURE 7. DS0025 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure 8*, the input current must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:



TL/F/7322-8

FIGURE 8. Rise Time Model for the DS0025

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M \gg I_{R1} \text{ and } I_B \gg I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B\, h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L\frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, and AI-3 yields:

$$\frac{\Delta V}{\Delta t}\left[C_L + C_{TC}\left(h_{FEQ1} + 1\right)\right] = h_{FEQ1}\, I_{IN} \qquad \text{(AI-4)}$$

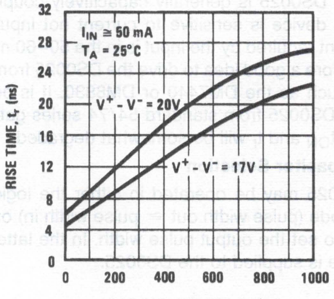
or

$$t_r \cong \frac{\left[C_L + \left(h_{FEQ1} + 1\right)C_{TC}\right]\Delta V}{h_{FEQ1}\, I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 pF respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0\text{V}$, $V^- = -12\text{V}$. *Figure 9* gives rise time for various values of C_L.

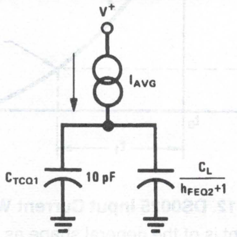


TL/F/7322-9

FIGURE 9. Rise Time vs C_L for the DS0025

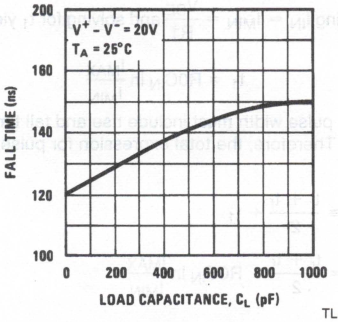
Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of *Figure 10*. In actual practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure 11* shows t_f as function of C_L.



TL/F/7322-10

FIGURE 10. Fall Time Equivalent Circuit



TL/F/7322-11

FIGURE 11. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

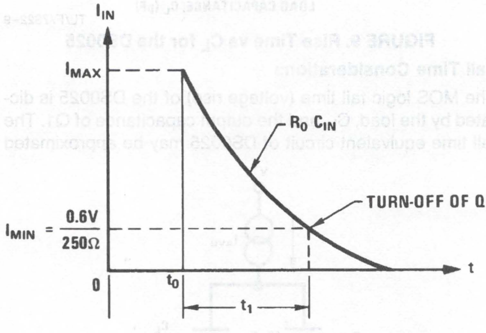
$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \qquad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.



TL/F/7322–12

FIGURE 12. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure 12.* I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below $V_{BE}/R1$ or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0\,C_{IN}} \qquad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)\ (2200\text{ pF}) \ln$$

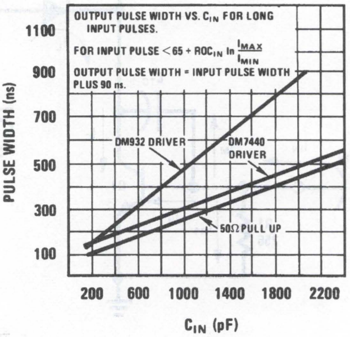
$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure 13.* For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

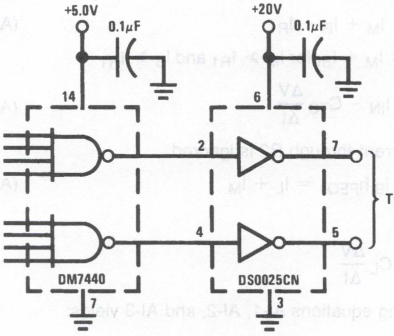
The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure 14* driving the address or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DH0034 may be employed as shown in *Figure 15.* Finally, the level shift may be accomplished using PNP transistors are shown in *Figure 16.*



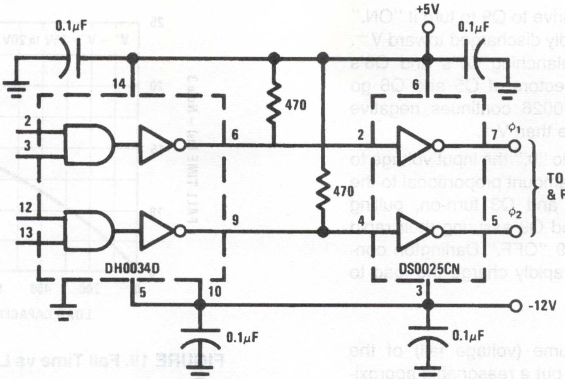
TL/F/7322–13

FIGURE 13. Output PW Controlled by C_{IN}



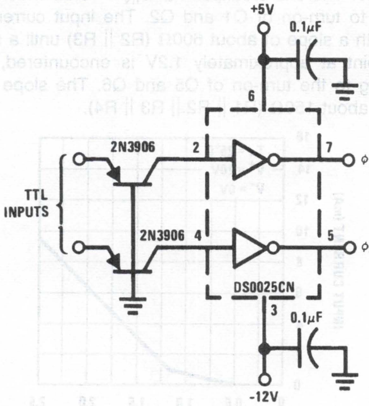
TL/F/7322–14

FIGURE 14. DC Coupled DS0025 Driving 1103 RAM


0.1μF
+5V
0.1μF
14
470
6
2
3
6
2
7
ϕ_1
470
TO MOS SHIFT & REGISTERS
12
13
9
4
5
ϕ_2
DH0034D
DS0025CN
5
10
3
-12V
0.1μF
0.1μF

TL/F/7322-15

FIGURE 15. DC Coupled Clock Driver Using DH0034


+5V
0.1μF
6
2N3906
2
7
ϕ_1
TTL INPUTS
2N3906
4
5
ϕ_2
DS0025CN
3
0.1μF
-12V

TL/F/7322-16

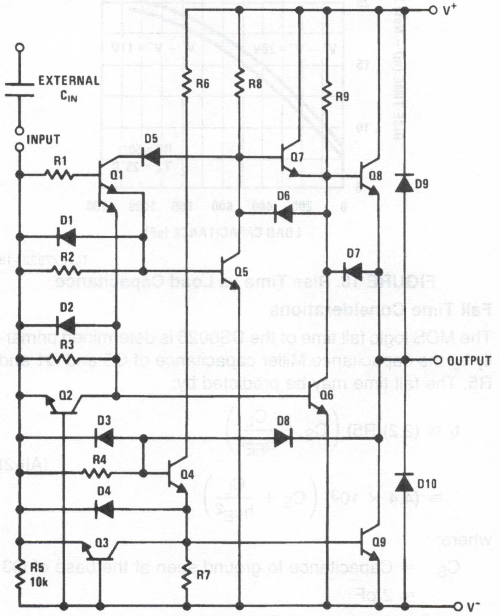
FIGURE 16. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure 17.* The device is typically AC coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q4, Q5, and Q6 are "OFF" allowing Q7 and Q8 to come "ON." R9 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q5 and Q6 turning them "ON." Simultaneously, Q7 and Q8 are snapped "OFF." As the input voltage rises (to about 1.2V), Q1 and Q4 turn-on. Multiple emitter transistor Q1 provides additional base drive to Q5 and Q6 assuring their complete and rapid turn-on. Since Q7 and Q8 were rapidly turned "OFF" minimal power supply current spiking will occur when Q9 comes "ON."


V+
EXTERNAL C_{IN}
R6
R8
R9
INPUT
D5
R1
Q1
Q7
Q8
D9
D6
D1
R2
D7
Q5
D2
R3
OUTPUT
Q2
Q6
D3
D8
R4
Q4
D10
D4
Q3
R5 10k
R7
Q9
V−

TL/F/7322-17

FIGURE 17. DS0026 Schematic (One-Half Circuit)

Q4 now provides sufficient base drive to Q9 to turn it "ON." The load capacitance is then rapidly discharged toward V−. Diodes D6 and D7 prevent avalanching Q7's and Q8's base-emitter junction as the collectors of Q5 and Q6 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V−.

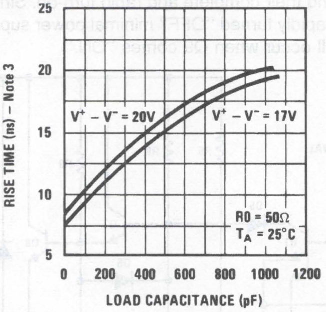
When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q2 and Q3 turn-on, pulling stored base charge out of Q4 and Q9 assuring their rapid turn-off. With Q1, Q5, Q6 and Q9 "OFF," Darlington connected Q7 and Q8 turn-on and rapidly charge the load to within a V_{BE} of V+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\, \Delta V \qquad \text{(AII-1)}$$

For $C_L = 1000$ pF, $V^+ = 5.0V$, $V^- = -12V$, $t_r \cong 21$ ns. *Figure 18* shows DS0026 rise times vs C_L.



TL/F/7322–18

FIGURE 18. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right)$$

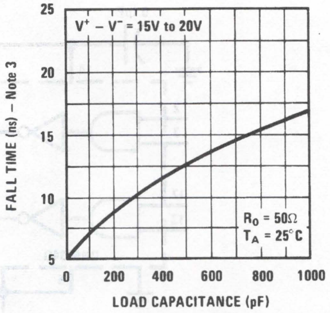
$$\cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3 = 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)(h_{FEQ4} + 1) \cong 500$

For the values given and $C_L = 1000$ pF, $t_f \cong 17.5$ ns. *Figure 19.* gives t_f for various values of C_L.

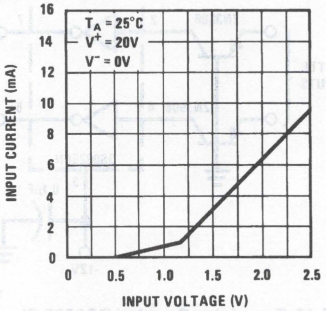


TL/F/7322–19

FIGURE 19. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure 20.* There is breakpoint at $V_{IN} \cong 0.6V$ which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).



TL/F/7322–20

FIGURE 20. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

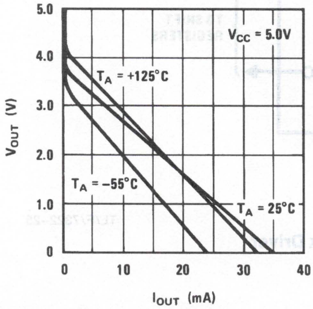
$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I''\,MIN} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R0 \ln \dfrac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure 21* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega) \ln \dfrac{20 \text{ mA}}{1 \text{ mA}}} = 560 \text{ pF}$$

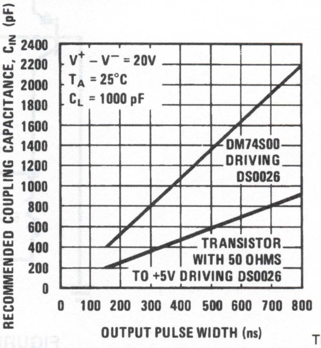


TL/F/7322-21

FIGURE 21. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure 22.*

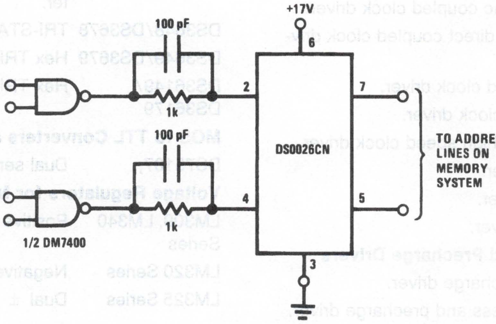


TL/F/7322-22

FIGURE 22. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

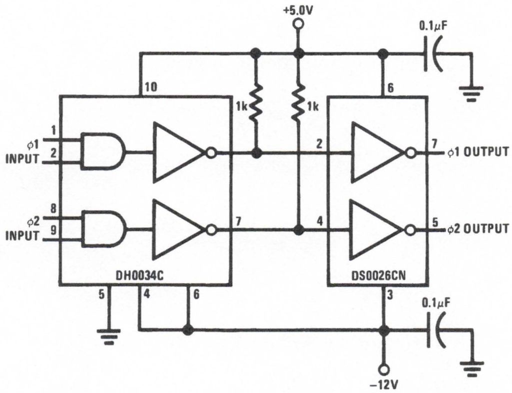
The DS0026 may be applied in direct coupled applications. *Figure 23* shows the device driving address or pre-charge lines on an MM1103 RAM.


+17V
6
100 pF
1k
2
100 pF
1k
4
DS0026CN
7
5
3
TO ADDRESS LINES ON MEMORY SYSTEM
1/2 DM7400

TL/F/7322-23

FIGURE 23. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuits of *Figure 24* or *25* are recommended.


+5.0V
0.1µF
10
6
1k
1k
φ1 INPUT
1
2
φ2 INPUT
8
9
7
2
4
7
φ1 OUTPUT
5
φ2 OUTPUT
DH0034C
DS0026CN
5
4
6
3
0.1µF
−12V

TL/F/7322-24

FIGURE 24. Transistor Coupled MOS Clock Driver

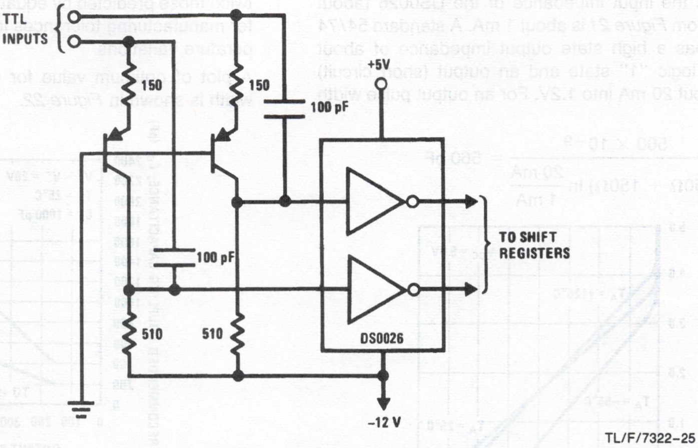


FIGURE 25. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025C	Low cost, two phase clock driver.
DS0026C	Low cost, two phase, high speed clock driver.
DS3674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS RAM Memory Address and Precharge Drivers

DS0025C	Dual address and precharge driver.
DS0026C	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS8800	Dual TTL to negative level converter.
DS88L12	Active pull-up TTL to positive high level MOS converter gates.
DS3647A	Quad TRI-STATE® MOS driver I/O register.
DS3648/DS3678	TRI-STATE MOS driver multiplexer.
DS3649/DS3679	Hex TRI-STATE MOS driver.
DS36149/DS36179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS75107,	Dual sense amp for MM1103 1k MOS

Voltage Regulators for MOS Systems

LM309, LM340 Series	Positive regulators.
LM320 Series	Negative regulators.
LM325 Series	Dual ± regulators.

Section 6

Microprocessor Support

Section 6 Contents

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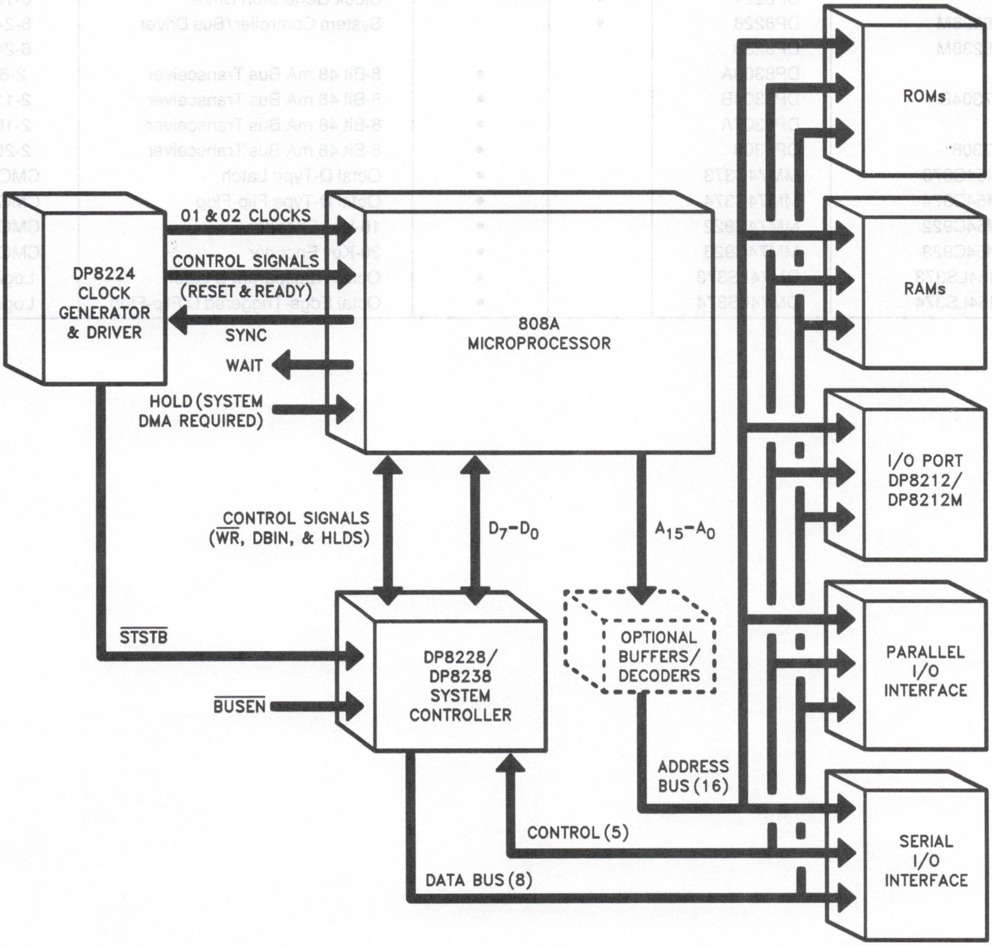
Microprocessor Support

National offers a selection of high quality circuits designed specifically to interface with, and support, the very popular 8-bit 8080A microprocessor. National's family of 8080A support circuits includes clock/generator driver, system controller, I/O port and databus transceivers, all of which make it easy to add microprocessor capability to any system design. For further information on these devices, refer to the enclosed selection guide.

National's 8080A Support Circuits


DP8224
CLOCK
GENERATOR
& DRIVER
01 & 02 CLOCKS
CONTROL SIGNALS
(RESET & READY)
SYNC
WAIT
HOLD (SYSTEM
DMA REQUIRED)
808A
MICROPROCESSOR
CONTROL SIGNALS
(WR, DBIN, & HLDS)
D_7-D_0
$A_{15}-A_0$
STSTB
BUSEN
DP8228/
DP8238
SYSTEM
CONTROLLER
OPTIONAL
BUFFERS/
DECODERS
ADDRESS
BUS (16)
CONTROL (5)
DATA BUS (8)
ROMs
RAMs
I/O PORT
DP8212/
DP8212M
PARALLEL
I/O
INTERFACE
SERIAL
I/O
INTERFACE

TL/XX/0104–1

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Microprocessor Support Circuits

Temperature Range		8080 CPU	General Purpose	Description	Page Number
−55°C to +125°C	0°C to +70°C				
DP8212M	DP8212	•	•	8-Bit I/O Port	6-5
DP8216M	DP8216	•	•	4-Bit Parallel Receiver/Driver	6-13
DP8226M	DP8226				6-13
	DP8224	•		Clock Generator/Driver	6-18
DP8228M	DP8228	•		System Controller/Bus Driver	6-24
DP8238M	DP8238				6-24
	DP8303A		•	8-Bit 48 mA Bus Transceiver	2-6
DP7304B	DP8304B		•	8-Bit 48 mA Bus Transceiver	2-11
	DP8307A		•	8-Bit 48 mA Bus Transceiver	2-16
DP7308	DP8308		•	8-Bit 48 mA Bus Transceiver	2-20
MM54C373	MM74C373		•	Octal D-Type Latch	CMOS
MM54C374	MM74C374		•	Octal D-Type Flip-Flop	CMOS
MM54C922	MM74C922		•	16-Key Encoder	CMOS
MM54C923	MM74C923		•	20-Key Encoder	CMOS
DM54LS373	DM74LS373		•	Octal Transparent D Latch	Logic
DM54LS374	DM74LS374		•	Octal Edge-Triggered D Flip-Flop	Logic

National Semiconductor

DP8212/DP8212M 8-Bit Input/Output Port

General Description

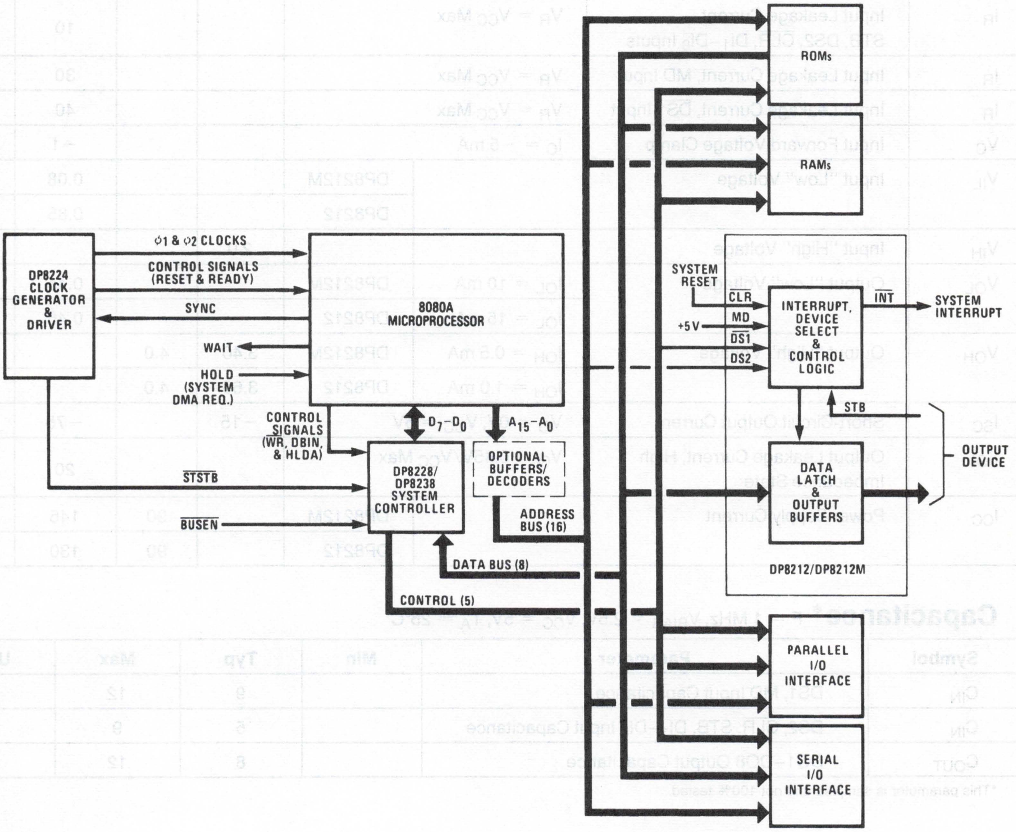
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's 8080A support family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit data latch and buffer
- Service request flip-flop for generation and control of interrupts
- 0.25 mA input load current
- TRI-STATE TTL output drive capability
- Outputs sink 15 mA
- Asynchronous latch clear
- 3.65V output for direct interface to INS8080A
- Reduces system package count by replacing buffers, latches, and multiplexers in microcomputer systems

8080A Microcomputer Family Block Diagram


DP8224 CLOCK GENERATOR & DRIVER
φ1 & φ2 CLOCKS
CONTROL SIGNALS (RESET & READY)
SYNC
8080A MICROPROCESSOR
WAIT
HOLD (SYSTEM DMA REQ.)
CONTROL SIGNALS (WR, DBIN, & HLDA)
$\overline{STSTB}$
$\overline{BUSEN}$
DP8228/DP8238 SYSTEM CONTROLLER
D_7–D_0
A_{15}–A_0
OPTIONAL BUFFERS/ DECODERS
ADDRESS BUS (16)
DATA BUS (8)
CONTROL (5)
ROMs
RAMs
SYSTEM RESET
$\overline{CLR}$
MD
+5V
$\overline{DS1}$
DS2
INTERRUPT, DEVICE SELECT & CONTROL LOGIC
$\overline{INT}$
SYSTEM INTERRUPT
STB
OUTPUT DEVICE
DATA LATCH & OUTPUT BUFFERS
DP8212/DP8212M
PARALLEL I/O INTERFACE
SERIAL I/O INTERFACE

TL/F/6824-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V
Output Currents	125 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1903 mW
Molded Package	2005 mW

*Derate cavity package 12.7 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8212M	4.50	5.50	V_{DC}
DP8212	4.75	5.25	V_{DC}
Operating Temperaure (T_A)			
DP8212M	−55	+125	°C
DP8212	0	+75	°C

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

Electrical Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_F	Input Load Current, STB, DS2, $\overline{\text{CLR}}$, DI_1–DI_8 Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current, MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current, $\overline{\text{DS1}}$ Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current STB, DS2, $\overline{\text{CLR}}$, DI_1–DI_8 Inputs	$V_R = V_{CC}$ Max				10	μA
I_R	Input Leakage Current, MD Input	$V_R = V_{CC}$ Max				30	μA
I_R	Input Leakage Current, $\overline{\text{DS1}}$ Input	$V_R = V_{CC}$ Max				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5$ mA				−1	V
V_{IL}	Input "Low" Voltage		DP8212M			0.08	V
			DP8212			0.85	V
V_{IH}	Input "High" Voltage			2.0			V
V_{OL}	Output "Low" Voltage	$I_{OL} = 10$ mA	DP8212M			0.45	V
		$I_{OL} = 15$ mA	DP8212			0.45	V
V_{OH}	Output "High" Voltage	$I_{OH} = 0.5$ mA	DP8212M	3.40	4.0		V
		$I_{OH} = 1.0$ mA	DP8212	3.65	4.0		V
I_{SC}	Short-Circuit Output Current	$V_O = 0V$, $V_{CC} = 5V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current, High Impedance State	$V_O = 0.45V/V_{CC}$ Max				20	μA
I_{CC}	Power Supply Current		DP8212M		90	145	mA
			DP8212		90	130	mA

Capacitance* F = 1 MHz, $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Min	Typ	Max	Units
C_{IN}	DS1, MD Input Capacitance		9	12	pF
C_{IN}	DS2, $\overline{\text{CLR}}$, STB, DI_1–DI_8 Input Capacitance		5	9	pF
C_{OUT}	DO1–DO8 Output Capacitance		8	12	pF

*This parameter is sampled and not 100% tested.

Switching Characteristics $\text{Min} \le T_A \le \text{Max}, \text{Min} \le V_{CC} \le \text{Max}$

Symbol	Parameter	Conditions	DP8212M		DP8212		Units
			Min	Max	Min	Max	
t_{PW}	Pulse Width		40		30		ns
t_{PD}	Data to Output Delay	(Note 1)		30		30	ns
t_{WE}	Write Enable to Output Delay	(Note 1)		50		40	ns
t_{SET}	Data Set-Up Time		20		15		ns
t_H	Data Hold Time		30		20		ns
t_R	Reset to Output Delay	(Note 1)		55		40	ns
t_S	Set to Output Delay	(Note 1)		35		30	ns
t_E	Output Enable/Disable Time	(Note 2)		50		45	ns
t_C	Clear to Output Delay	(Note 1)		65		55	ns

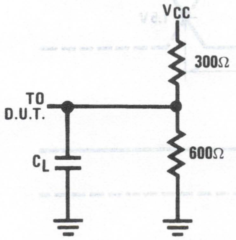
Note 1: $C_L = 30$ pF

Note 2: $C_L = 30$ pF except for DP8212M
$t_{E\ (DISABLE)}$ $C_L = 5$ pF

Switching Conditions

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5 ns.
3. Between 1V and 2V Measurements made at 1.5V with 15 mA & 30 pF Test Load.
4. C_L includes jig and probe capacitance.
5. $C_L = 30$ pF.
6. $C_L = 30$ pF except for DP8212M $t_{E\ (DISABLE)}$ $C_L = 5$ pF

Test Load



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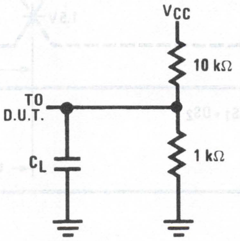
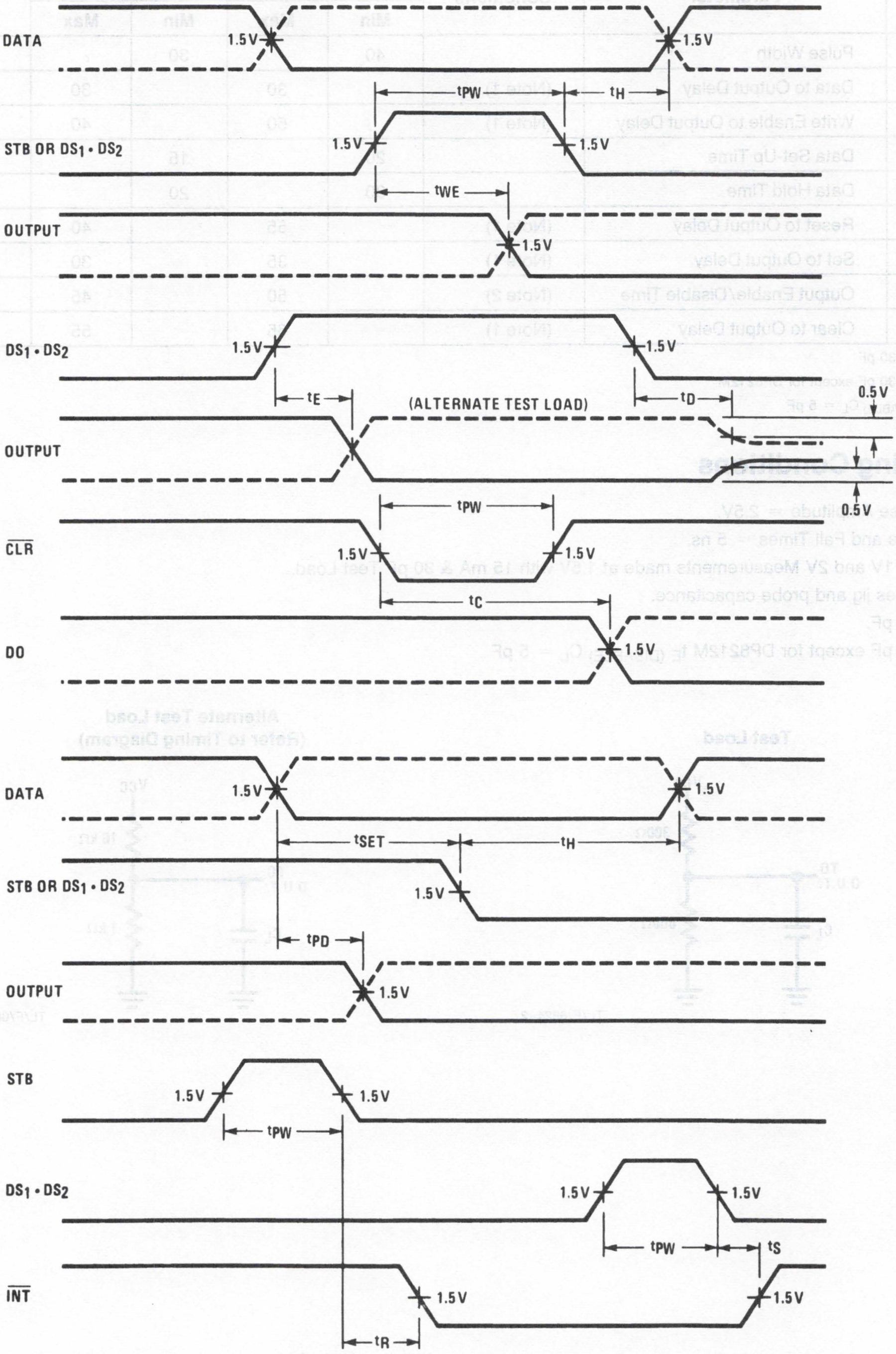
Alternate Test Load
(Refer to Timing Diagram)



TL/F/6824-3

Timing Diagram


DATA
1.5V
1.5V
tPW
tH
STB OR DS1 • DS2
1.5V
1.5V
tWE
OUTPUT
1.5V
DS1 • DS2
1.5V
1.5V
tE
(ALTERNATE TEST LOAD)
tD
0.5V
VOH
OUTPUT
VOL
0.5V
tPW
CLR
1.5V
1.5V
tC
DO
1.5V
DATA
1.5V
1.5V
tSET
tH
STB OR DS1 • DS2
1.5V
tPD
OUTPUT
1.5V
STB
1.5V
1.5V
tPW
DS1 • DS2
1.5V
1.5V
tPW
tS
INT
1.5V
1.5V
tR

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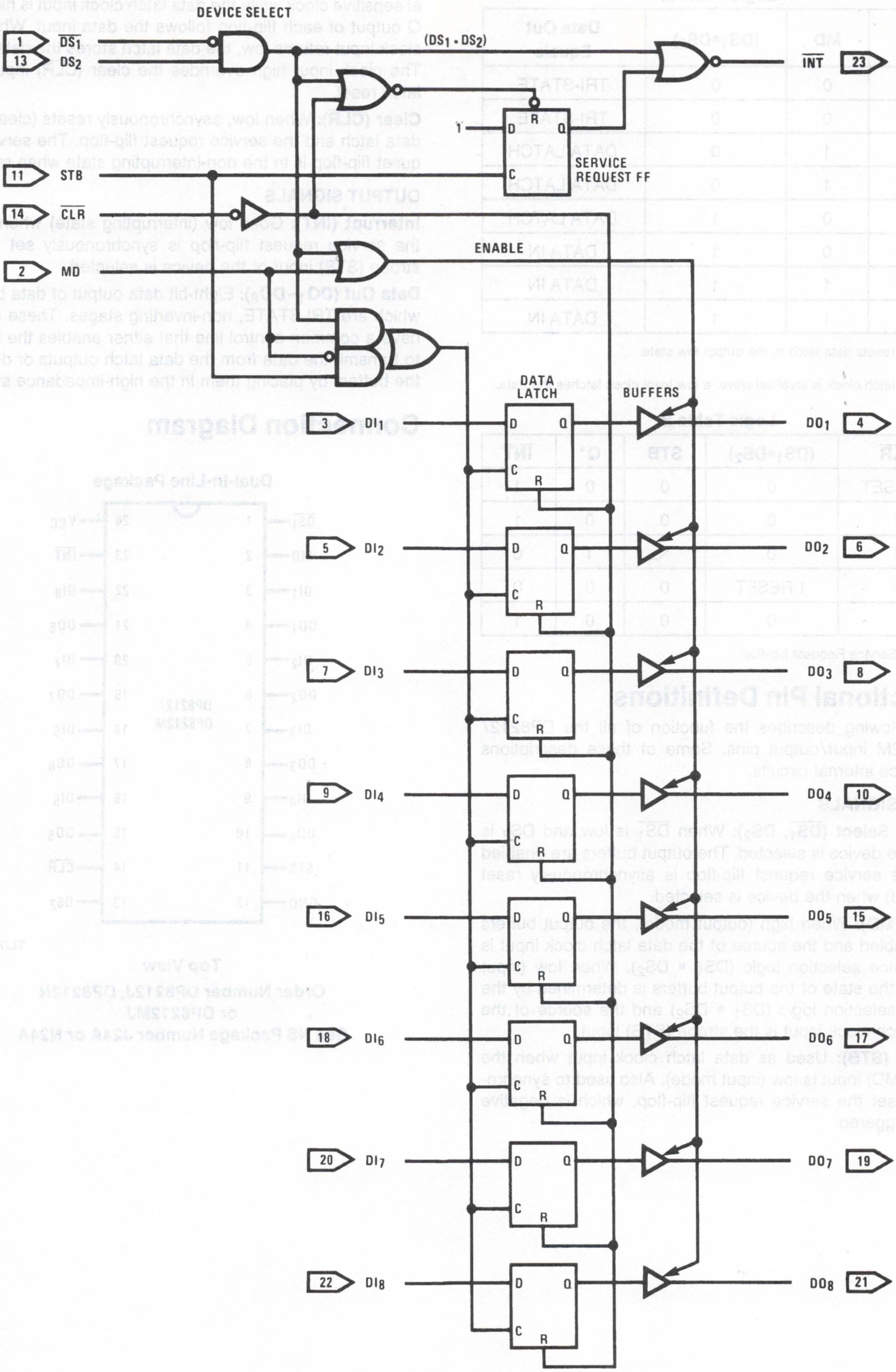
Logic Diagram


DEVICE SELECT
1
$\overline{DS_1}$
13
DS_2
$(DS_1 \cdot DS_2)$
$\overline{INT}$
23
1
D
R
Q
C
SERVICE REQUEST FF
11
STB
14
$\overline{CLR}$
2
MD
ENABLE
DATA LATCH
BUFFERS
3
DI_1
DO_1
4
5
DI_2
DO_2
6
7
DI_3
DO_3
8
9
DI_4
DO_4
10
16
DI_5
DO_5
15
18
DI_6
DO_6
17
20
DI_7
DO_7
19
22
DI_8
DO_8
21

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Logic Tables

Logic Table A

STB	MD	($DS_1 \bullet DS_2$)	Data Out Equals
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{\text{CLR}}$ ↘ resets data latch to the output low state.

The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{\text{CLR}}$	($DS_1 \bullet DS_2$)	STB	Q*	$\overline{\text{INT}}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	↘	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Functional Pin Definitions

The following describes the function of all the DP8212/DP8212M input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic ($DS_1 \bullet DS_2$). When low (input mode), the state of the output buffers is determined by the device selection logic ($DS_1 \bullet DS_2$) and the source of the data latch clock input is the strobe (STB) input.

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1–DI_8): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. Incorporating a level sensitive clock while the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear ($\overline{\text{CLR}}$) input data latch reset.

Clear ($\overline{\text{CLR}}$): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

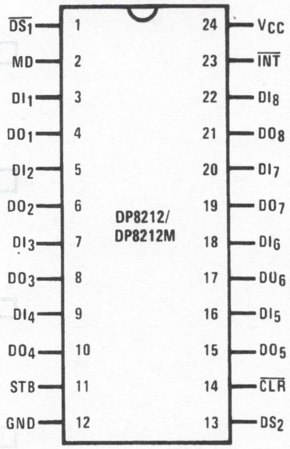
OUTPUT SIGNALS

Interrupt ($\overline{\text{INT}}$): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1–DO_8): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

Connection Diagram

Dual-In-Line Package



TL/F/6824-6

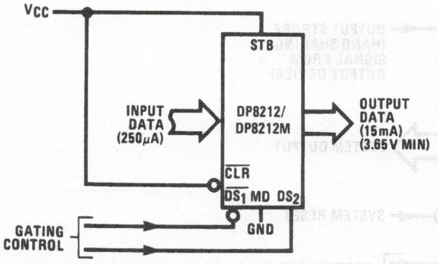
Top View

Order Number DP8212J, DP8212N or DP8212MJ

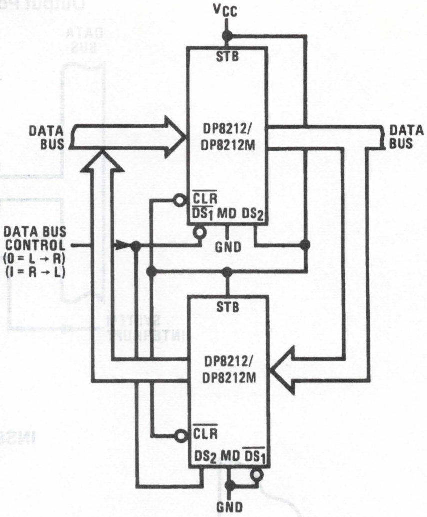
See NS Package Number J24A or N24A

Applications in Microcomputer Systems

Gated Buffer
(TRI-STATE)


VCC
STB
INPUT DATA (250μA)
DP8212/ DP8212M
OUTPUT DATA (15mA) (3.65V MIN)
CLR
DS1 MD DS2
GND
GATING CONTROL

TL/F/6824-7


VCC
STB
DATA BUS
DP8212/ DP8212M
DATA BUS
CLR
DS1 MD DS2
GND
DATA BUS CONTROL (0 = L → R) (I = R → L)
STB
DP8212/ DP8212M
CLR
DS2 MD DS1
GND

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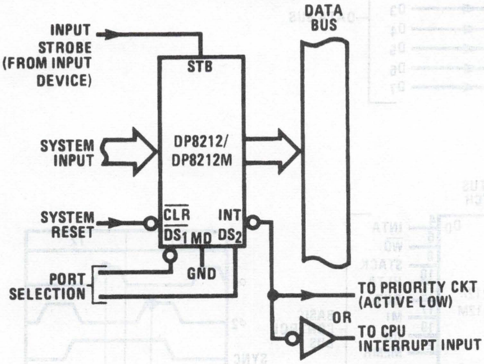
Interrupting Input Port


INPUT STROBE (FROM INPUT DEVICE)
DATA BUS
STB
SYSTEM INPUT
DP8212/ DP8212M
SYSTEM RESET
CLR
INT
DS1 MD DS2
PORT SELECTION
GND
TO PRIORITY CKT (ACTIVE LOW)
OR
TO CPU INTERRUPT INPUT

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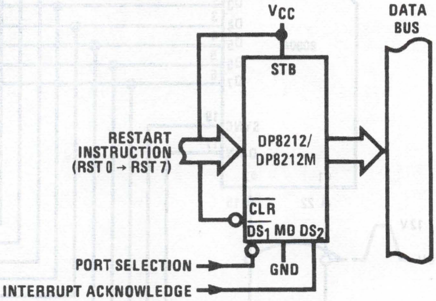
Interrupt Instruction Port


VCC
DATA BUS
STB
RESTART INSTRUCTION (RST 0 → RST 7)
DP8212/ DP8212M
CLR
DS1 MD DS2
PORT SELECTION
GND
INTERRUPT ACKNOWLEDGE

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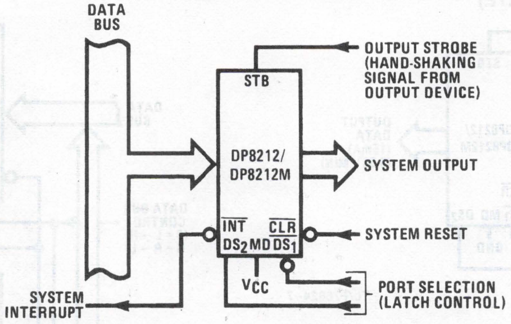
Applications in Microcomputer Systems (Continued)

Output Port (with Hand-Shanking)


DATA BUS
STB
OUTPUT STROBE (HAND-SHAKING SIGNAL FROM OUTPUT DEVICE)
DP8212/ DP8212M
SYSTEM OUTPUT
INT
CLR
DS2 MD DS1
SYSTEM RESET
VCC
PORT SELECTION (LATCH CONTROL)
SYSTEM INTERRUPT

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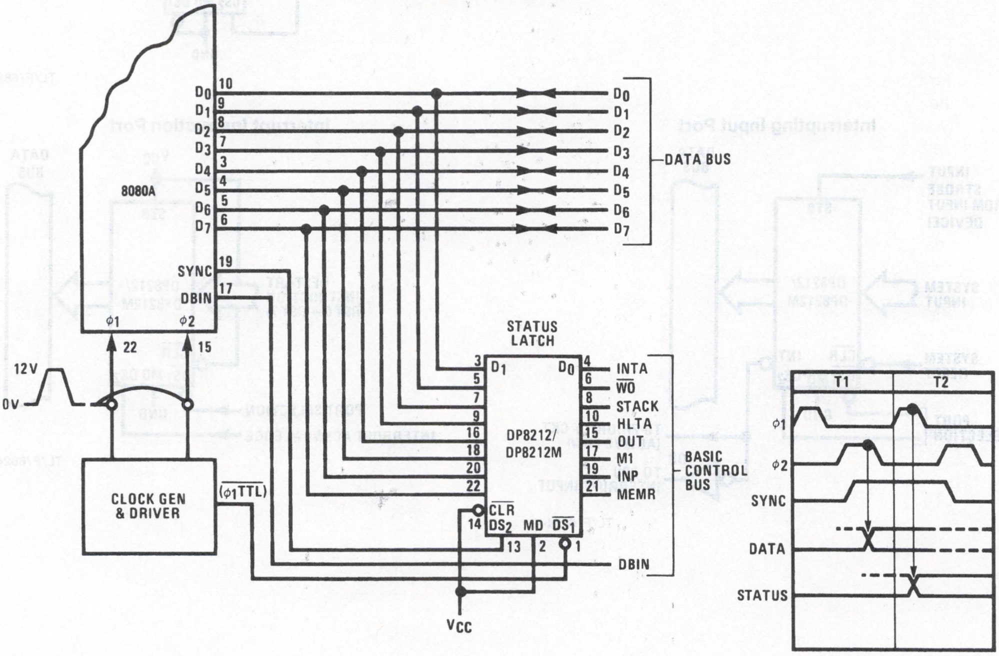
INS8080A Status Latch


8080A
D0 10
D1 9
D2 8
D3 7
D4 3
D5 4
D6 5
D7 6
SYNC 19
DBIN 17
φ1 22
φ2 15
12V
0V
CLOCK GEN & DRIVER
(φ1TTL)
D0
D1
D2
D3
D4
D5
D6
D7
DATA BUS
STATUS LATCH
D1 D0
3 4 INTA
5 6 WO
7 8 STACK
9 10 HLTA
16 15 OUT
18 17 M1
20 19 INP
22 21 MEMR
DP8212/ DP8212M
CLR
14 DS2 MD DS1
13 2 1
DBIN
BASIC CONTROL BUS
VCC
T1
T2
φ1
φ2
SYNC
DATA
STATUS

TL/F/6824-12

National Semiconductor

DP8216/DP8216M/DP8226/DP8226M 4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bi-directional bus drivers to use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit drivers consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high driver (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The CS input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

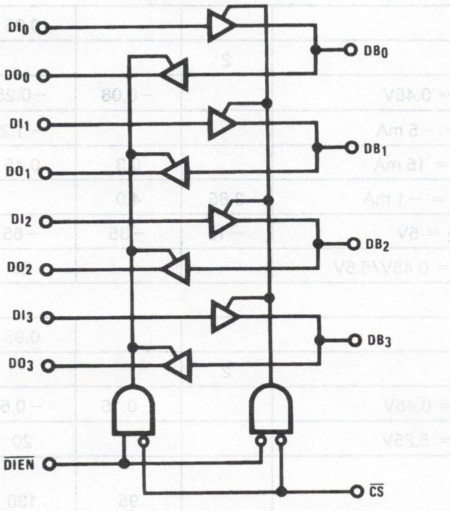
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

- Data bus buffer driver to 8080 type CPUs
- Low input load current—0.25 mA maximum
- High output drive capability for driving system data bus—50 mA at 0.5V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature

Logic Diagrams

DP8216/DP8216M



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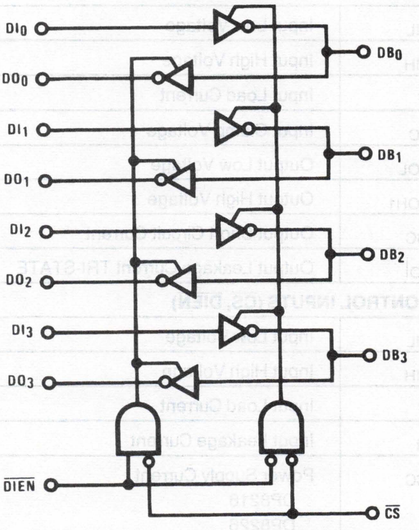
DP8226/DP8226M



TL/F/8753-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Min	Max	Units
All Output and Supply Voltages	−0.5	+7.0	V
All Input Voltages	−1.0	+5.5	V
Output Currents		125	mA
Maximum Power Dissipation* at 25°C			
Cavity Package		1509	mW
Molded Package		1476	mW
Storage Temperature	−65	+150	°C
Lead Temperature (soldering, 4 seconds)		260	°C

Note: *Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DP8216M, DP8226M	4.5	5.5	V
DP8216, DP8226	4.75	5.25	V
Temperature, T_A			
DP8216M, DP8226M	−55	+125	°C
DP8216, DP8226	0	+70	°C

Electrical Characteristics DP8216, DP8226 V_{CC} = 5V ±5% (Notes 2, 3, and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.03	−0.25	mA
I_R	Input Leakage Current	$V_R = 5.25V$			10	μA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL1}	Output Low Voltage	$I_{OL} = 25$ mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	DP8216 $I_{OL} = 55$ mA DP8226 $I_{OL} = 50$ mA		0.5	0.6	V
V_{OH}	Output High Voltage	$I_{OH} = -10$ mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5V$	−30	−75	−120	mA
$\lvert I_O \rvert$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.08	−0.25	mA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL}	Output Low Voltage	$I_{OL} = 15$ mA		0.3	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -1$ mA	3.65	4.0		V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5V$	−15	−35	−65	mA
$\lvert I_O \rvert$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.15	−0.5	mA
I_R	Input Leakage Current	$V_R = 5.25V$			20	μA
I_{CC}	Power Supply Current					
	DP8216			95	130	mA
	DP8226			85	120	mA

Electrical Characteristics (Continued) DP8216M, DP8226M $V_{CC} = 5V \pm 10\%$ (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.90	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.08	−0.25	mA
I_R	Input Leakage Current	$V_R = 5.5V$			40	μA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL1}	Output Low Voltage	$I_{OL} = 25$ mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	$I_{OL} = 45$ mA		0.5	0.6	V
V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.08	−0.25	mA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL}	Output Low Voltage	$I_{OL} = 15$ mA		0.3	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -0.5$ mA	3.4	3.8		V
V_{OH2}	Output High Voltage	$I_{OH} = -2$ mA	2.4			V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.15	−0.5	mA
I_R	Input Leakage Current	$V_R = 5.5V$			80	μA
I_{CC}	Power Supply Current DP8216M DP8226M			 95 85	 130 120	 mA mA

Switching Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Units
DP8216M, DP8226M, $V_{CC} = 5V \pm 10\%$						
t_{PD1}	Input to Output Delay, DO Outputs	$C_L = 30$ pF, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216M DP8226M	$C_L = 300$ pF, $R_1 = 90\Omega$, $R_2 = 180\Omega$		19 16	33 25	ns ns
t_E	Output Enable Time DP8216M DP8226M	DO Outputs: $C_L = 30$ pF, $R_1 = 300\Omega/10$ kΩ, $R_2 = 600\Omega/1$ kΩ DB Outputs: $C_L = 300$ pF, $R_1 = 90\Omega/10$ kΩ, $R_2 = 180\Omega/1$ kΩ		42 36	75 62	ns ns
t_D	Output Disable Time DP8216M DP8226M	DO Outputs: $C_L = 5$ pF, $R_1 = 300\Omega/10$ kΩ, $R_2 = 600\Omega/1$ kΩ DB Outputs: $C_L = 5$ pF, $R_1 = 90\Omega/10$ kΩ, $R_2 = 180\Omega/1$ kΩ		16 16	40 38	ns ns
DP8216, DP8226 $V_{CC} = 5.0V \pm 5\%$						
t_{PD1}	Input to Output Delay, DO Outputs	$C_L = 30$ pF, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216 DP8226	$C_L = 300$ pF, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20 16	30 25	ns ns
t_E	Output Enable Time DP8216 DP8226	DO Outputs: $C_L = 30$ pF, $R_1 = 300\Omega/10$ kΩ, $R_2 = 600\Omega/1$ kΩ DB Outputs: $C_L = 300$ pF, $R_1 = 90\Omega/10$ kΩ, $R_2 = 180\Omega/1$ kΩ		45 35	65 54	ns ns
t_D	Output Disable Time	DO Outputs: $C_L = 5$ pF, $R_1 = 300\Omega/10$ kΩ, $R_2 = 600\Omega/1$ kΩ DB Outputs: $C_L = 5$ pF, $R_1 = 90\Omega/10$ kΩ, $R_2 = 180\Omega/1$ kΩ		20	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DP8216M and DP8226M and across the 0°C to +70°C temperature range for the DP8216 and DP8226. All typical values are given for $V_{CC} = 5V$ and $T_A = 25°C$.

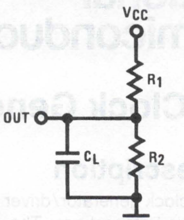
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Test Conditions

Input pluse amplitude of 2.5V.
Input rise and fall times of 5.0 ns between 1.0V and 2.0V.
Output loading is 5.0 mA and 10 pF.
Speed measurements are made at 1.5V levels.

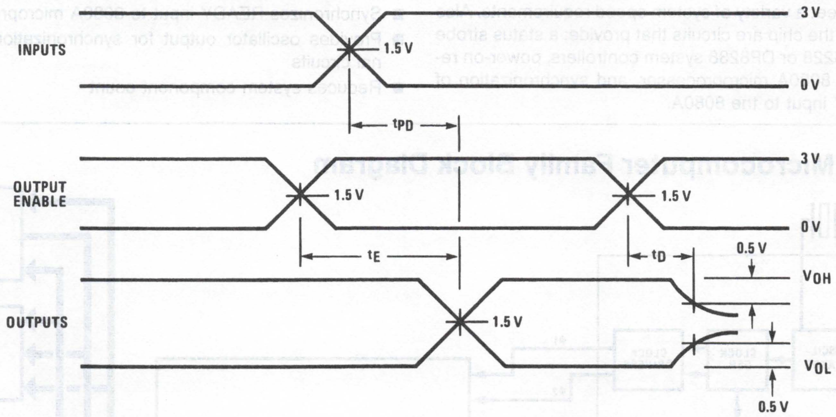
Test Load Circuit



V_{CC}
R_1
OUT
C_L
R_2

TL/F/8753-4

Switching Time Waveforms

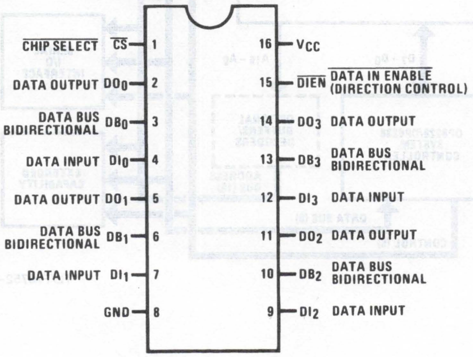


INPUTS
3 V
1.5 V
0 V
t_{PD}
OUTPUT ENABLE
3 V
1.5 V
1.5 V
0 V
t_E
t_D
0.5 V
V_{OH}
OUTPUTS
1.5 V
V_{OL}
0.5 V

TL/F/8753-5

Connection Diagram

Dual-In-Line Package



CHIP SELECT $\overline{CS}$ 1
DATA OUTPUT DO_0 2
DATA BUS BIDIRECTIONAL DB_0 3
DATA INPUT DI_0 4
DATA OUTPUT DO_1 5
DATA BUS BIDIRECTIONAL DB_1 6
DATA INPUT DI_1 7
GND 8
16 V_{CC}
15 $\overline{DIEN}$ $\overline{DATA IN ENABLE}$ (DIRECTION CONTROL)
14 DO_3 DATA OUTPUT
13 DB_3 DATA BUS BIDIRECTIONAL
12 DI_3 DATA INPUT
11 DO_2 DATA OUTPUT
10 DB_2 DATA BUS BIDIRECTIONAL
9 DI_2 DATA INPUT

TL/F/8753-3

Order Number DP8216J, DP8216N, DP8226J, DP8226N, DP8216MJ or DP8226MJ
See NS Package Number J16A or N16A

Capacitance $T_A = 25°C$

Symbol	Parameter	Limit			Unit
		Min	Typ	Min	
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DO Outputs		13	18	pF

Note: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V, and T_A = 25°C.

National Semiconductor

DP8224 Clock Generator and Driver

General Description

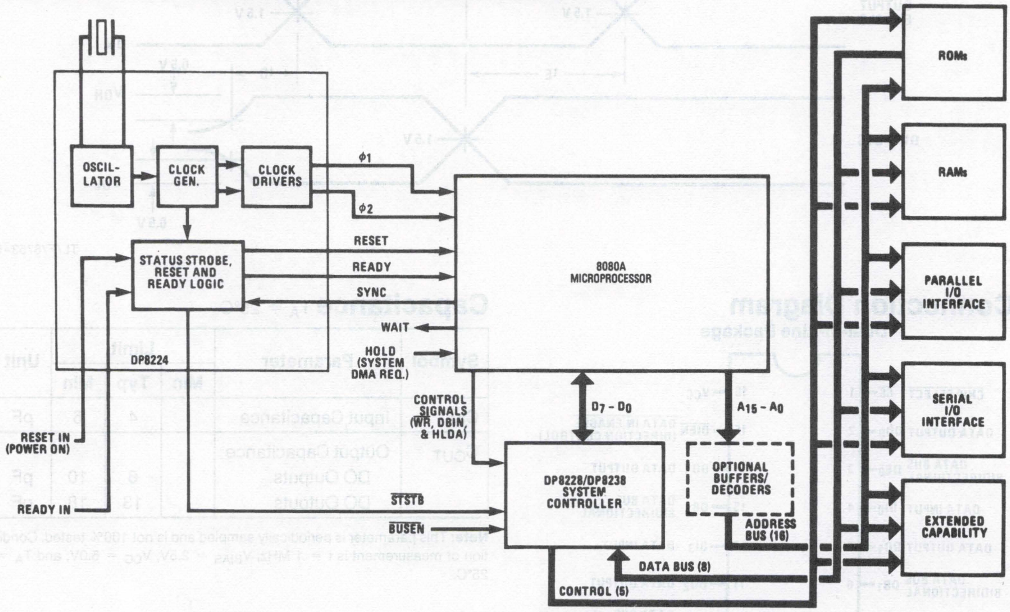
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for the 8080A microcomputer family.

Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the 8080A microprocessor, and synchronization of the READY input to the 8080A.

Features

- Crystal-controlled oscillator for stable system operation
- Single chip clock generator and driver for 8080A microprocessor
- Provides status strobe for DP8228 or DP8238 system controllers
- Provides power-on reset for 8080A microprocessor
- Synchronizes READY input to 8080A microprocessor
- Provides oscillator output for synchronization of external circuits
- Reduces system component count

8080A Microcomputer Family Block Diagram


OSCIL-LATOR
CLOCK GEN.
CLOCK DRIVERS
φ1
φ2
STATUS STROBE, RESET AND READY LOGIC
RESET
READY
SYNC
WAIT
HOLD (SYSTEM DMA REQ.)
DP8224
8080A MICROPROCESSOR
CONTROL SIGNALS (WR, DBIN, & HLDA)
RESET IN (POWER ON)
READY IN
STSTB
BUSEN
D7 - D0
A15 - A0
DP8228/DP8238 SYSTEM CONTROLLER
OPTIONAL BUFFERS/ DECODERS
ADDRESS BUS (16)
DATA BUS (8)
CONTROL (5)
ROMs
RAMs
PARALLEL I/O INTERFACE
SERIAL I/O INTERFACE
EXTENDED CAPABILITY

TL/F/8752-1

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{DD}	15V
Input Voltage	−1V to +5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_F	Input Current Loading	$V_F = 0.45V$			−0.25	mA
I_R	Input Leakage Current	$V_R = 5.25V$			10	µA
V_C	Input Forward Clamp Voltage	$I_C = -5$ mA			−1.0	V
V_{IL}	Input "Low" Voltage	$V_{CC} = 5V$			0.8	V
V_{IH}	Input "High" Voltage	$\overline{\text{RESIN}}$ Input	2.6			V
		All Other Inputs	2.0			V
$V_{IH}-V_{IL}$	$\overline{\text{RESIN}}$ Input Hysteresis	$V_{CC} = 5V$	0.25			V
V_{OL}	Output "Low" Voltage					
	($\phi 1$, $\phi 2$), Ready, Reset $\overline{\text{STSTB}}$	$I_{OL} = 2.5$ mA			0.45	V
	Osc., $\phi 2$ (TTL)	$I_{OL} = 10$ mA			0.45	V
	Osc., $\phi 2$ (TTL)	$I_{OL} = 15$ mA			0.45	V
V_{OH}	Output "High" Voltage					
	$\phi 1$, $\phi 2$	$I_{OH} = -100$ µA	9.4			V
	Ready, Reset	$I_{OH} = -100$ µA	3.6			V
	Osc., $\phi 2$ (TTL), $\overline{\text{STSTB}}$	$I_{OH} = -1$ mA	2.4			V
I_{SC}	Output Short-Circuit Current (All Low Voltage Outputs Only), (Note 1)	$V_O = 0V$, $V_{CC} = 5V$	−10		−60	mA
I_{CC}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				12	mA

Note 1: Caution $-\phi 1$ and $\phi 2$ output drivers do not have short circuit protection.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DP8224. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$, and $V_{DD} = 12V$.

Crystal Requirements*

Tolerance	0.005% at 0°C to +70°C	Equivalent Resistance	75Ω to 20Ω
Resonance	Fundamental	Power Dissipation (Min)	4 mW
Load Capacitance	20 pF to 30 pF		

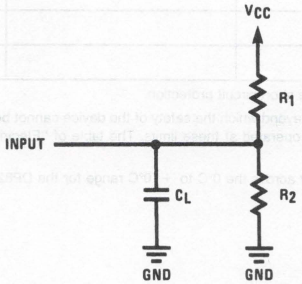
*It is good design practice to ground the case of the crystal

**With tank circuit, use 3rd overtone mode

Switching Characteristics (Note 3)

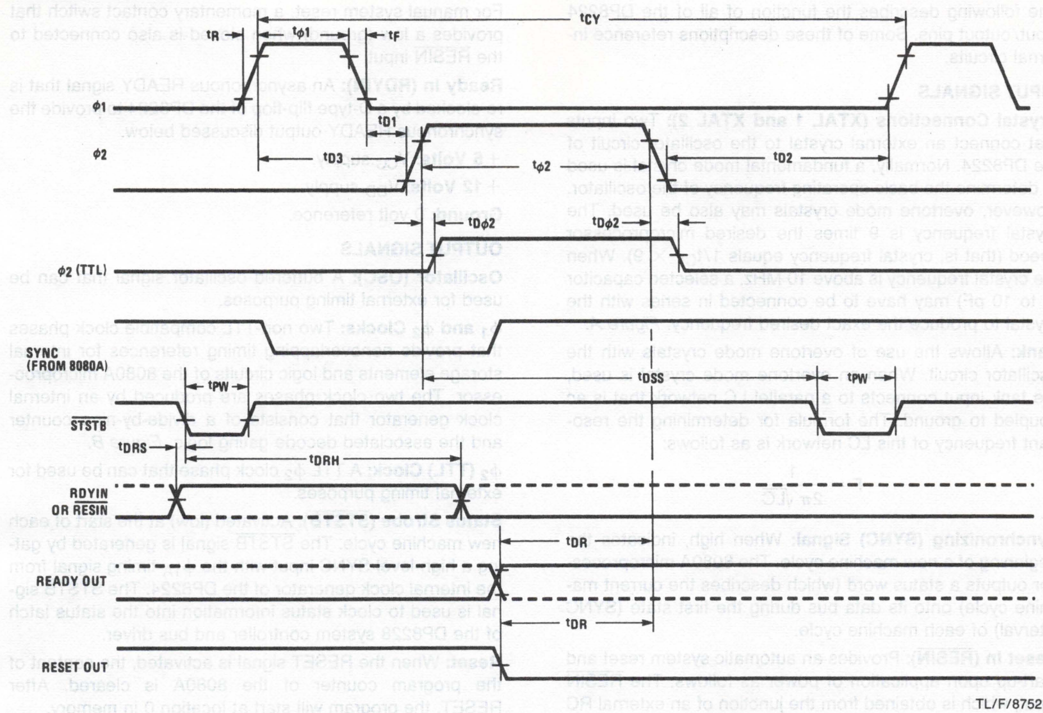
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	ϕ1 Pulse Width	C_L = 20 pF to 50 pF	$\frac{2t_{CY}}{9} - 20$			ns
$t_{\phi 2}$	ϕ2 Pulse Width		$\frac{5t_{CY}}{9} - 35$			ns
t_{D1}	ϕ1 to ϕ2 Delay		0			ns
t_{D2}	ϕ2 to ϕ1 Delay		$\frac{2t_{CY}}{9} - 14$			ns
t_{D3}	ϕ1 to ϕ2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$	ns
t_r	ϕ1 and ϕ2 Rise Time				20	ns
t_f	ϕ1 and ϕ2 Fall Time				20	ns
$t_{D\phi 2}$	ϕ2 to ϕ2 (TTL) Delay	ϕ2 TTL, C_L = 30 pF, R1 = 300Ω, R2 = 600Ω	−5		15	ns
t_{DSS}	ϕ2 to $\overline{\text{STSTB}}$ Delay	$\overline{\text{STSTB}}$, C_L = 15 pF R1 = 2 kΩ, R2 = 4 kΩ	$\frac{6t_{CY}}{9} - 30$		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{\text{STSTB}}$ Pulse Width		$\frac{t_{CY}}{9} - 15$			ns
t_{DRS}	RDYIN Set-Up Time to Status Strobe		$50 - \frac{4t_{CY}}{9}$			ns
t_{DRH}	RDYIN Hold Time After $\overline{\text{STSTB}}$		$\frac{4t_{CY}}{9}$			ns
t_{DR}	READY or RESET to ϕ2 Delay	Ready and Reset, C_L = 10 pF, R1 = 2 kΩ, R2 = 4 kΩ	$\frac{4t_{CY}}{9} - 25$			ns
t_{CLK}	CLK Period		$\frac{t_{CY}}{9}$			ns
f_{MAX}	Maximum Oscillating Frequency		27			MHz
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1 MHz			8	pF

Test Circuit



TL/F/8752-2

Waveforms


tCY
tR
tφ1
tF
φ1
tD1
φ2
tD3
tφ2
tD2
tDφ2
tDφ2
φ2 (TTL)
SYNC (FROM 8080A)
tPW
STSTB
tDRS
tDRH
tDSS
tPW
RDYIN OR RESIN
tDR
READY OUT
tDR
RESET OUT

TL/F/8752-3

Voltage Measurement Points: φ1, φ2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

Switching Characteristics (For t_{CY} = 488.28 ns)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	φ1 Pulse Width	φ1 and φ2 Loaded to C_L = 20 to 50 pF Ready and Reset Loaded to 2 mA/10 pF All Measurements Referenced to 1.5V unless Specified Otherwise	89			ns
$t_{\phi 2}$	φ2 Pulse Width		236			ns
t_{D1}	Delay φ1 to φ2		0			ns
t_{D2}	Delay φ2 to φ1		95			ns
t_{D3}	Delay φ1 to φ2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	φ2 to STSTB Delay		296		326	ns
$t_{D\phi 2}$	φ2 to φ2 (TTL) Delay		−5		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-Up Time to STSTB		−167			ns
t_{DRH}	RDYIN Hold Time after STSTB		217			ns
t_{DR}	READY or RESET to φ2 Delay		192			ns
f_{MAX}	Oscillator Frequency				18.432	MHz

Functional Pin Definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is 9 times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 pF) may have to be connected in series with the crystal to produce the exact desired frequency. *Figure A*.

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi \sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The 8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the 8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. *Figure B*.

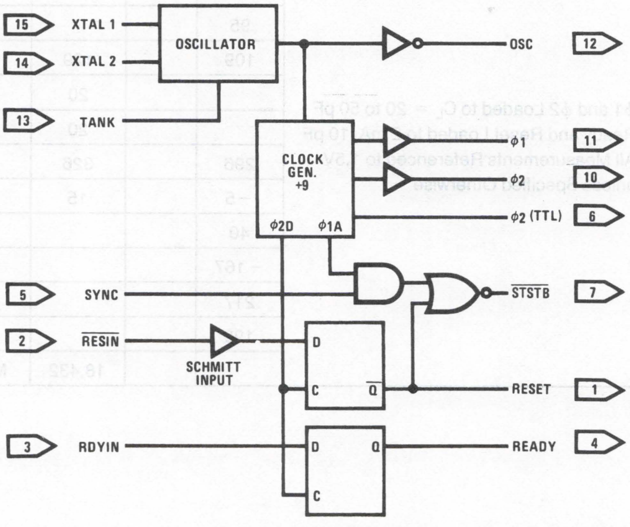
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the 8080A is cleared. After RESET, the program will start at location 0 in memory.

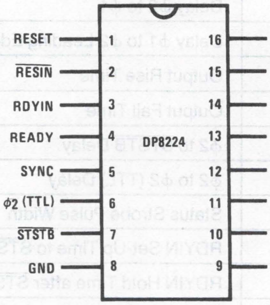
Ready: The READY signal indicates to the 8080A that valid memory or input data is available. This signal is used to synchronize the 8080A with slower memory or input/output devices.

Logic and Connection Diagrams



TL/F/8752–4

Dual-In-Line Package

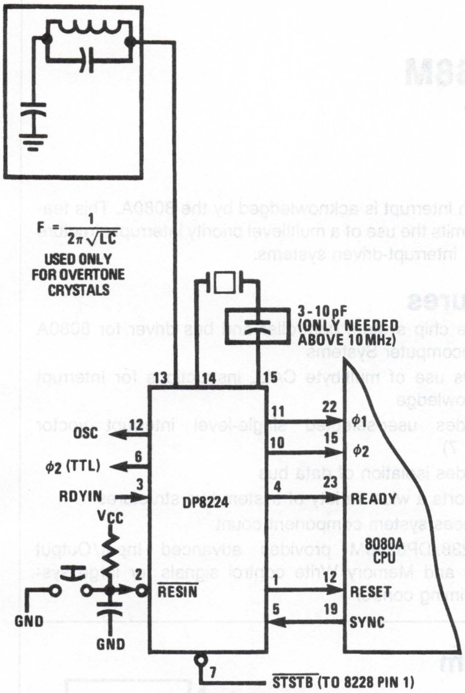


TL/F/8752–5

Top View

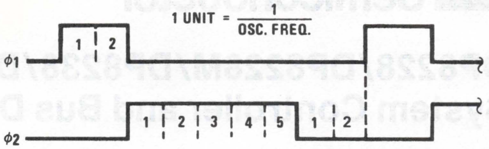
Order Number DP8224J or DP8224N
See NS Package Number
J16A or N16A

Applications Information


F = $\frac{1}{2\pi\sqrt{LC}}$
USED ONLY FOR OVERTONE CRYSTALS
3-10 pF (ONLY NEEDED ABOVE 10 MHz)
13
14
15
OSC
12
φ2 (TTL)
6
RDYIN
3
V_{CC}
DP8224
2
$\overline{RESIN}$
GND
GND
11
22
φ1
10
15
φ2
4
23
READY
8080A CPU
1
12
RESET
5
19
SYNC
7
$\overline{STSTB}$ (TO 8228 PIN 1)

TL/F/8752-6

FIGURE A. DP8224 Connection Diagram


1 UNIT = $\frac{1}{\text{OSC. FREQ.}}$
φ1
1
2
φ2
1
2
3
4
5
1
2

TL/F/8752-7

EXAMPLE: (8080 t_{CY} = 500 ns)
OSC = 18 MHz/55 ns
ϕ_1 = 110 ns (2 × 55 ns)
ϕ_2 = 275 ns (5 × 55 ns)
$\phi_2 - \phi_1$ = 110 ns (2 × 55 ns)

FIGURE B. DP8224 Clock Generator Waveforms

National Semiconductor

DP8228/DP8228M/DP8238/DP8238M System Controller and Bus Driver

General Description

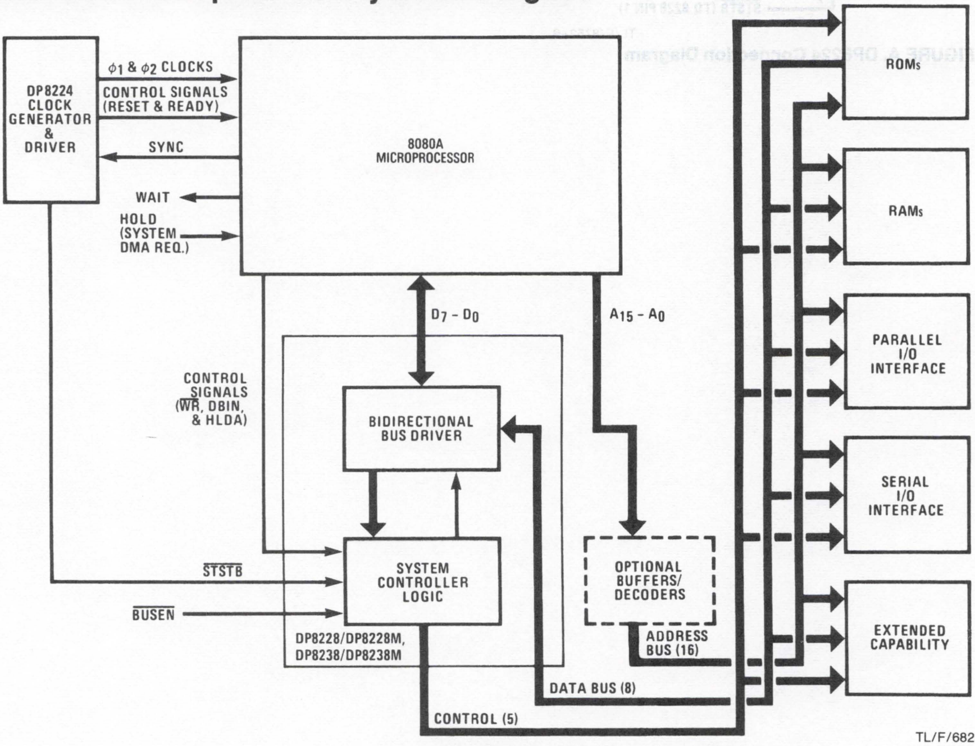
The DP8228/DP8228M, DP8238/DP8238M are system controller/bus drivers contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of the 8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the 8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected signal-level interrupt vector (RST 7) is provided by the device for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The devices also generate an Interrupt Acknowledge ($\overline{\text{INTA}}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the 8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- Single chip system controller and bus driver for 8080A Microcomputer Systems
- Allows use of multibyte CALL instructions for Interrupt Acknowledge
- Provides user-selected single-level interrupt vector (RST 7)
- Provides isolation of data bus
- Supports a wide variety of system bus structures
- Reduces system component count
- DP8238/DP8238M provides advanced Input/Output Write and Memory Write control signals for large system timing control

8080A Microcomputer Family Block Diagram



DP8224 CLOCK GENERATOR & DRIVER
φ1 & φ2 CLOCKS
CONTROL SIGNALS (RESET & READY)
SYNC
WAIT
HOLD (SYSTEM DMA REQ.)
8080A MICROPROCESSOR
D7 - D0
A15 - A0
CONTROL SIGNALS (WR, DBIN, & HLDA)
BIDIRECTIONAL BUS DRIVER
SYSTEM CONTROLLER LOGIC
STSTB
BUSEN
DP8228/DP8228M, DP8238/DP8238M
OPTIONAL BUFFERS/ DECODERS
ADDRESS BUS (16)
DATA BUS (8)
CONTROL (5)
ROMs
RAMs
PARALLEL I/O INTERFACE
SERIAL I/O INTERFACE
EXTENDED CAPABILITY

TL/F/6825–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Input Voltage	−1.5V to +7V
Output Current	100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	2179 mW
Molded Package	2361 mW

*Derate cavity package 14.5 mW/°C above 25°C; derate molded package 18.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8228M, DP8238M	4.50	5.50	V_{DC}
DP8228, DP8238	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8228M, DP8238M	−55	+125	°C
DP8228, DP8238	0	+70	°C

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

Electrical Characteristics $\text{Min} \le T_A \le \text{Max}, \text{Min} \le V_{CC} \le \text{Max}$, unless otherwise noted

Symbol	Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_C	Input Clamp Voltage, All Inputs		V_{CC} = Min, I_C = −5 mA			0.6	−1.0	V
I_F	Input Load Current	$\overline{\text{STSTB}}$	V_{CC} = Max V_F = 0.45V for DP8228, DP8238 V_F = 0.40V for DP8228M, DP8238M				500	µA
		D2 and D6					750	µA
		D0, D1, D4, D5 and D7					250	µA
		All Other Inputs					250	µA
I_R	Input Leakage Current	DB0–DB7	V_{CC} = Max, V_R = V_{CC}				20	µA
		All Other Inputs					100	µA
V_{TH}	Input Threshold Voltage, All Inputs		V_{CC} = 5V		0.8		2.0	V
I_{CC}	Power Supply Current		V_{CC} = Max	DP8228, DP8238		160	190	mA
				DP8228M, DP8238M		160	210	mA
V_{OL}	Output Low Voltage	D0–D7	V_{CC} = Min, I_{OL} = 2 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
		All Other Outputs	V_{CC} = Min, I_{OL} = 10 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
V_{OH}	Output High	D0–D7	V_C = Min, I_{OL} = −10 µA	DP8228M, DP8238M	3.3	3.8		V
				DP8228, DP8238	3.6	3.8		V
		All Other Outputs	V_{CC} = Min, I_{OH} = −1 mA		2.4	3.8		V
I_{OS}	Short Circuit Current, All Outputs		V_{CC} = 5V, V_O = 0V		15		90	mA
$I_{O\,(OFF)}$	OFF State Output Current All Control Outputs		V_{CC} = Max, V_O = V_{CC}				100	µA
			V_{CC} = Max, V_O = 0.45V				−100	µA
I_{INT}	INTA Current		(See Test Conditions, *Figure 3*)				5	mA

Note 1: Typical values are for T_A = 25°C and typical supply voltages.

Capacitance* $V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1\ MHz$

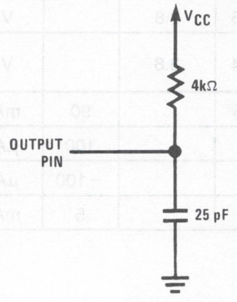
Symbol	Parameter	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

*This parameter is periodically sampled and not 100% tested.

Switching Characteristics $Min \le V_{CC} \le Max, Min \le T_A \le Max$

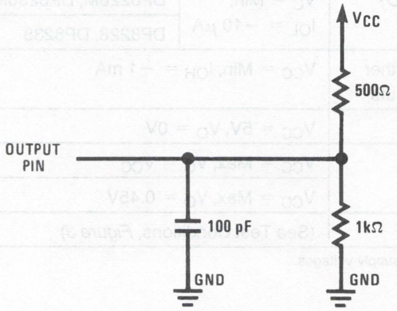
Symbol	Parameter	Conditions	DP8228M, DP8238M		DP8228, DP8238		Units
			Min	Max	Min	Max	
t_{PW}	Width of Status Strobe		25		22		ns
t_{SS}	Set-Up Time, Status Inputs D0–D7		8		8		ns
t_{SH}	Hold Time, Status Inuts D0–D7		5		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	*(Figure 2)*	20	75	20	60	ns
t_{RR}	Delay from DBIN to Control Outputs	*(Figure 2)*		30		30	ns
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus	*(Figure 1)*		45		45	ns
t_{RD}	Delay from System Bus to 8080 Bus During Read	*(Figure 1)*		45		30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	*(Figure 2)*	5	60	5	45	ns
t_{WE}	Delay to Enable System Bus DB0–DB7 after $\overline{STSTB}$	*(Figure 2)*		30		30	ns
t_{WD}	Delay from 8080 Bus D0–D7 to System Bus DB0–DB7 During Write	*(Figure 2)*	5	40	5	40	ns
t_E	Delay from System Bus Enable to System Bus DB0–DB7	*(Figure 2)*		30		30	ns
t_{HD}	HLDA to Read Status Outputs	*(Figure 2)*		25		25	ns
t_{DS}	Set-Up Time, System Bus Inputs to HLDA		10		10		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20		20		ns

Test Conditions



TL/F/6825-2

FIGURE 1. Test Load



TL/F/6825-3

FIGURE 2. Test Load

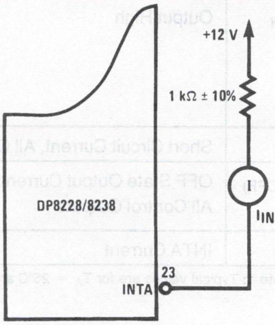


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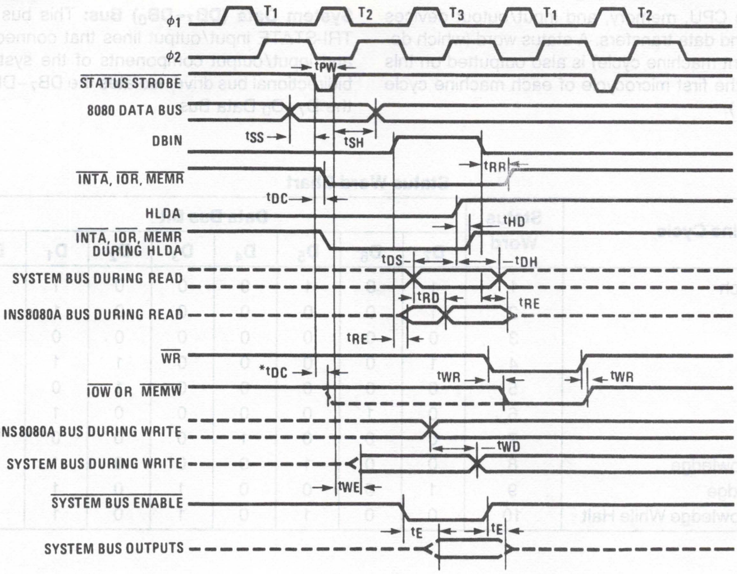
FIGURE 3. INTA Test Circuit (For RST 7)

Timing Diagram



TL/F/6825-5

VOLTAGE MEASUREMENT POINTS: D_0–D_7 (when outputs) Logic "0" = 0.8V, Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Advanced $\overline{\text{I/OW}}$ $\overline{\text{MEMW}}$ for 8238 only.

Functional Pin Definitions

The following describes the function of all of the DP8228/DP8228M, DP8238/DP8238M pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ input is used to store a status word (refer to chart) from the 8080A microprocessor into the internal status latch of the DP8228, DP8238. The status word is latched when the $\overline{\text{STSTB}}$ returns to the high state. The 8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the 8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{\text{WR}}$): When low, indicates that the data on the 8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the 8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{\text{I/OR}}$, $\overline{\text{MEMR}}$, or $\overline{\text{INTA}}$ (return to the output high state).

Bus Enable ($\overline{\text{BUSEN}}$): Asynchronous DMA input to the internal gating array. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5V.

Ground: 0V reference.

OUTPUT SIGNALS

Memory Read ($\overline{\text{MEMR}}$): When low, signals data to be loaded in from memory. The $\overline{\text{MEMR}}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{\text{MEMW}}$): When low, signals data to be stored in memory. The $\overline{\text{MEMW}}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{\text{MEMW}}$ signal is generated by gating a low-level $\overline{\text{WR}}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{\text{I/OR}}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{\text{I/OR}}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{\text{I/OW}}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{\text{I/OW}}$ signal for the DP8238 is generated by strobing in status word 7. For the DP8238 the $\overline{\text{I/OW}}$ signal is generated by gating in a low-level $\overline{\text{WR}}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{\text{INTA}}$): When low, indicates that an interrupt has been acknowledged by the 8080A microprocessor. The $\overline{\text{INTA}}$ signal is generated by strobing in staus word 8 or 10.

Signal Level Interrupt (RST 7): When the $\overline{\text{INTA}}$ output is tied to 12V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7–D_0) Bus: This bus comprises eight TRI-STATE® input/output lines that connect to the 8080A microprocessor. The bus provides bidirectional communica-

Functional Pin Definitions (Continued)

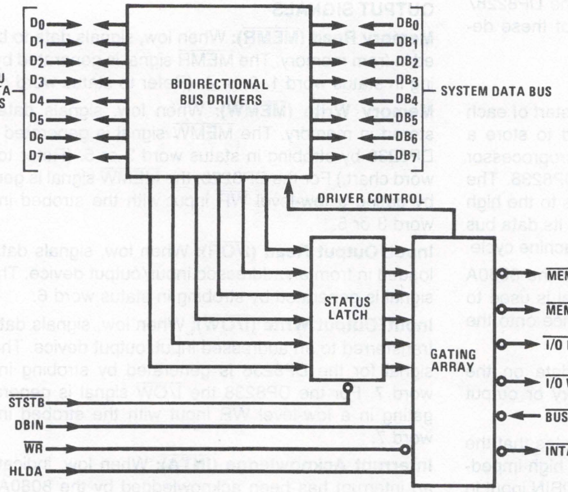
tion between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

System Data (DB_7–DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7–DB_0 Data Bus from the D_7–D_0 Data Bus.

Status Word Chart

Machine Cycle	Status Word	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Control Signal
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{\text{MEMR}}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{\text{MEMR}}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{\text{MEMW}}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{\text{MEMR}}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{\text{MEMW}}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{\text{I/OR}}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{\text{I/OW}}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{\text{INTA}}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{\text{INTA}}$

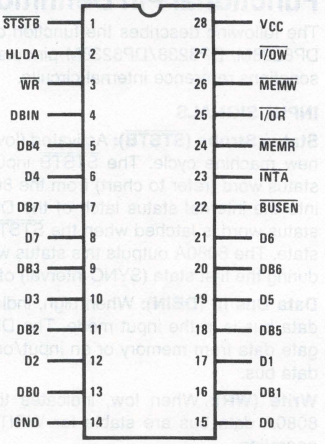
Block and Connection Diagrams



D0
D1
D2
D3
D4
D5
D6
D7
CPU DATA BUS
BIDIRECTIONAL BUS DRIVERS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
SYSTEM DATA BUS
DRIVER CONTROL
STATUS LATCH
GATING ARRAY
MEM R
MEM W
I/O R
I/O W
BUSEN
INTA
STSTB
DBIN
WR
HLDA

TL/F/6825-6

Dual-In-Line Package



STSTB 1
HLDA 2
WR 3
DBIN 4
DB4 5
D4 6
DB7 7
D7 8
DB3 9
D3 10
DB2 11
D2 12
DB0 13
GND 14
28 VCC
27 I/OW
26 MEMW
25 I/OR
24 MEMR
23 INTA
22 BUSEN
21 D6
20 DB6
19 D5
18 DB5
17 D1
16 DB1
15 D0

TL/F/6825-7

Order Number DP8228J, DP8228MJ, DP8228N, DP8238J, DP8238MJ or DP8238N

See NS Package Number J28A or N28B

Section 7

Level Translators and Buffers

Section 7 Contents

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DS78L12/DS88L12 Hex TTL-MOS Inverter/Interface Gate 7-24

National Semiconductor

Level Translators/Buffers

Several different families of logic circuits are available today, each offering advantages in certain applications. This wide selection of circuit types allows the design engineer to more easily construct functions and systems which meet his specific requirements.

Each of these logic "families", however, is produced using different processes, and their specific electrical characteristics are almost always different. Interfacing between these logic families can, at times, be difficult.

National Semiconductor offers a selection of level translators which can greatly simplify this task. The following selection guide outlines the level translator circuits available.

National Semiconductor

Level Translators/Buffers

Device Number		Logic Function	Output Characteristics	Output	Input	Page Number
0°C to +70°C	−55°C to +125°C					
DP8480A		Inverting	TRI-STATE Fall Through Latch	TTL	10k ECL	7-5
DP8481		Inverting	Gated Fall Through Latch	10k ECL	TTL	7-8
DP8482A		Inverting	TRI-STATE Fall Through Latch	TTL	10k ECL	7-11
DP8483		Inverting	Gated Fall Through Latch	100k ECL	TTL	7-14
DS3630	DS1630	Hex Buffer	50 ns Prop. Delay at 500 pF	CMOS	CMOS	7-17
DS8800	DS7800	Dual 2-Input Gate	Open-Collector −30V to 30V	PMOS	TTL	7-21
DS88L12	DS78L12	Hex Inverter	Active Pull-Up 0.4V to 14V	MOS	TTL	7-24
MM74C901	MM54C901	Hex Inverter	Active Pull-Up 0.4V @ 2.6 mA	TTL	CMOS	CMOS
MM74C902	MM54C902	Hex Buffer	Active Pull-Up 0.4V @ 3.2 mA	TTL	CMOS	CMOS
MM74C903	MM54C903	Hex Inverter	Active Pull-Up 0V to 15V	PMOS	CMOS	CMOS
MM74C904	MM54C904	Hex Buffer	Active Pull-Up 0V to 15V	PMOS	CMOS	CMOS
MM74C906	MM54C906	Hex Buffer	Open Drain 0V to 15V	NMOS	CMOS	CMOS
MM74C907	MM54C907	Hex Buffer	Open Drain V_{CC} to V_{CC} − 15V	PMOS	CMOS	CMOS

National Semiconductor

DP8480A 10k ECL to TTL Level Translator with Latch

General Description

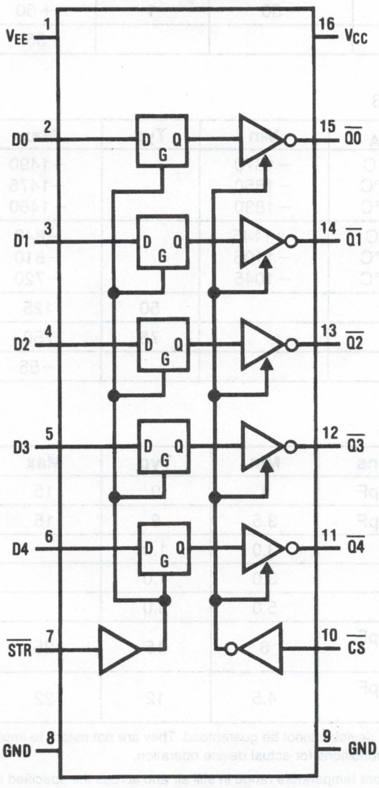
This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 10k ECL input compatible

Logic and Connection Diagram

Dual-In-Line Package



1 V_{EE}
16 V_{CC}
2 D0
15 $\overline{Q0}$
3 D1
14 $\overline{Q1}$
4 D2
13 $\overline{Q2}$
5 D3
12 $\overline{Q3}$
6 D4
11 $\overline{Q4}$
7 $\overline{STR}$
10 $\overline{CS}$
8 GND
9 GND
D Q G

TL/F/5861–1

Top View

Truth Table

D	$\overline{Q}$	STR	$\overline{CS}$
H	L	L	L
L	H	L	L
X	$\overline{Q}$	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8480AF, DP8480AJ or DP8480AN
See NS Package Number F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ± 10%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) Notes 2, 3 and 4

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	V_{CC} −2V			V
I_{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I_{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I_{OZ}	TRI-STATE Output Current		−50	1	+50	μA
I_{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −5.2V	0° C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current	V_{IN} = V_{IL} Max			50	125	μA
I_{IH}	Input High Current	V_{IN} = V_{IH} Max			75	750	μA
I_{EE}	Supply Current					−55	mA

Switching Characteristics Notes 2 and 5

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe to Output Delay	C_L = 50 pF	4	9	15	ns
t_{PD2}	Data to Output Delay	C_L = 50 pF	3.5	8	15	ns
t_S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t_H	Data Hold Time	(Note 6)	3.0	1.0		ns
t_{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF	6	15	25	ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

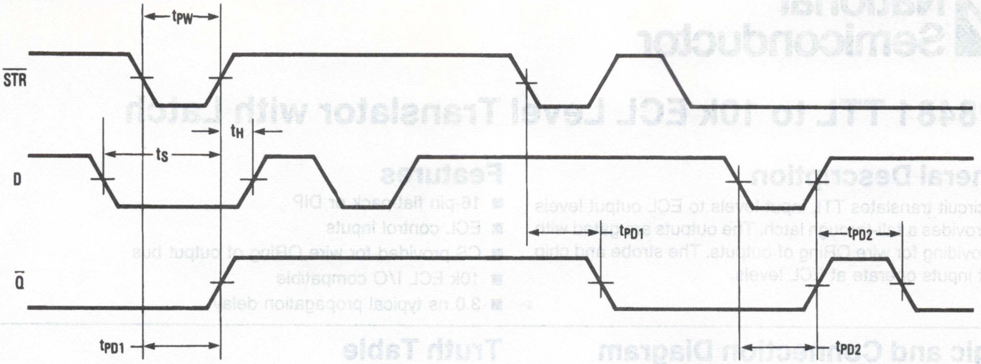
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 MA max.

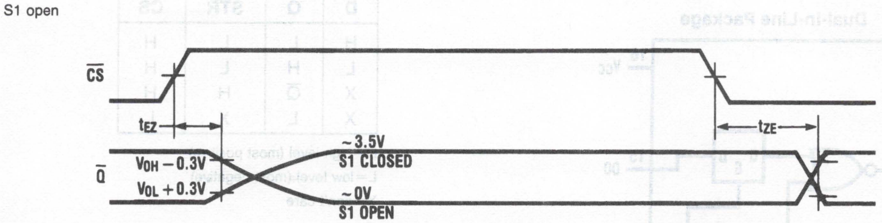
Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 2.0 ns ± 0.2 ns from 20% to 80%.

Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to loose data. Board mounting and good supply decoupling are desirable. The worst case conductions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms

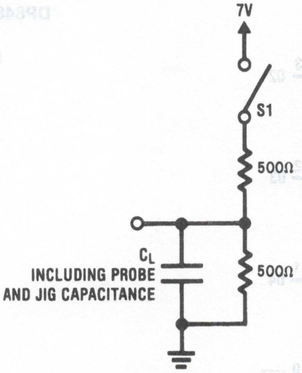

tPW
STR
tH
tS
D
Q̄
tPD1
tPD1
tPD2
tPD2

TL/F/5861-2


S1 open
CS
tEZ
tZE
Q̄
VOH − 0.3V
VOL + 0.3V
~3.5V
S1 CLOSED
~0V
S1 OPEN

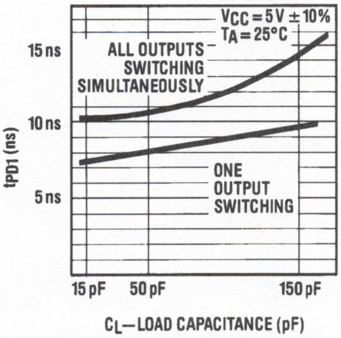
TL/F/5861-3

Test Load

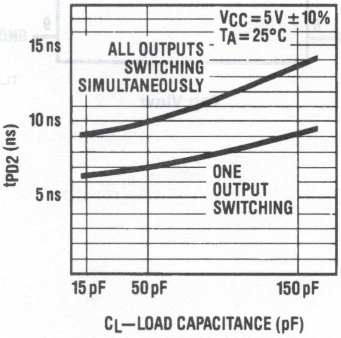

7V
S1
500Ω
500Ω
CL
INCLUDING PROBE
AND JIG CAPACITANCE

TL/F/5861-4

Typical Performance Versus CL



TL/F/5861-5



TL/F/5861-6

National Semiconductor

DP8481 TTL to 10k ECL Level Translator with Latch

General Description

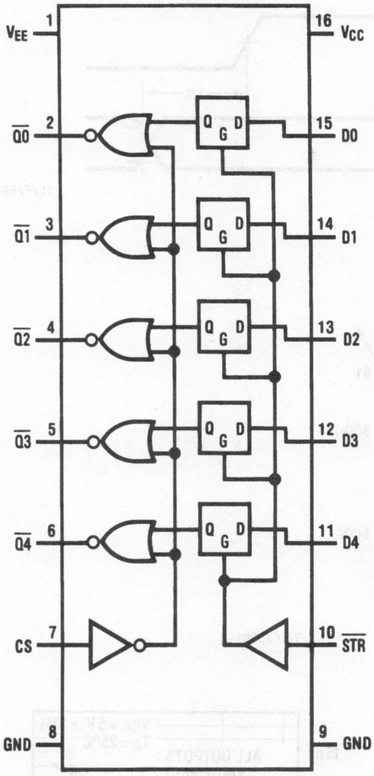
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 10k ECL I/O compatible
- 3.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package



1 V_{EE}
2 $\overline{Q0}$
3 $\overline{Q1}$
4 $\overline{Q2}$
5 $\overline{Q3}$
6 $\overline{Q4}$
7 CS
8 GND
16 V_{CC}
15 D0
14 D1
13 D2
12 D3
11 D4
10 $\overline{STR}$
9 GND
Q D G

TL/F/5862-1

Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	CS
H	L	L	H
L	H	L	H
X	$\overline{Q}$	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number
DP8481F, DP8481J or DP8481N
See NS Package
F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ±10%
V_{CC} Supply Voltage	5.0V ±10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	$V_{IN}=0.5V$		−25	−200	μA
I_{IH}	Input High Current	$V_{IN}=2.5V$		1.0	40	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN}=-12$ mA		−0.9	−1.2	V
I_{CC}	Supply Current	$V_{CC}=5.5V$		10	20	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current	$V_{IN}=-1.8V$			55	150	μA
I_{IH}	Input High Current	$V_{IN}=-0.8V$			85	200	μA
V_{OL}	Output Low Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C	−1870 −1850 −1830		−1665 −1650 −1625	mV
V_{OH}	Output High Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C	−1000 −960 −900		−840 −810 −720	mV
V_{OLC}	Output Low Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C			−1645 −1630 −1605	mV
V_{OHC}	Output High Voltage	$V_{EE}=-5.2V$	0°C 25°C 75°C	−1020 −980 −920			mV
I_{EE}	Supply Current	$V_{EE}=-5.7V$			−70	−90	mA

Switching Characteristics (Notes 2 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe To Output Delay		1.5	3.0	6.0	ns
t_{PD2}	Data To Output Delay		2.5	4.5	7.5	ns
t_S	Data Set-Up Time to Strobe		5.0	2.0		ns
t_H	Data Hold Time		1.0	0		ns
t_{PW}	Strobe Pulse Width		5.0	3.0		ns
t_{PD3}	Chip Select to Output Delay		1.0	2.5	4.0	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

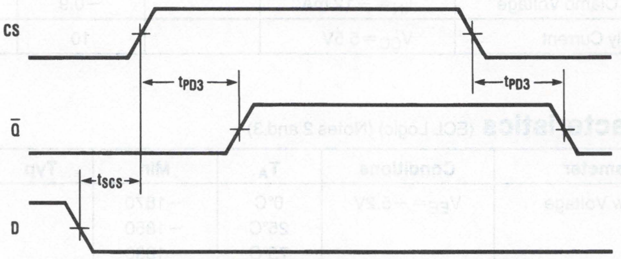
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

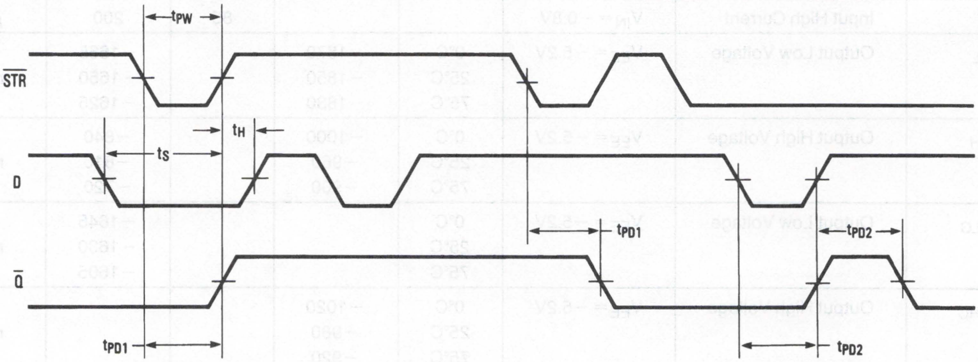
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 2.0 ns ±0.2 ns from 20% to 80%. TTL input characteristic is 0V to 3V with $t_r = t_f \le 3$ ns measured from 10% to 90%.

Switching Time Waveforms



TL/F/5862-2



TL/F/5862-3

National Semiconductor

DP8482A 100k ECL to TTL Level Translator with Latch

General Description

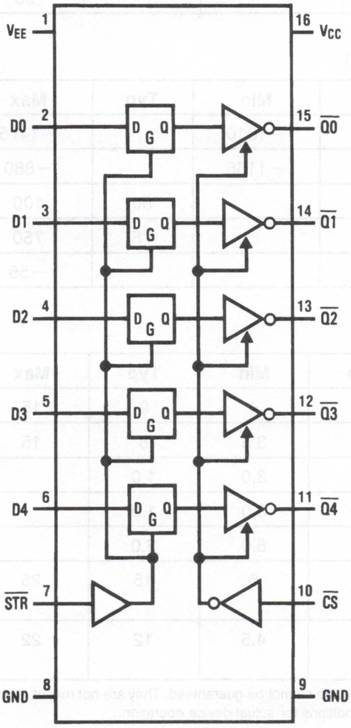
This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 100k ECL input compatible

Logic and Connection Diagram

Dual-In-Line Package



1 V_{EE}
2 D0
3 D1
4 D2
5 D3
6 D4
7 $\overline{STR}$
8 GND
16 V_{CC}
15 $\overline{Q0}$
14 $\overline{Q1}$
13 $\overline{Q2}$
12 $\overline{Q3}$
11 $\overline{Q4}$
10 $\overline{CS}$
9 GND
D G Q

TL/F/5863–1

Top View

Truth Table

D	$\overline{Q}$	STR	CS
H	L	L	L
L	H	L	L
X	$\overline{Q}$	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8482AF, DP8482AJ or DP8482AN
See NS Package Number F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V ± 7%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA			0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -10$ mA	$V_{CC} - 2$V			V
I_{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I_{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I_{OZ}	TRI-STATE Output Current		−50	1	+50	µA
I_{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	$V_{EE} = -4.5$V		−1810		−1475	mV
V_{IH}	Input High Voltage	$V_{EE} = -4.5$V		−1165		−880	mV
I_{IL}	Input Low Current	$V_{IN} = V_{IL}$ Max			50	100	µA
I_{IH}	Input High Current	$V_{IN} = V_{IH}$ Max			75	750	µA
I_{EE}	Supply Current					−55	mA

Switching Characteristics (Notes 2 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe to Output Delay	$C_L = 50$ pF	4	9	15	ns
t_{PD2}	Data to Output Delay	$C_L = 50$ pF	3.5	8	15	ns
t_S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t_H	Data Hold Time	(Note 6)	3.0	1.0		ns
t_{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	$C_L = 50$ pF	6	15	25	ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	$C_L = 50$ pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for $T_A = 25$°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

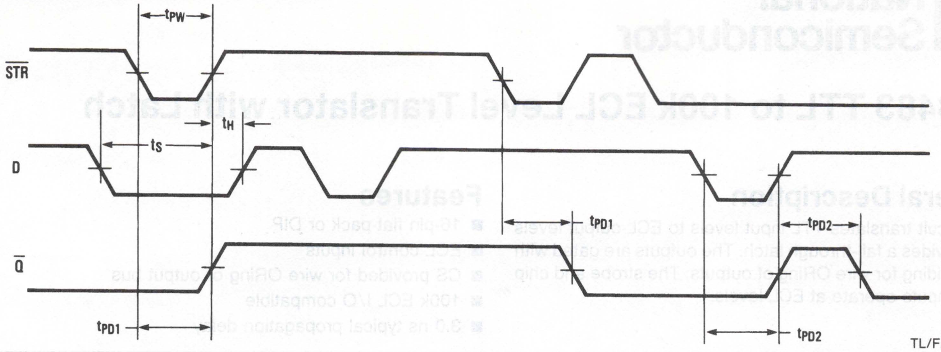
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 mA max.

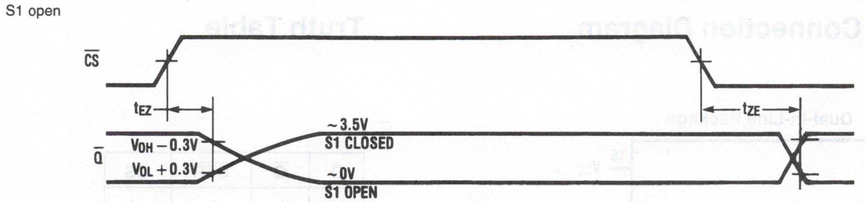
Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%.

Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to lose data. Board mounting and good supply decoupling are desirable. The worst case conditions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms

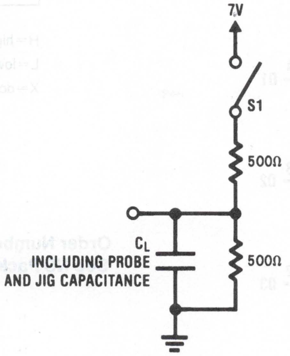

tPW
STR
tH
tS
D
tPD1
tPD2
Q
tPD1
tPD2

TL/F/5863-2


S1 open
CS
tEZ
tZE
Q
VOH − 0.3V
VOL + 0.3V
~3.5V
S1 CLOSED
~0V
S1 OPEN

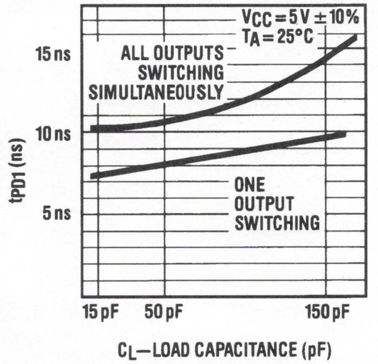
TL/F/5863-3

Test Load

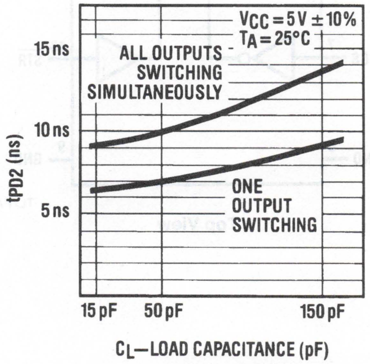

7V
S1
500Ω
CL
INCLUDING PROBE
AND JIG CAPACITANCE
500Ω

TL/F/5863-4

Typical Performance Versus C_L



TL/F/5863-5



TL/F/5863-6

National Semiconductor

DP8483 TTL to 100k ECL Level Translator with Latch

General Description

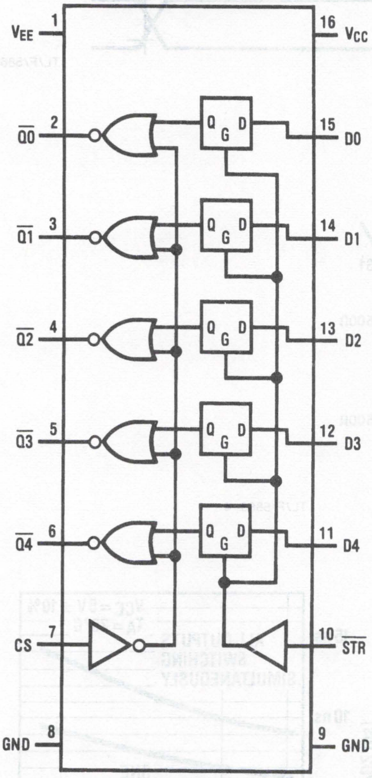
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 100k ECL I/O compatible
- 3.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package


V_{EE} 1
16 V_{CC}
$\overline{Q0}$ 2
15 D0
$\overline{Q1}$ 3
14 D1
$\overline{Q2}$ 4
13 D2
$\overline{Q3}$ 5
12 D3
$\overline{Q4}$ 6
11 D4
Q G D
CS 7
10 $\overline{STR}$
GND 8
9 GND

TL/F/5864-1

Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	CS
H	L	L	H
L	H	L	H
X	$\overline{Q}$	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8483F, DP8483J or DP8483N
See NS Package Number F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V +7%
V_{CC} Supply Voltage	5.0V ±10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	$V_{IN}=0.5V$		−25	−200	μA
I_{IH}	Input High Current	$V_{IN}=2.5V$		1.0	40	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN}=-12$ mA		−0.9	−1.2	V
I_{CC}	Supply Current	$V_{CC}=5.5V$		10	20	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	$V_{EE}=-4.5V$	−1810		−1475	mV
V_{IH}	Input High Voltage	$V_{EE}=-4.5V$	−1165		−880	mV
I_{IL}	Input Low Current	$V_{IN}=-1.8V$		45	150	μA
I_{IH}	Input High Current	$V_{IN}=-0.8V$		75	200	μA
V_{OL}	Output Low Voltage	$V_{EE}=-4.5V$	−1810	−1705	−1620	mV
V_{OH}	Output High Voltage	$V_{EE}=-4.5V$	−1025	−955	−880	mV
V_{OLC}	Output Low Voltage	$V_{EE}=-4.5V$			−1610	mV
V_{OHC}	Output High Voltage	$V_{EE}=-4.5V$	−1035			mV
I_{EE}	Supply Current	$V_{EE}=-4.8V$		−65	−85	mA

Switching Characteristics (Notes 2 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe To Output Delay	(Note 4)	1.5	3.0	6.0	ns
t_{PD2}	Data To Output Delay		2.5	4.5	7.5	ns
t_S	Data Set-Up Time to Strobe		5.0	2.0		ns
t_H	Data Hold Time		1.0	0		ns
t_{PW}	Strobe Pulse Width		5.0	3.0		ns
t_{PD3}	Chip Select to Output Delay		1.0	2.5	4.0	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

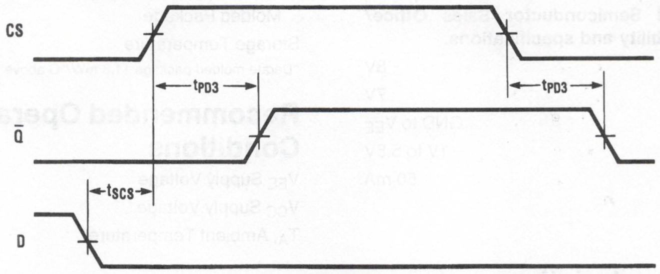
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

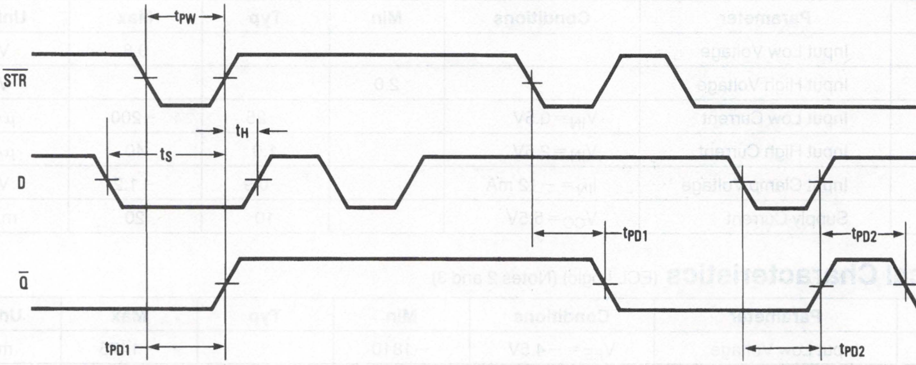
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 0.7 ns ±0.1 ns from 20% to 80%. TTL input characteristics is 0V to 3V with $t_r=t_f\leq 3$ ns measured from 10% to 90%.

Switching Time Waveforms


CS
tPD3
tPD3
Q̄
tSCS
D

TL/F/5864-2


tPW
STR
tH
tS
D
tPD1
tPD2
Q̄
tPD1
tPD2

TL/F/5864-3

National Semiconductor

DS1630B/DS3630B Hex CMOS Compatible Buffer

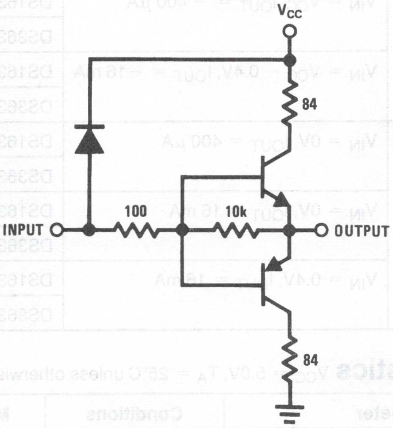
General Description

The DS1630B/DS3630B is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630B/DS3630B features low quiescent power consumption (typically 50 μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630B/DS3630B is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

Features

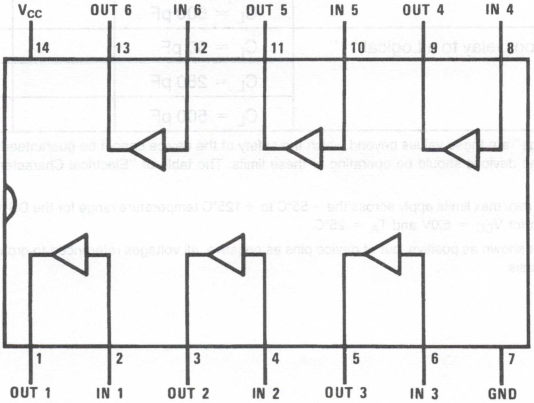
- High-speed capacitive driver
- Wide supply voltage range
- Input/output may interface to TTL
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50 μW typical standby power

Equivalent Schematic and Connection Diagrams



TL/F/5826–1

Dual-In-Line Package



TL/F/5826–2

Top View

Order Number DS1630BJ, DS3630BJ or DS3630BN
See NS Package Number J14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630B	−55	+125	°C
DS3630B	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{INH}	Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\ \mu A$	DS1630B		90	200	μA
			DS3630B		90	200	μA
		$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16\ mA$	DS1630B		0.5	6.4	mA
			DS3630B		0.5	4.0	mA
I_{INL}	Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16\ mA$	DS1630B		−0.15	2.0	mA
			DS3630B		$V_{CC} - 150$	1.3	mA
V_{OH}	Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\ \mu A$	DS1630B	$V_{CC} - 1$	$V_{CC} - 0.75$		V
			DS3630B	$V_{CC} - 0.9$	$V_{CC} - 0.75$		V
		$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = -16\ mA$	DS1630B	$V_{CC} - 2.5$	$V_{CC} - 2.0$		V
			DS3630B	$V_{CC} - 2.5$	$V_{CC} - 2.0$		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\ \mu A$	DS1630B		0.75	1	V
			DS3630B		0.75	0.9	V
		$V_{IN} = 0V$, $I_{OUT} = 16\ mA$	DS1630B		0.95	1.3	V
			DS3630B		0.95	1.3	V
		$V_{IN} = 0.4V$, $I_{OUT} = 16\ mA$	DS1630B		1.2	1.6	V
			DS3630B		1.2	1.5	V

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0"	$C_L = 50\ pF$		30	45	ns
		$C_L = 250\ pF$		40	60	ns
		$C_L = 500\ pF$		50	75	ns
t_{pd1}	Propagation Delay to a Logical "1"	$C_L = 50\ pF$		15	25	ns
		$C_L = 250\ pF$		35	50	ns
		$C_L = 500\ pF$		50	75	ns

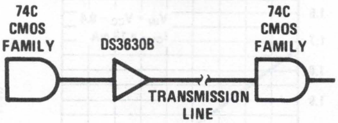
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for 'Operating Temperature Range' they are not meant to imply that the devices should be operating at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630B and across the 0°C to +70°C range for the DS3630B. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

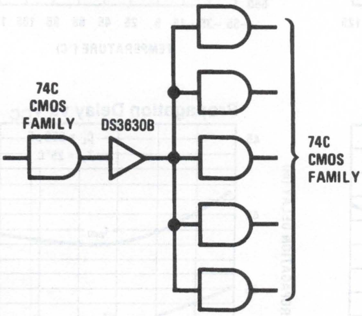
Typical Applications

CMOS to Transmission Line Interface


74C
CMOS
FAMILY
DS3630B
74C
CMOS
FAMILY
TRANSMISSION
LINE

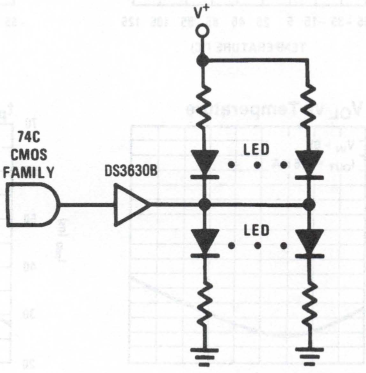
TL/F/5826-3

CMOS to CMOS Interface


74C
CMOS
FAMILY
DS3630B
74C
CMOS
FAMILY

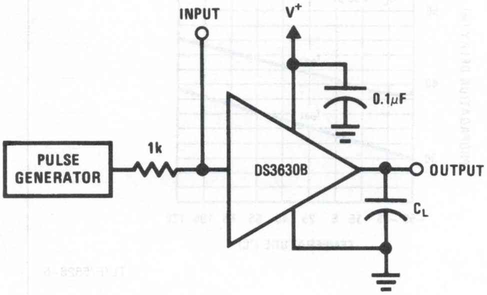
TL/F/5826-4

LED Driver


V^+
74C
CMOS
FAMILY
DS3630B
LED
LED

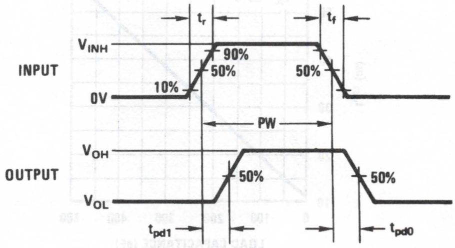
TL/F/5826-5

AC Test Circuit and Switching Time Waveforms


INPUT
V^+
0.1μF
PULSE
GENERATOR
1k
DS3630B
OUTPUT
C_L

TL/F/5826-7

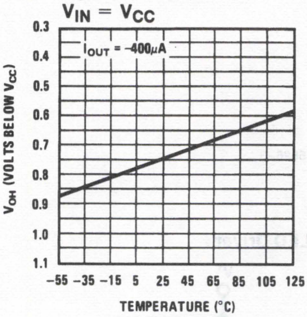
C_L includes probe and jig capacitance


t_r
t_f
V_{INH}
INPUT
0V
90%
50%
10%
50%
PW
V_{OH}
OUTPUT
V_{OL}
50%
50%
t_{pd1}
t_{pd0}

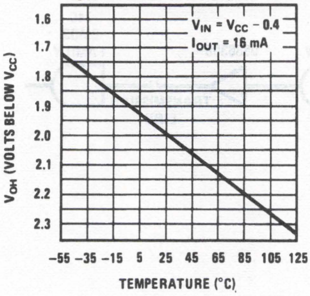
TL/F/5826-8

Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, $V_{IN} = 0$ to V_{CC}

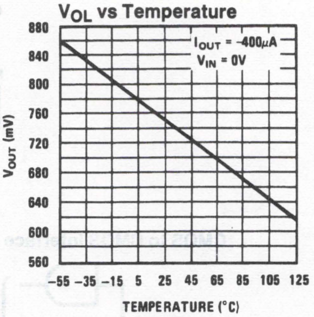
Typical Performance Characteristics



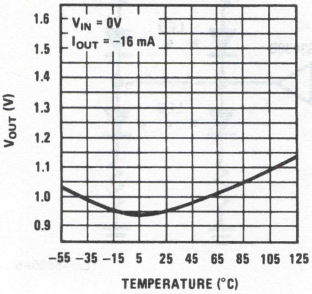
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



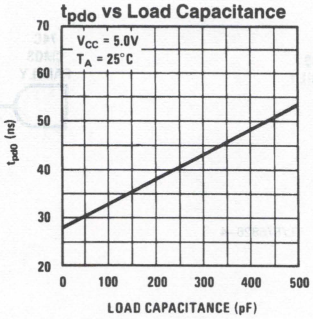
V_{OH} Active vs Temperature



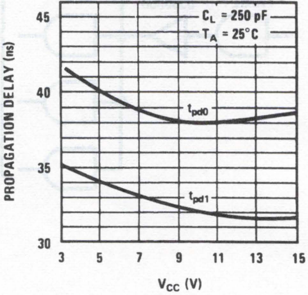
V_{OL} vs Temperature



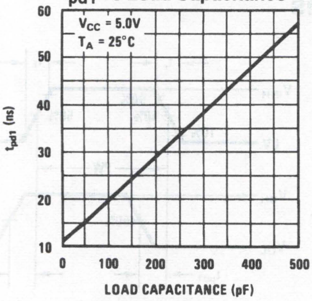
V_{OL} vs Temperature



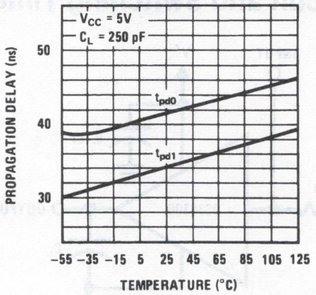
t_{pdo} vs Load Capacitance



Propagation Delay vs V_{CC}



t_{pd1} vs Load Capacitance



Propagation Delay vs Temperature

TL/F/5826-6

National Semiconductor

DS7800/DS8800 Dual Voltage Level Translator

General Description

The DS7800/DS8800 are dual voltage translators designed for interfacing between conventional TTL or LS voltage levels and those levels associated with high impedance junction or MOS REF-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

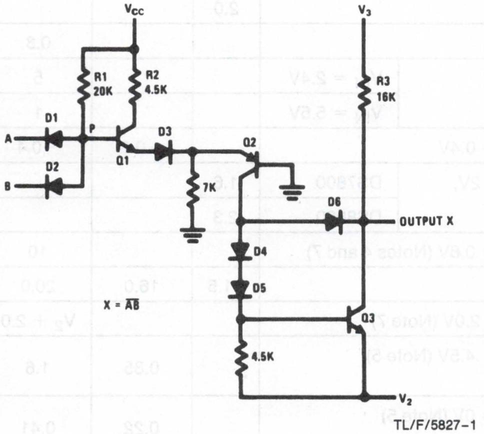
Features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:

DS7800	−55°C to +125°C
DS8800	0°C to +70°C

- Compatible with all MOS devices

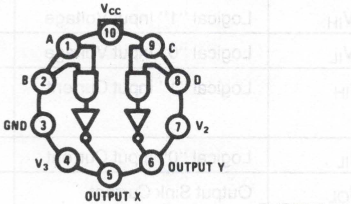
Schematic and Connection Diagrams



V_{CC}
R1 20K
R2 4.5K
R3 16K
V_3
D1
A
P
Q1
D3
Q2
D2
B
7K
D6
OUTPUT X
D4
D5
X = $\overline{AB}$
Q3
4.5K
V_2

TL/F/5827–1

Metal Can Package



V_{CC}
10
A 1
9 C
B 2
8 D
GND 3
7 V_2
V_3 4
6 OUTPUT Y
5
OUTPUT X

TL/F/5827–2

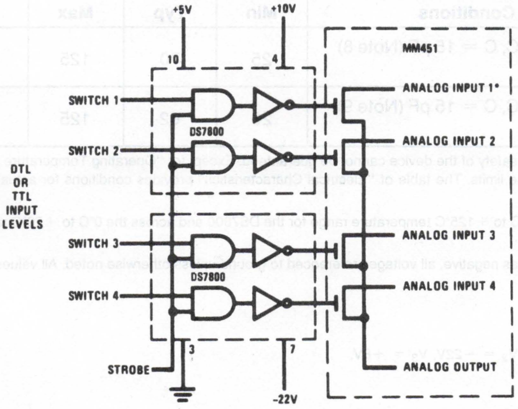
Top View

Order Number DS7800H or DS8800H

See NS Package Number H10C

Typical Applications

4-Channel Analog Switch

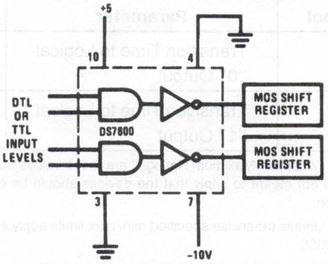


+5V
+10V
10
4
MM451
SWITCH 1
ANALOG INPUT 1*
DS7800
SWITCH 2
ANALOG INPUT 2
DTL OR TTL INPUT LEVELS
SWITCH 3
ANALOG INPUT 3
DS7800
SWITCH 4
ANALOG INPUT 4
3
7
STROBE
ANALOG OUTPUT
−22V

TL/F/5827–3

*Analog signals within the range of +8V to −8V.

Bipolar to MOS Interfacing



+5
10
4
DTL OR TTL INPUT LEVELS
DS7800
MOS SHIFT REGISTER
MOS SHIFT REGISTER
3
7
−10V

TL/F/5827–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Supply Voltage	7.0V
V2 Supply Voltage	−30V
V3 Supply Voltage	30V
V3−V2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C Metal Can (TO-5) Package	690 mW

*Derate metal can package 4.6 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T_A)			
DS7800	−55	+125	°C
DS8800	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			5	µA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.2	−0.4	mA
I_{OL}	Output Sink Current	V_{CC} = Min, V_{IN} = 2V,	DS7800	1.6			mA
		V3 Open	DS8800	2.3			mA
I_{OH}	Output Leakage Voltage	V_{CC} = Max, V_{IN} = 0.8V (Notes 4 and 7)				10	µA
R_O	Output Collector Resistor	T_A = 25°C		11.5	16.0	20.0	kΩ
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V (Note 7)				$V_2 + 2.0$	V
$I_{CC(MAX)}$	Power Supply Current Output "ON" Per Gate	V_{CC} = Max, V_{IN} = 4.5V (Note 5)			0.85	1.6	mA
$I_{CC(MIN)}$	Power Supply Current Output "OFF" Per Gate	V_{CC} = Max, V_{IN} = 0V (Note 5)			0.22	0.41	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Transition Time to Logical "0" Output	T_A = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t_{pd1}	Transition Time to Logical "1" Output	T_A = 25°C, C = 15 pF (Note 9)	25	62	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Current measured is drawn from V_3 supply.

Note 5: Current measured is drawn from V_{CC} supply.

Note 6: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.

Note 7: Specification applies for all allowable values of V_2 and V_3.

Note 8: Measured from 1.5V on input to 50% level on output.

Note 9: Measured from 1.5V on input to logic "0" voltage, plus 1V.

Theory of Operation

The two input diodes perform the AND function on TTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL, the interfacing with these types of circuits is achieved.

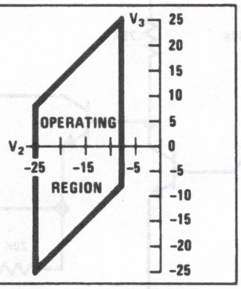
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2.

Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3. Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the ouput voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

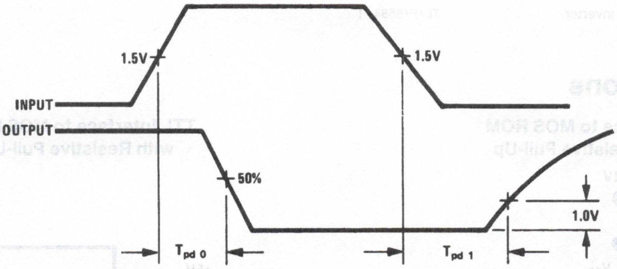
Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



TL/F/5827-5

Switching Time Waveforms



TL/F/5827-6

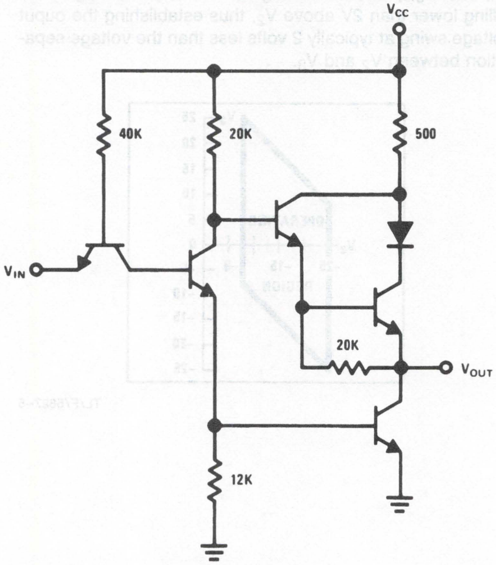
National Semiconductor

DS78L12/DS88L12 Hex TTL-MOS Inverter/Interface Gate

General Description

The DS78L12/DS88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200 μA.

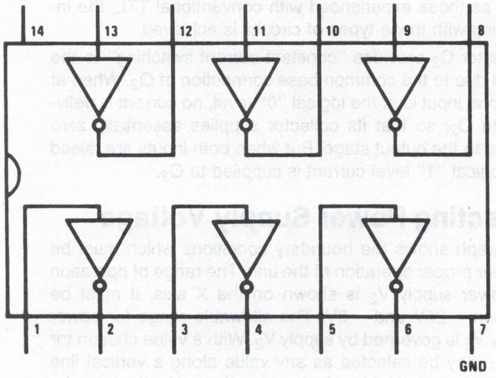
Schematic and Connection Diagrams


VCC
40K
20K
500
VIN
20K
VOUT
12K

Note: Shown is schematic for each inverter.

TL/F/8584–1

Dual-In-Line Package


VCC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND

TL/F/8584–2

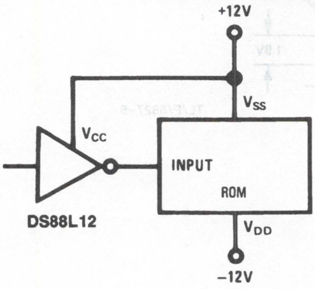
Top View

Order Number DS78L12J, DS88L12J, DS88L12N and DS78L12W

See NS Package Number J14A, N14A or W14B

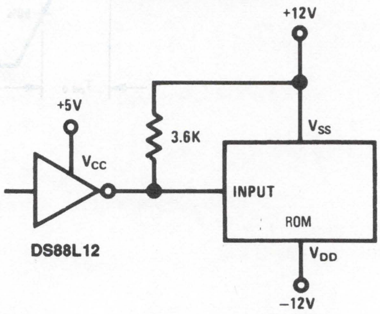
Typical Applications

TTL Interface to MOS ROM without Resistive Pull-Up


+12V
VSS
VCC
INPUT
ROM
DS88L12
VDD
−12V

TL/F/8584–3

TTL Interface to MOS ROM with Resistive Pull-Up


+12V
+5V
3.6K
VSS
VCC
INPUT
ROM
DS88L12
VDD
−12V

TL/F/8584–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS78L12	4.5	5.5	V
DS88L12	4.75	5.25	V
Temperature (T_A)			
DS78L12	−55	125	°C
DS88L12	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	$V_{CC} = 14.0V$		2.0	1.3		V
		$V_{CC} = \text{Min}$		2.0	1.3		V
V_{IL}	Logical "0" Input Voltage	$V_{CC} = 14.0V$			1.3	0.7	V
		$V_{CC} = \text{Min}$			1.3	0.7	V
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.7V$	$V_{CC} = 14.0V$, $I_{OUT} = -200\ \mu A$	11.8	12.0		V
			$V_{CC} = \text{Min}$, $I_{OUT} = -200\ \mu A$	14.5	15.0		V
		$V_{IN} = 0V$, $V_{CC} = \text{Min}$, $I_{OUT} = -5.0\ \mu A$ (Note 6)					V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 2.0V$	$V_{CC} = 14.0V$, $I_{OUT} = 12$ mA		0.5	1.0	V
			$V_{CC} = \text{Min}$, $I_{OUT} = 3.6$ mA		0.2	0.4	V
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$	$V_{CC} = 14.0V$		<1	20	µA
			$V_{CC} = \text{Max}$		<1	10	µA
		$V_{IN} = 5.5V$	$V_{CC} = 14.0V$		<1	100	µA
			$V_{CC} = \text{Max}$		<1	100	µA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$	$V_{CC} = 14.0V$		−320	−500	µA
			$V_{CC} = \text{Max}$		−100	−180	µA
I_{SC}	Output Short Circuit Current	$V_{OUT} = 0V$ (Note 4)	$V_{CC} = 14.0V$	−10	−25	−50	mA
			$V_{CC} = \text{Max}$	−3	−8	−15	mA
I_{CCH}	Supply Current—Logical "1" (Each Inverter)	$V_{IN} = 0V$	$V_{CC} = 14.0V$		0.32	0.50	mA
			$V_{CC} = \text{Max}$		0.11	0.16	mA
I_{CCL}	Supply Current—Logical "0" (Each Inverter)	$V_{IN} = 5.25V$	$V_{CC} = 14.0V$		1.0	1.5	mA
			$V_{CC} = \text{Max}$		0.3	0.5	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	$T_A = 25°C$	$V_{CC} = 5.0V$ *(Figure 2)*		27	45	ns
			$V_{CC} = 14.0V$ *(Figure 1)*		11	20	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	$T_A = 25°C$	$V_{CC} = 5.0V$ *(Figure 2)*, (Note 5)		79	100	ns
			$V_{CC} = 14.0V$ *(Figure 1)*		34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78L12 and across the 0°C to +70°C range for the DS88L12.

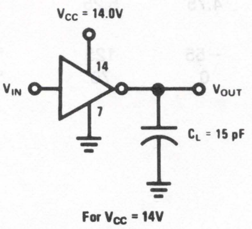
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: t_{pd1} for $V_{CC} = 5.0V$ is dependent upon the resistance and capacitance used.

Note 6: $V_{OH} = V_{CC} - 1.1V$ for the DS88L12 and $V_{CC} - 1.4V$ for the DS78L12.

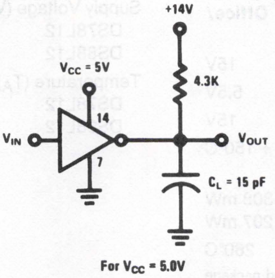
AC Test Circuits



V_{CC} = 14.0V
14
7
V_{IN}
V_{OUT}
C_L = 15 pF
For V_{CC} = 14V

TL/F/8584-5

FIGURE 1

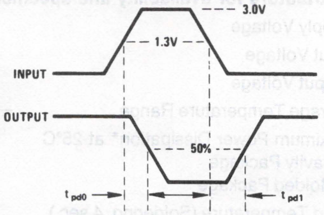


+14V
4.3K
V_{CC} = 5V
14
7
V_{IN}
V_{OUT}
C_L = 15 pF
For V_{CC} = 5.0V

TL/F/8584-6

FIGURE 2

Switching Time Waveforms



3.0V
1.3V
INPUT
OUTPUT
50%
t_{pd0}
t_{pd1}

TL/F/8584-7

f = 1 MHz
$t_r = t_f$ = 10 ns
PW = 100 ns

Section 8

Frequency Synthesis

Section 8 Contents

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Frequency Synthesis—Selection Guide 8-5
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National Semiconductor

Frequency Synthesis

Frequency synthesis is the process of generating a multitude of different frequencies from one reference frequency. A common application where the frequency synthesis concept is used is in electronically tuned radios and televisions.

Digital tuning systems are fast replacing the conventional mechanical systems in AM, FM and television receivers. The digital approach encompasses the following operational features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power-on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large-scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive.

The heart of any digital tuning system is, of course, the phase locked loop (PLL) synthesizer. The basic subcomponents of a digital system are: a voltage controlled oscillator (VCO), a phase comparator and some programmable and fixed dividers. The PLL's basic function is to take two input signals and match them as illustrated in *Figure 1.* The output of the phase comparator of the PLL is an error signal which is filtered and fed back to the VCO as a DC control voltage. The DC control voltage adjusts the VCO until it causes the phase comparator's two inputs to match one another.

The weak point of this simple illustration is that many PLLs are fabricated using MOS processes which make them relatively incapable of receiving high frequency signals. In fact, state-of-the-art microCMOS devices are usually limited to 100 MHz operation. Even the FM band exceeds this limitation. As a result, a prescaler is almost always used in PLL tuning applications such as FM radios, police scanning radios, aircraft radios, etc. The prescaler is specifically designed to divide high frequency AC input signals down to a usable frequency for the PLL. The prescaler becomes an extension of the PLL's programmable counter as illustrated in *Figure 2.*

For less sophisticated tuning applications, a fixed division prescaler will make the VCO signal palatable to the PLL and be sufficient for general tuning characteristics. However, in some applications, a fixed division prescaler can cause significant undesirable side effects such as:

1. Increased channel spacing (step size) at the output of the PLL's counter; or
2. A forced decrease of the fixed oscillator reference frequency in order to obtain specific channel spacing which can lead to
    A. increased lock-on time,
    B. decreased scanning rates, and
    C. sidebands at undesirable frequencies.

AN-335 in this section explains in detail how these two shortcomings of fixed division prescaling are alleviated by using a dual modulus prescaler. A dual modulus prescaler is substituted for the fixed prescaler and is controlled by programmable counters in the dual modulus PLL, as illustrated by the dotted line in *Figure 2.*

In order to address the requirements of digital frequency synthesis applications, National has introduced a growing family of PLL synthesizers and prescalers. The DS8906, DS8907 and DS8908 are complete PLL synthesizers with features that go beyond those illustrated in *Figure 2.*

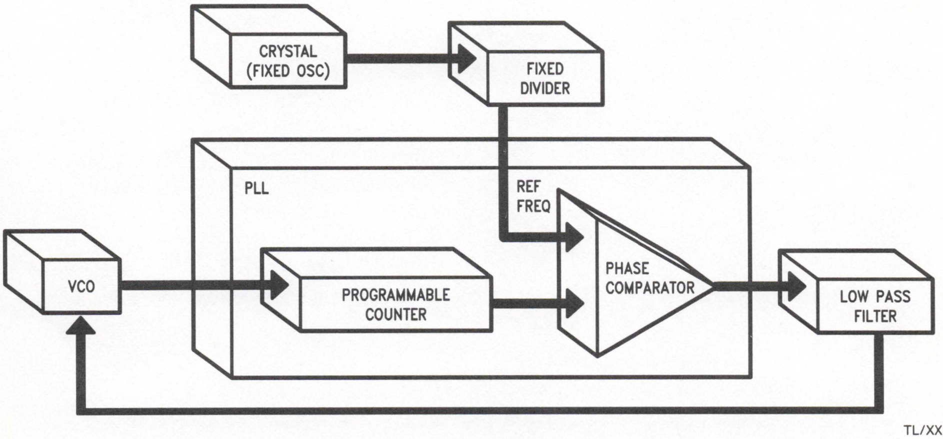
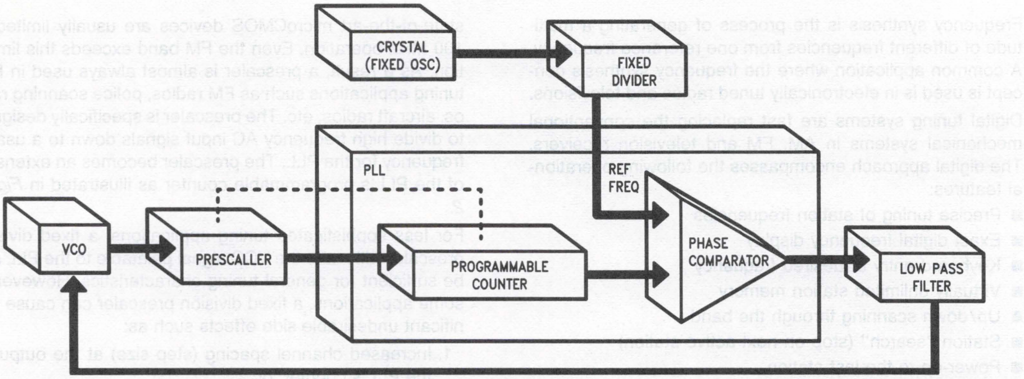


FIGURE 1

Highlights

- The DS8908 integrates a reference oscillator, phase comparator, charge pump, operational amplifier, 120 MHz ECL/I^{2}L dual modulus programmable divider, and a shift register/latch for serial data entry.
- The DS8614, DS8615, DS8616, DS8617, DS8627, and DS8628 represent a broad family of single and dual modulus prescalers for use in conjunction with other manufacturers' NMOS or CMOS PLLs. These low-power/high-speed prescalers are available with division ratios ranging from a fixed ÷20 up to a dual modulus ÷64/65. This array of products allows for the choice of a division ratio which is virtually tailored to the speed and tuning requirements of a particular frequency synthesis application.


CRYSTAL (FIXED OSC)
FIXED DIVIDER
PLL
REF FREQ
VCO
PRESCALLER
PROGRAMMABLE COUNTER
PHASE COMPARATOR
LOW PASS FILTER

TL/XX/0108-2

FIGURE 2

National Semiconductor

Frequency Synthesizers Selection Guide

PLL FREQUENCY SYNTHESIZERS

Product Type	Frequency Bands	Power (mA)	Tuning Resolution	Page No.
DS8906	AM/FM	160	500 Hz/12.5 kHz	8-19
DS8907	AM/FM	160	10 Hz/25 kHz	8-26
DS8908	AM/FM	160	1 kHz,9 kHz,10 kHz, 20 kHz	8-32
DS8911	AM/FM/VHF TV	35	FM; 10, 12.5, 25, 100 kHz AM; 1, 1.25, 2.5, 10 kHz	8-40
AN-335 Digital PLL Synthesis				8-49

HIGH FREQUENCY PRESCALERS

Product Type	Divide Modulus	Power (mA)	f_{MAX}	Page No.
Single (Fixed) Modulus Dividers				
DS8627	÷24	7/10	130/225 MHz	8-10
DS8628	÷20	7/10	130/225 MHz	8-10
DS8629	÷100	135	30/120 MHz	8-13
Dual-Modulus Dividers				
DS8614	÷20/21	7/10	130/225 MHz	8-6
DS8615	÷32/33	7/10	130/225 MHz	8-6
DS8616	÷40/41	7/10	130/225 MHz	8-6
DS8617	÷64/65	7/10	130/225 MHz	8-6

National Semiconductor

DS8614/DS8615/DS8616/DS8617 130/225 MHz Low Power Dual Modulus Prescalers

General Description

The DS8614 series products are low power dual modulus prescalers which divide by 20/21, 32/33, 40/41, and 64/65, respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40/100 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products can be operated from either an unregulated 5.5V to 13.5V source or regulated 5V ±10% source. Unregulated operation is obtained by connecting V_S to the source with V_{REG} open. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

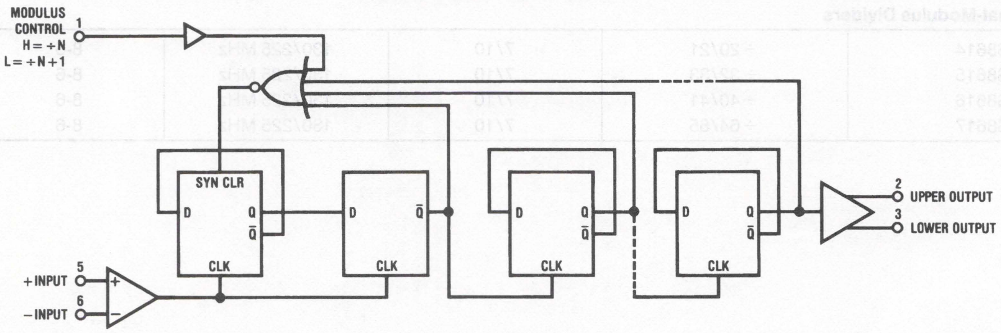
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4); 225 MHz (-2)
- Low power: 10 mA (-4, -2)
- Input sensitivity: 100 mVrms (-4); 40 mVrms (-2)
- Pin compatible with Motorola MC12015-17 prescalers
- Unregulated/regulated power supply option

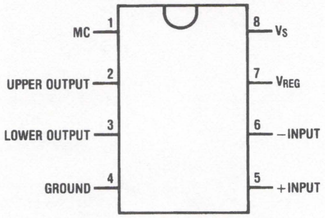
Logic and Connection Diagrams

Generalized ÷ N/N + 1



TL/F/5240–1

Dual-In-Line Package



TL/F/5240–2

Top View

Order Number DS8614N, DS8615N, DS8616N or DS8617N (-4, -2)
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_S, Unregulated Supply Voltage	15V
V_{REG}, Regulated Supply Voltage	7V
Modulus Control Input Voltage	7V
Open-Collector Output Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-2 DS8615-2 DS8616-2 DS8617-2		Units
			Min	Max	Min	Max	
V_S	Unregulated Supply Voltage	V_{REG} = Open	6.8	13.5	5.5	13.5	V
V_{REG}	Regulated Supply Voltage	V_S and V_{REG} Shorted	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130		225	MHz
V_{IN}	Input Signal Amplitude		100	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		V/μs
I_{OH}	High Level Output Current			−400		−400	μA
I_{OL}	Low Level Output Current			2.0		2.0	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-2 DS8615-2 DS8616-2 DS8617-2		Units
			Min	Max	Min	Max	
V_{IH}	High Level MC Input Voltage	V_S = 13.5V, V_{REG} = Open	2.0		2.0		V
V_{IL}	Low Level MC Input Voltage	V_{REG} = V_S = 4.5V		0.8		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, Pins 2 and 3 Shorted	V_{REG} −2		V_{REG} −2		V
I_{CEX}	Open-Collector High Level Output	Lower Output = 5.5V		100		100	μA
V_{OL}	Low Level Output Voltage	V_{REG} = 4.5V, I_{OL} = 2 mA		0.5		0.5	V
I_I	Max MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IH} = 7V		100		100	μA
I_{IH}	High Level MC Input Current	V_{REG} = 4.5V, V_{IH} = 2.7V		20		20	μA
I_{IL}	Low Level MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IL} = 0.4V		−200		−200	μA
I_S	Supply Current, Unregulated Mode	V_S = 13.5V, V_{REG} = Open		10		10	mA
I_{REG}	Supply Current, Regulated Mode	V_S = V_{REG} = 5.5V		10		10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −30°C to +70°C range.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as Max or Min on absolute value basis.

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $T_A = -30°C$ to $+70°C$

Symbol	Parameter		Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-Up Time (Notes 4 and 5)	DS8614			55	ns
		DS8615, DS8616			65	ns
		DS8617			75	ns
R_{IN}	AC Input Resistance		V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		V_{IN} = 100 MHz and 50 mVrms	3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

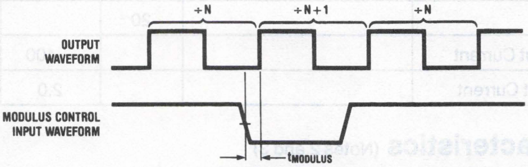
Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescaler output to ensure proper modulus selection.

Note 5: See Timing Diagrams.

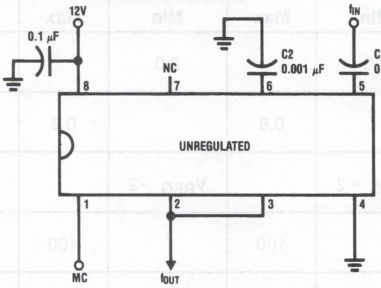
Timing Diagram


÷N
÷N+1
÷N
OUTPUT WAVEFORM
MODULUS CONTROL INPUT WAVEFORM
$t_{MODULUS}$

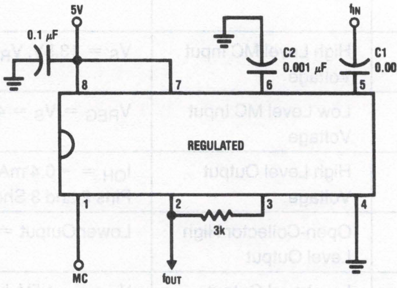
TL/F/5240-3

The logical state of the modulus control input just prior to the output's rising edge will determine the modulus ratio of the device immediately following that rising edge. The pulse width difference of N and N + 1 operation occurs during the output = HI conditions.

Typical Applications

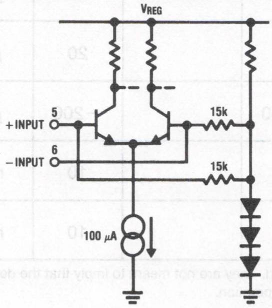

12V
0.1 µF
NC
C2 0.001 µF
f_{IN}
C1 0.001 µF
8
7
6
5
UNREGULATED
1
2
3
4
MC
f_{OUT}

TL/F/5240-4

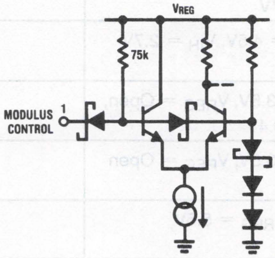

5V
0.1 µF
C2 0.001 µF
f_{IN}
C1 0.001 µF
8
7
6
5
REGULATED
1
2
3
4
3k
MC
f_{OUT}

TL/F/5240-5

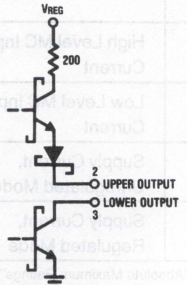
Schematic Diagrams


V_{REG}
5
+INPUT
6
−INPUT
15k
15k
100 µA

TL/F/5240-6


V_{REG}
75k
1
MODULUS CONTROL

TL/F/5240-7


V_{REG}
200
2
UPPER OUTPUT
LOWER OUTPUT
3

TL/F/5240-8

Application Hints

OPERATING NOTES

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pulldown resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

For regulated mode operation connect V_S to V_{REG} to ensure proper operation (see Typical Application diagram).

National Semiconductor

DS8627/DS8628 130/225 MHz Low Power Prescalers

General Description

The DS8627 and DS8628 are low power fixed ratio prescalers which divide by 24 and 20, respectively. The inputs can be driven either single or double-ended and they are buffered, providing 40/100 mVrms input sensitivity. The output provided is open-collector and is capable of interfacing with TTL and CMOS.

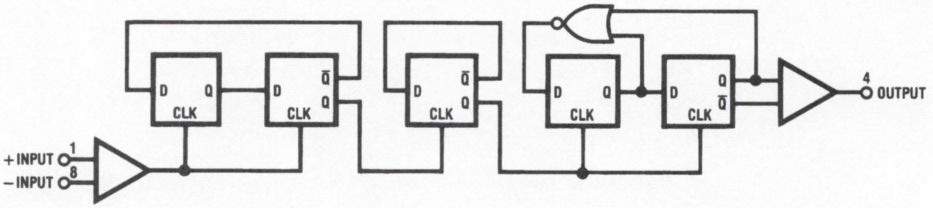
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4, -3); 225 mHz (-2, std)
- Low power: 10 mA (-4, -2); 7 mA (-3, std)
- Input sensitivity: 100 mVrms (-4, -3); 40 mVrms (-2, std)

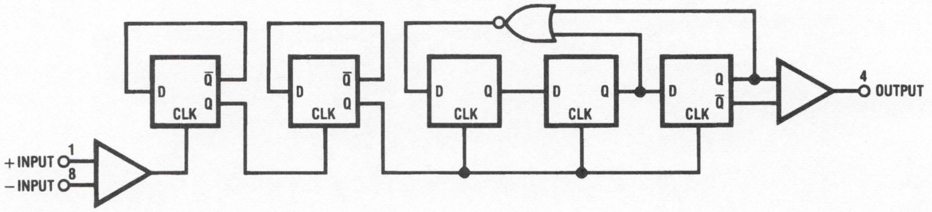
Logic and Connection Diagrams

DS8627 (÷ 24)


D
Q
CLK
$\overline{Q}$
+INPUT
−INPUT
1
8
4
OUTPUT

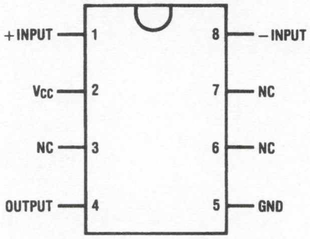
TL/F/5009–1

DS8628 (÷ 20)


D
Q
CLK
$\overline{Q}$
+INPUT
−INPUT
1
8
4
OUTPUT

TL/F/5009–2

Dual-In-Line Package


+INPUT 1
V_{CC} 2
NC 3
OUTPUT 4
8 −INPUT
7 NC
6 NC
5 GND

TL/F/5009–3

Top View

Order Number DS8627N or DS8628N (-4, -3, -2)

See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Supply Voltage 7V

V_{IN} Input Voltage $< V_{CC}$

Open-Collector Output Voltage 7V

Operating Free Air Temperature Range −30°C to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130	20	130	20	225	20	225	MHz
V_{IN}	Input Signal Amplitude		100	300	100	300	40	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		20		20		V/μs
I_{OL}	Low Level Output Current			3		3				3	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CEX}	Open-Collector High Level Output	Output = 5.5V		100		100		100		100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 3 mA		0.4		0.4		0.4		0.4	V
I_{CC}	Supply Current	V_{CC} = 5.5V		10		7		10		7	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
R_{IN}	AC Input Resistance	V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

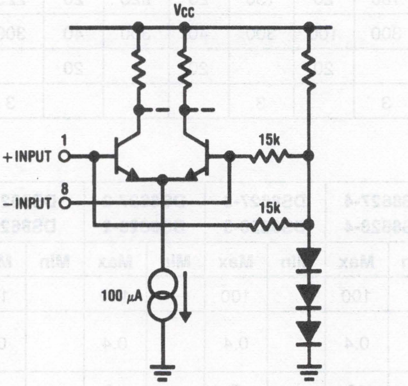
Application Hints

OPERATING NOTES

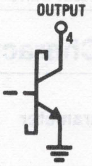
The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

Schematic Diagrams

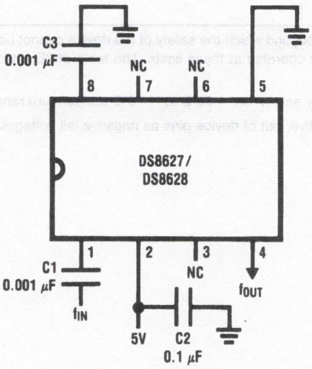


TL/F/5009-4



TL/F/5009-5

Typical Application



TL/F/5009-6

National Semiconductor

DS8629 120 MHz Divide-by-100 Prescaler

General Description

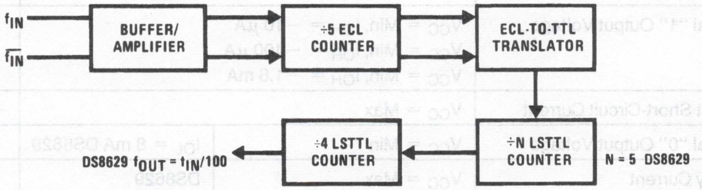
The DS8629 is a fixed ratio counter combining ECL and Low Power Schottky technology on a single monolithic substrate. This provides high frequency capability and TTL compatibility. A single 5.2V ±10% supply is needed.

The device can be operated in a single-ended or differential input mode, with the signal source typically capacitively coupled to the input. An input amplifier is included to allow use of extremely small amplitude, high frequency signals. The output of the device is a square wave of frequency $f_{OUT} = f_{IN}/100$ for the DS8629. The output is standard Low Power Schottky.

Features

- High Frequency, dc—120 MHz—small input amplitude
- Sine wave input 30 MHz $< f_{IN} <$ 120 MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ±10%
- Single ended or differential input modes
- Positive or negative-edge triggered
- Count down sequence avoids broadcast FM IF harmonics

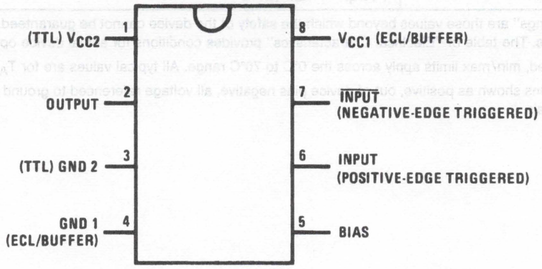
Logic and Connection Diagrams



f_{IN}
$\overline{f_{IN}}$
BUFFER/ AMPLIFIER
÷5 ECL COUNTER
ECL-TO-TTL TRANSLATOR
÷N LSTTL COUNTER
N = 5 DS8629
÷4 LSTTL COUNTER
DS8629 $f_{OUT} = f_{IN}/100$

TL/F/7539–1

Dual-In-Line Package



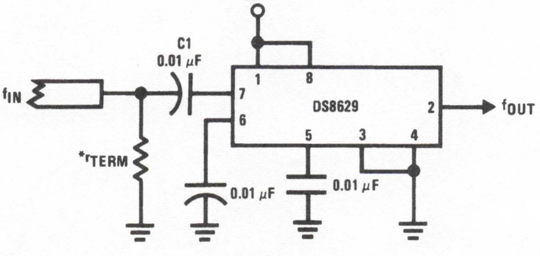
(TTL) V_{CC2} 1
OUTPUT 2
(TTL) GND 2 3
GND 1 (ECL/BUFFER) 4
8 V_{CC1} (ECL/BUFFER)
7 $\overline{INPUT}$ (NEGATIVE-EDGE TRIGGERED)
6 INPUT (POSITIVE-EDGE TRIGGERED)
5 BIAS

TL/F/7539–2

Order Number DS8629N
See NS Package Number N08E

Typical Applications

High Frequency—Single-Ended Input



5.2V
C1
0.01 µF
f_{IN}
*r_{TERM}
DS8629
1
8
7
6
5
3
4
2
f_{OUT}
0.01 µF
0.01 µF

TL/F/7539–3

*r_{TERM} is the termination impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.68	5.72	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN1(p-p)}$	Input Voltage (Peak-To-Peak)	Single-Ended @ 120 MHz	200		1000	mV
$V_{IN2(p-p)}$	Input Voltage (Peak-To-Peak)	Differential @ 120 MHz	100		1000	mV
f_{SINE}	Input Frequency with Sine Wave	V_{IN} = 600 mVp-p	30		120	MHz
f_{TTL}	Input Frequency with TTL Input		0		120	MHz
dv	Minimum Slew Rate of Square Wave Input	V_{IN} = 600 mVp-p			100	V/µs
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OH} = −10 µA V_{CC} = Min, I_{OH} = −400 µA V_{CC} = Min, I_{OH} = −1.6 mA	2.9 2.4 2.0			V V V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max	−10		−40	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min I_{OL} = 8 mA DS8629			0.5	V
I_{CC}	Supply Current	V_{CC} = Max DS8629		90	135	mA
Z_{IN}	Input Impedance	V_{IN} = 0.1 V_{p-p} to 1 V_{p-p} Freq. = 120 MHz	100	200	350	Ω

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 70°C range. All typical values are for T_A = 25°C and V_{CC} = 5.2V.

Note 3: All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Application Hints

OPERATING NOTES

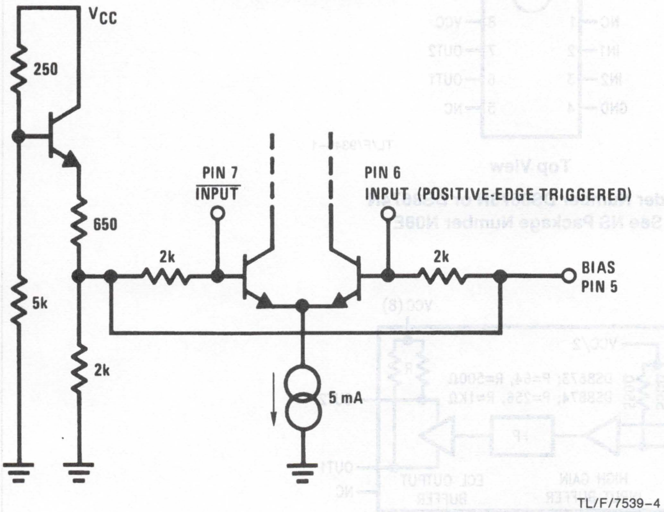
Two ground and two V_{CC} connections are provided separating the ECL and buffer/amplifier stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds externally to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimize stray inductance. A well by-passed voltage source should be used.

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.01 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

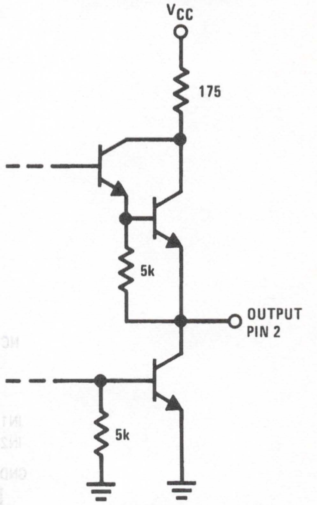
The input waveform may be sinusoidal, but below about 30 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 100 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided. If it is desired to use a TTL input signal source, the unused input should have a 10 kΩ resistor added to ground and the input coupling capacitor should be eliminated with the TTL source dc coupled to the input.

The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 160 MHz (typically).

Input Configuration



Output Configuration



TL/F/7539-5

National Semiconductor

DS8673/DS8674 Low Power VHF/UHF Prescalers

General Description

The DS8673 and DS8674 products are low power prescalers which divide by 64 and 256 respectively. The devices are used in frequency synthesis applications such as TV/CATV, cellular phone, and instrumentation to divide a very high frequency down to a frequency usable by low power MOS PLL's.

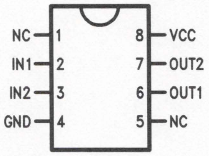
The devices have differential buffered inputs and complementary ECL outputs. The inputs provide high input sensitivity and good isolation. The DS8673 is pin compatible with Plessey's SP4531, SP4632, and Motorola's MC12073 products. The DS8674 is pin compatible with Plessey's SP4653 and Motorola's MC12074 products.

Features

- 1.0 GHz operating frequency
- 25 mA typical supply current
- 20 mV rms input sensitivity
- 0.8V complementary ECL outputs
- Low output radiation

Block and Connection Diagrams

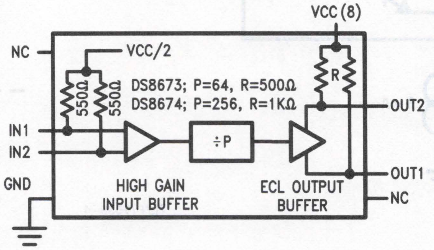
Dual-In-Line Package


NC 1
IN1 2
IN2 3
GND 4
8 VCC
7 OUT2
6 OUT1
5 NC

TL/F/9340–1

Top View

Order Number DS8673N or DS8674N
See NS Package Number N08E


VCC (8)
NC
VCC/2
550Ω
550Ω
DS8673; P=64, R=500Ω
DS8674; P=256, R=1KΩ
R
IN1
IN2
÷P
OUT2
OUT1
GND
HIGH GAIN INPUT BUFFER
ECL OUTPUT BUFFER
NC

TL/F/9340–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	V_{CC} + 0.5V
Operating Free Air Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

ESD rating is to be determined.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		4.5		5.5	V
F_{IN}	Input Frequency Range	V_{IN} Min	80		1,000	MHz
V_{IN}	Input Sensitivity into 50Ω	80 MHz	20		200	mV rms
		300 MHz	20		200	
		500 MHz	20		200	
		700 MHz	20		200	
		1 GHz	20		200	

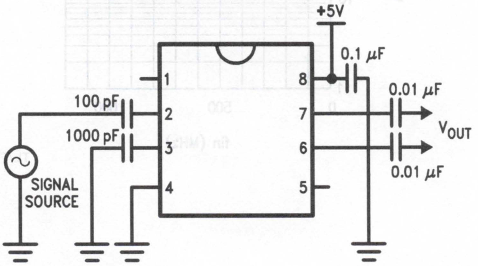
DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = 5.5V		25	35	mA
V_{OUT}	Output Voltage Swing	Peak-to-Peak (no load)	0.8	1.2	1.6	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Typical Applications

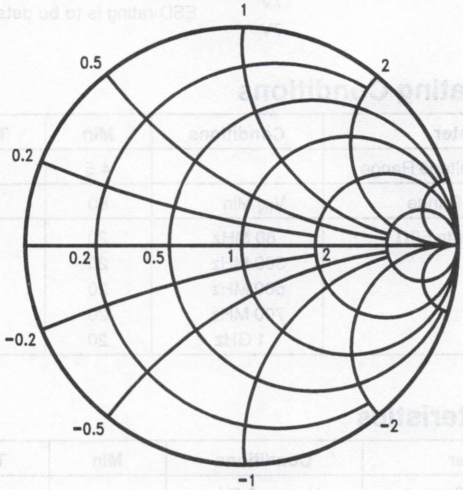
Typical Wiring Configuration



TL/F/9340-3

Typical Applications (Continued)

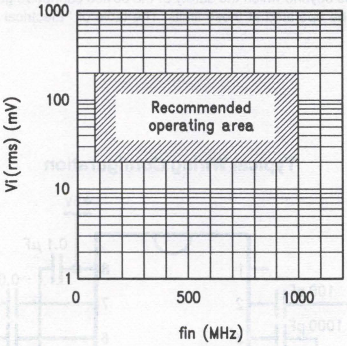
Typical Input Impedance



Reference value = 50Ω
Vi (rms) = 25 mV
V_{CC} = 5V
Waveshape is TBD

TL/F/9340-4

Typical Sensitivity Curve Under Nominal Conditions



TL/F/9340-5

National Semiconductor

DS8906 AM/FM Digital Phase-Locked Loop Synthesizer

General Description

The DS8906 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^{2}L dual modulus programmable divider, and a 20-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 12.5 kHz reference signal for FM and a 500 Hz reference signal for AM/SW. One of these reference signals is selected by the data from the controller for use by the phase comparator. Additional dividers are used to generate a 50 Hz timing signal used by the controller for "time-of-day".

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 22-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 20-bit data word, the next 14-bits are used for the PLL divide code. The remaining 6 bits are connected via latches to output pins. These 6 bits can be used to drive radio functions such as gain, mute, FM, AM, LW and SW only. These outputs are open collector. Bit 18 is used internally to select the AM or FM local oscillator input and to select between the 500 Hz and 12.5 kHz reference. A high level at bit 18 indicates FM and a low level indicates AM.

The PLL consists of a 14-bit programmable I^{2}L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–14 after address). It is clocked by the AM input via an ECL ÷ 7/8 prescaler, or through a ÷ 63/64 prescaler from the FM input. The AM input will work at frequencies up to 8 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 500 Hz and the FM band is tuned with a resolution of 12.5 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO thru a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator.

The high speed charge pump consists of a switchable constant current source (−0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high.

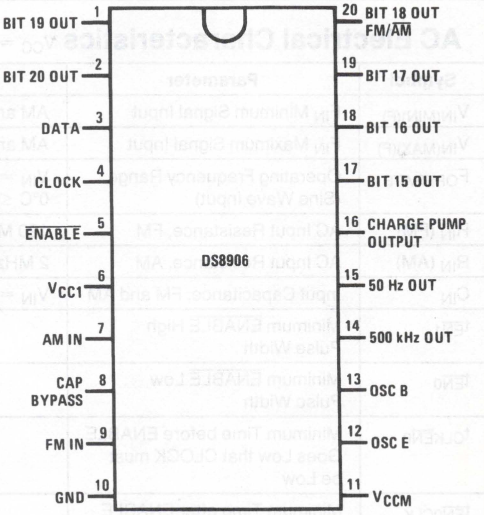
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 12.5 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for "time-of-day" reference with separate low power supply (V_{CCM})
- 6-open collector buffered outputs for band switching and other radio functions
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis

Connection Diagram

Dual-In-Line Package



TL/F/5775–1

Top View

Order Number DS8906N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	$V_{IN} = V_{CC1}$			0	10	µA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock and $\overline{\text{ENABLE}}$ INPUTS, $V_{IN} = 0V$			−5	−25	µA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	$V_{OH} = 5.25V$				50	µA
	500 kHz Output	$V_{OH} = 2.4V$, $V_{CCM} = 4.5V$				−250	µA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	$I_{OL} = 5$ mA				0.5	V
	50 Hz Output, 500 kHz Output	$I_{OL} = 250$ µA				−0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Output Current	$1.2V \leq V_{OUT} \leq V_{CCM} - 1.2V$ $V_{CCM} \leq 6.0V$	Pump Up	−0.10	−0.30	−0.6	mA
			Pump Down	0.10	0.30	0.6	mA
			TRI-STATE®		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, $V_{CC1} = 5.25V$, All Other Pins Open			2.5	6.0	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	$V_{IN} = 100$ mV rms $0°C \leq T_A \leq 70°C$	AM FM	0.4 60		8 120	MHz MHz
R_{IN} (FM)	AC Input Resistance, FM	120 MHz, $V_{IN} = 100$ mV rms		300			Ω
R_{IN} (AM)	AC Input Resistance, AM	2 MHz, $V_{IN} = 100$ mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	$V_{IN} = 120$ MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{\text{ENABLE}}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before ENABLE Goes Low that CLOCK must be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after ENABLE Goes Low that CLOCK must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High that Last Positive CLOCK Edge May Occur				300	600	ns

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

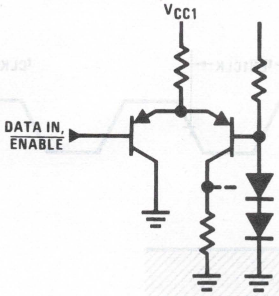
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time Before CLOCK that DATA Must be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time After CLOCK that DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

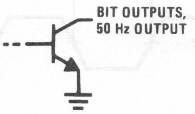
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8906.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

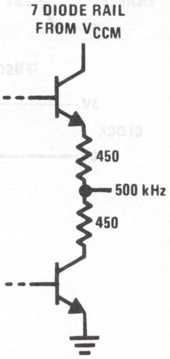
Schematic Diagrams (DS8906 AM/FM PLL Typical Input/Output Schematics)


V_{CC1}
DATA IN, $\overline{\text{ENABLE}}$

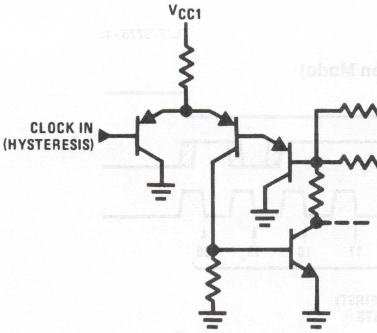
TL/F/5775-2


BIT OUTPUTS, 50 Hz OUTPUT

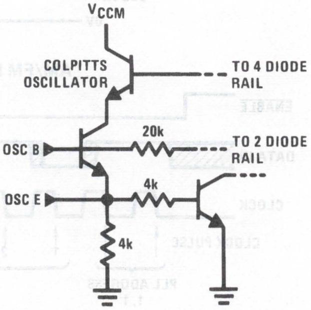
TL/F/5775-3


7 DIODE RAIL FROM V_{CCM}
450
500 kHz
450

TL/F/5775-4

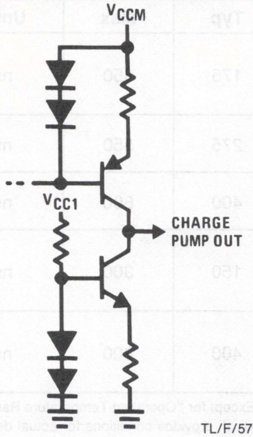

V_{CC1}
V_{CC1}
CLOCK IN (HYSTERESIS)

TL/F/5775-5

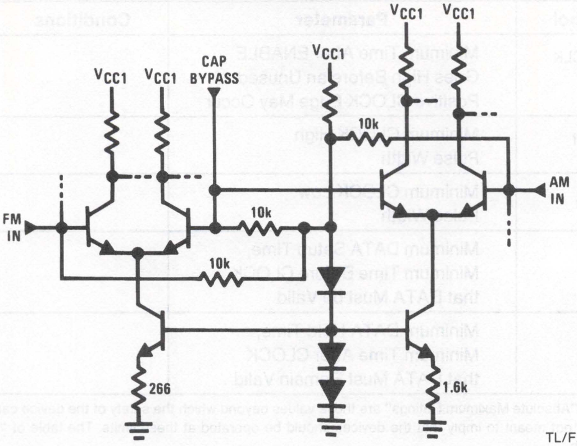

V_{CCM}
COLPITTS OSCILLATOR
TO 4 DIODE RAIL
OSC B
20k
TO 2 DIODE RAIL
OSC E
4k
4k

TL/F/5775-6

Schematic Diagrams (DS8906 AM/FM PLL Typical Input/Output Schematics) (Continued)


V_{CCM}
V_{CC1}
CHARGE PUMP OUT

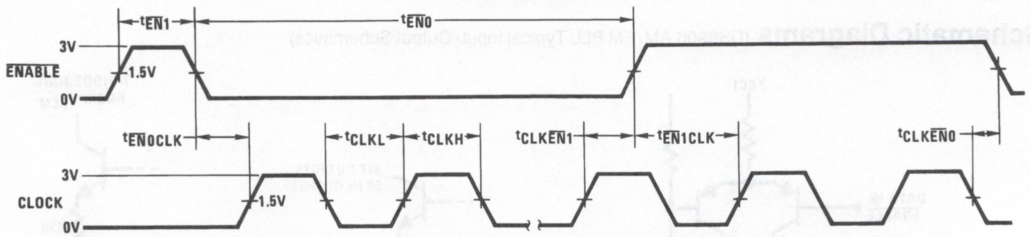
TL/F/5775-7


V_{CC1}
V_{CC1}
V_{CC1}
V_{CC1}
V_{CC1}
CAP BYPASS
10k
AM IN
FM IN
10k
10k
266
1.6k

TL/F/5775-8

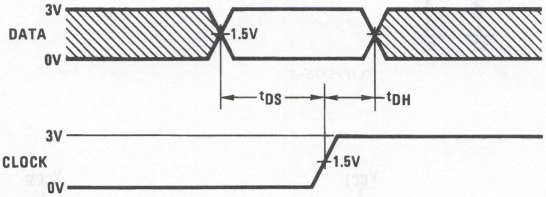
Timing Diagrams*

$\overline{\text{ENABLE}}$ vs CLOCK


tEN1
tEN0
3V
ENABLE
1.5V
0V
tEN0CLK
tCLKL
tCLKH
tCLKEN1
tEN1CLK
tCLKEN0
3V
CLOCK
1.5V
0V

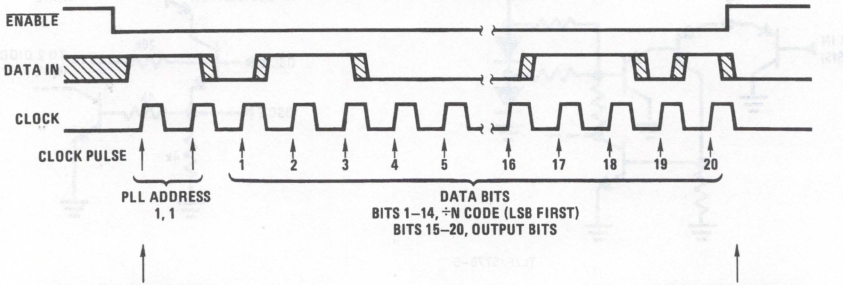
TL/F/5775-9

CLOCK vs DATA


3V
DATA
1.5V
0V
tDS
tDH
3V
CLOCK
1.5V
0V

TL/F/5775-10

AM/FM Frequency Synthesizer (Scan Mode)


ENABLE
DATA IN
CLOCK
CLOCK PULSE
1
2
3
4
5
16
17
18
19
20
PLL ADDRESS
1, 1
DATA BITS
BITS 1–14, ÷N CODE (LSB FIRST)
BITS 15–20, OUTPUT BITS

NEGATIVE TRANSITION ON $\overline{\text{ENABLE}}$ CLEARS PREVIOUS ADDRESS. CLOCK MUST BE LOW DURING TRANSITION.

POSITIVE TRANSITION ON $\overline{\text{ENABLE}}$ LATCHES IN NEW CODE IF PLL IS ADDRESSED.

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

TL/F/5775-11

Applications Information

SERIAL DATA ENTRY INTO THE DS8906

Serial information entry into the DS8906 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first 2 bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1, *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first 2 bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any *data* bits preceding the 20th to last bit will be shifted out, and are thus irrelevant. Data bits are counted as any bits following 2 valid (1,1) address bits with the $\overline{\text{ENABLE}}$ low.

When the $\overline{\text{ENABLE}}$ input returns high, any further serial data input is inhibited. Upon this positive transition of the $\overline{\text{ENABLE}}$, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

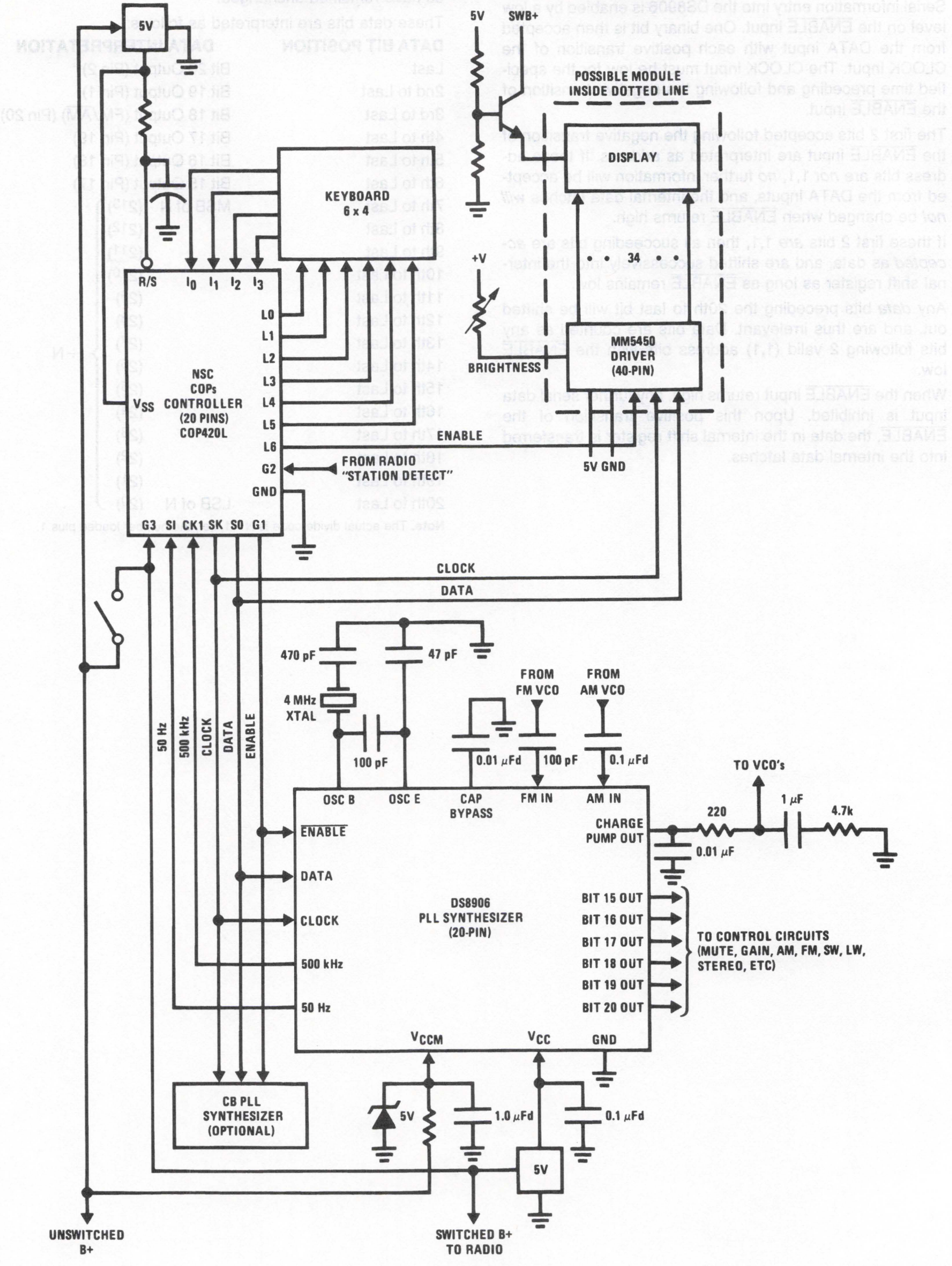
These data bits are interpreted as follows:

DATA BIT POSITION	DATA INTERPRETATION	
Last	Bit 20 Output (Pin 2)	
2nd to Last	Bit 19 Output (Pin 1)	
3rd to Last	Bit 18 Output (FM/$\overline{\text{AM}}$) (Pin 20)	
4th to Last	Bit 17 Output (Pin 19)	
5th to Last	Bit 16 Output (Pin 18)	
6th to Last	Bit 15 Output (Pin 17)	
7th to Last	MSB of N (2^{13})	
8th to Last	(2^{12})	
9th to Last	(2^{11})	
10th to Last	(2^{10})	
11th to Last	(2^{9})	
12th to Last	(2^{8})	
13th to Last	(2^{7})	
14th to Last	(2^{6})	÷N
15th to Last	(2^{5})	
16th to Last	(2^{4})	
17th to Last	(2^{3})	
18th to Last	(2^{2})	
19th to Last	(2^{1})	
20th to Last	LSB of N (2^{0})	

Note. The actual divide code is N + 1, i.e., the number loaded plus 1.

Typical Application

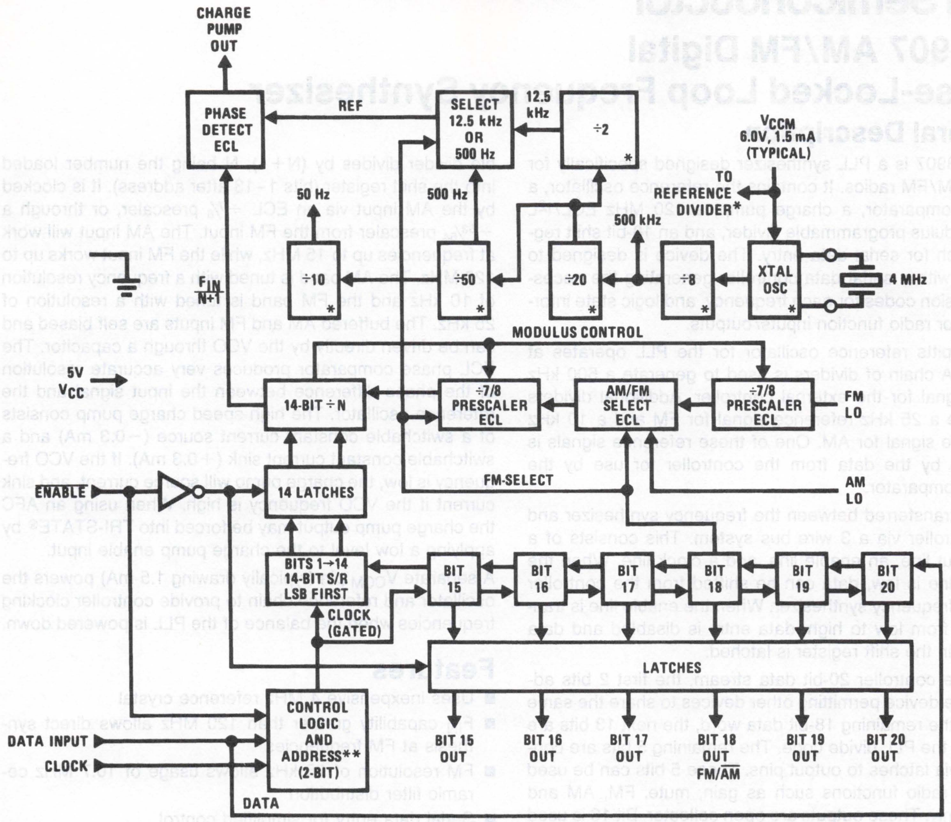
Electronically Tuned Radio Controller System; Direct Drive LED


5V
R/S
I_0 I_1 I_2 I_3
KEYBOARD 6 x 4
L0
L1
L2
L3
L4
L5
L6
G2
GND
NSC COPs CONTROLLER (20 PINS) COP420L
V_{SS}
G3 SI CK1 SK S0 G1
ENABLE
FROM RADIO "STATION DETECT"
5V
SWB+
+V
BRIGHTNESS
POSSIBLE MODULE INSIDE DOTTED LINE
DISPLAY
34
MM5450 DRIVER (40-PIN)
5V GND
CLOCK
DATA
50 Hz
500 kHz
CLOCK
DATA
ENABLE
470 pF
47 pF
4 MHz XTAL
100 pF
FROM FM VCO
FROM AM VCO
0.01 μFd
100 pF
0.1 μFd
TO VCO's
OSC B
OSC E
CAP BYPASS
FM IN
AM IN
CHARGE PUMP OUT
220
1 μF
4.7k
0.01 μF
ENABLE
DATA
CLOCK
500 kHz
50 Hz
DS8906 PLL SYNTHESIZER (20-PIN)
BIT 15 OUT
BIT 16 OUT
BIT 17 OUT
BIT 18 OUT
BIT 19 OUT
BIT 20 OUT
TO CONTROL CIRCUITS (MUTE, GAIN, AM, FM, SW, LW, STEREO, ETC)
V_{CCM}
V_{CC}
GND
CB PLL SYNTHESIZER (OPTIONAL)
5V
1.0 μFd
0.1 μFd
5V
UNSWITCHED B+
SWITCHED B+ TO RADIO

TL/F/5775-12

Logic Diagram

AM/FM PLL Synthesizer


CHARGE PUMP OUT
PHASE DETECT ECL
REF
SELECT 12.5 kHz OR 500 Hz
12.5 kHz
÷2
VCCM 6.0V, 1.5 mA (TYPICAL)
TO REFERENCE DIVIDER*
50 Hz
500 Hz
500 kHz
FIN N+1
÷10
÷50
÷20
÷8
XTAL OSC
4 MHz
MODULUS CONTROL
5V VCC
14-BIT ÷ N
÷7/8 PRESCALER ECL
AM/FM SELECT ECL
÷7/8 PRESCALER ECL
FM LO
FM-SELECT
AM LO
ENABLE
14 LATCHES
BITS 1→14 14-BIT S/R LSB FIRST
BIT 15
BIT 16
BIT 17
BIT 18
BIT 19
BIT 20
CLOCK (GATED)
LATCHES
CONTROL LOGIC AND ADDRESS** (2-BIT)
DATA INPUT
CLOCK
DATA
BIT 15 OUT
BIT 16 OUT
BIT 17 OUT
BIT 18 OUT FM/$\overline{AM}$
BIT 19 OUT
BIT 20 OUT

TL/F/5775–13

*Sections operating from V_{CCM} supply

**Address (1, 1)

National Semiconductor

DS8907 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8907 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^2L dual modulus programmable divider, and an 18-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 25 kHz reference signal for FM and a 10 kHz reference signal for AM. One of these reference signals is selected by the data from the controller for use by the phase comparator.

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line, and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 20-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 18-bit data word, the next 13 bits are used for the PLL divide code. The remaining 5 bits are connected via latches to output pins. These 5 bits can be used to drive radio functions such as gain, mute, FM, AM and stereo only. These outputs are open collector. Bit 16 is used internally to select the AM or FM local oscillator input and to select between the 10 kHz and 25 kHz reference. A high level at bit 16 indicates FM and a low level indicates AM.

The PLL consists of a 13-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p+1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–13 after address). It is clocked by the AM input via an ECL $\div 7/8$ prescaler, or through a $\div 63/64$ prescaler from the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 10 kHz and the FM band is tuned with a resolution of 25 kHz. The buffered AM and FM inputs are self biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source (−0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high. When using an AFC the charge pump output may be forced into TRI-STATE® by applying a low level to the charge pump enable input.

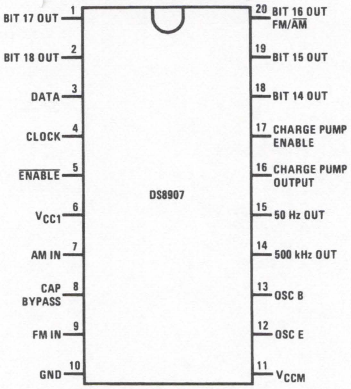
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 25 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for "time-of-day" reference driven from separate low power V_{CCM}
- 5-open collector buffered outputs for controlling various radio functions
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis

Connection Diagram

Dual-In-Line Package



TL/F/7511-1

Top View

Order Number DS8907N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.7V$			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{ENABLE}$ Inputs, $V_{IN} = 0V$			−5	−25	μA
I_{IL}	Logical "0" Input Current	Charge Pump Enable, $V_{IN} = 0V$			−250	−450	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	$V_{OH} = 5.25V$				50	μA
	500 kHz Output	$V_{OH} = 2.4V$, $V_{CCM} = 4.5V$				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	$I_{OL} = 5$ mA				0.5	V
	50 Hz Output, 500 kHz Output	$I_{OL} = 250\ \mu A$				0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bits Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	$1.2V \leq V_{OUT} \leq V_{CCM} - 1.2V$ $V_{CCM} \leq 6.0V$	Pump Up	−0.10	−0.30	−0.6	mA
			Pump Down	0.10	0.30	0.6	mA
			TRI-STATE		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, $V_{CC1} = 5.25V$, All Other Pins Open			2.5	6.0	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	$V_{IN} = 100$ mV rms $0°C \leq T_A \leq 70°C$	AM	0.4		8	MHz
			FM	60		120	MHz
$R_{IN}(FM)$	AC Input Resistance, FM	120 MHz, $V_{IN} = 100$ mV rms		300			Ω
$R_{IN}(AM)$	AC Input Resistance, AM	2 MHz, $V_{IN} = 100$ mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	$V_{IN} = 120$ MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{ENABLE}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{ENABLE}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time Before ENABLE Goes Low That CLOCK Must Be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time After ENABLE Goes Low That CLOCK Must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time Before $\overline{ENABLE}$ Goes High That Last Positive CLOCK Edge May Occur				300	600	ns

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

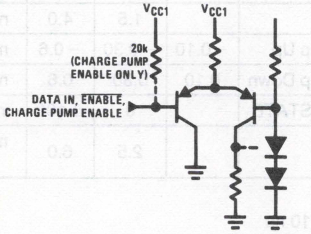
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

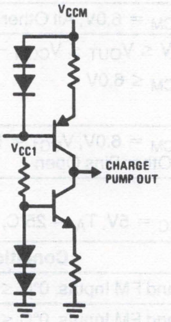
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8907.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

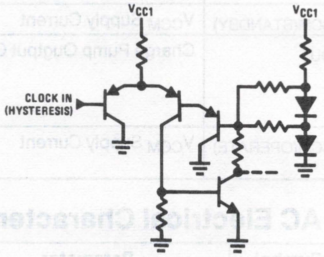
Schematic Diagrams (DS8907 AM/FM PLL typical Input/Output Schematics)


V_{CC1}
V_{CC1}
20k
(CHARGE PUMP ENABLE ONLY)
DATA IN, ENABLE, CHARGE PUMP ENABLE

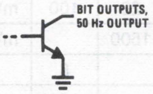
TL/F/7511–2


V_{CCM}
V_{CC1}
CHARGE PUMP OUT

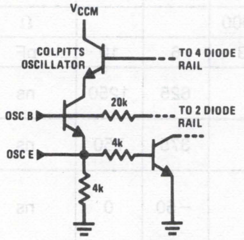
TL/F/7511–3


V_{CC1}
V_{CC1}
CLOCK IN (HYSTERESIS)

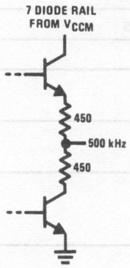
TL/F/7511–4


BIT OUTPUTS, 50 Hz OUTPUT

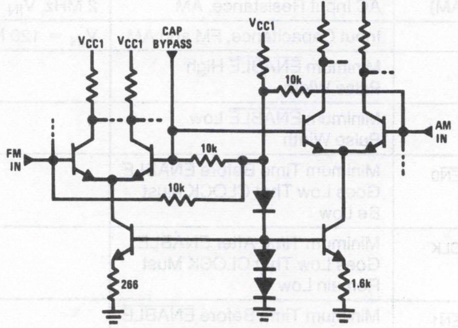
TL/F/7511–5


V_{CCM}
COLPITTS OSCILLATOR
TO 4 DIODE RAIL
20k
TO 2 DIODE RAIL
OSC B
OSC E
4k
4k

TL/F/7511–6


7 DIODE RAIL FROM V_{CCM}
450
500 kHz
450

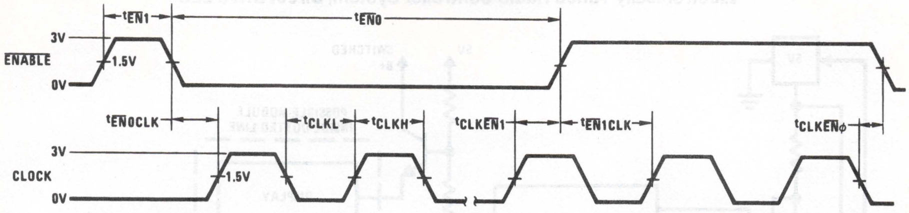
TL/F/7511–7


V_{CC1}
V_{CC1}
CAP BYPASS
V_{CC1}
V_{CC1}
V_{CC1}
10k
10k
10k
FM IN
AM IN
266
1.6k

TL/F/7511–8

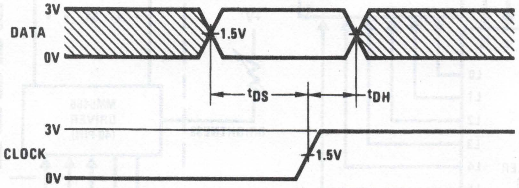
Timing Diagrams*

$\overline{\text{ENABLE}}$ vs CLOCK


$t_{\overline{EN}1}$
$t_{\overline{EN}0}$
3V
$\overline{\text{ENABLE}}$
0V
1.5V
$t_{\overline{EN}0CLK}$
t_{CLKL}
t_{CLKH}
$t_{CLK\overline{EN}1}$
$t_{\overline{EN}1CLK}$
$t_{CLK\overline{EN}\phi}$
3V
CLOCK
0V
1.5V

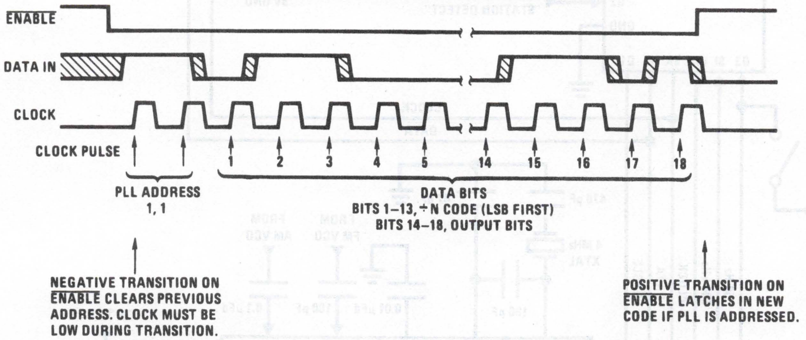
TL/F/7511-9

CLOCK vs DATA


3V
DATA
0V
1.5V
t_{DS}
t_{DH}
3V
CLOCK
0V
1.5V

TL/F/7511-10

AM/FM Frequency Synthesizer (Scan Mode)


$\overline{\text{ENABLE}}$
DATA IN
CLOCK
CLOCK PULSE
1
2
3
4
5
14
15
16
17
18
PLL ADDRESS
1, 1
DATA BITS
BITS 1–13, ÷N CODE (LSB FIRST)
BITS 14–18, OUTPUT BITS
NEGATIVE TRANSITION ON $\overline{\text{ENABLE}}$ CLEARS PREVIOUS ADDRESS. CLOCK MUST BE LOW DURING TRANSITION.
POSITIVE TRANSITION ON $\overline{\text{ENABLE}}$ LATCHES IN NEW CODE IF PLL IS ADDRESSED.

TL/F/7511-11

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8907

Serial information entry into the DS8907 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any data bits preceding the 18th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the $\overline{\text{ENABLE}}$ low. When the $\overline{\text{ENABLE}}$ input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

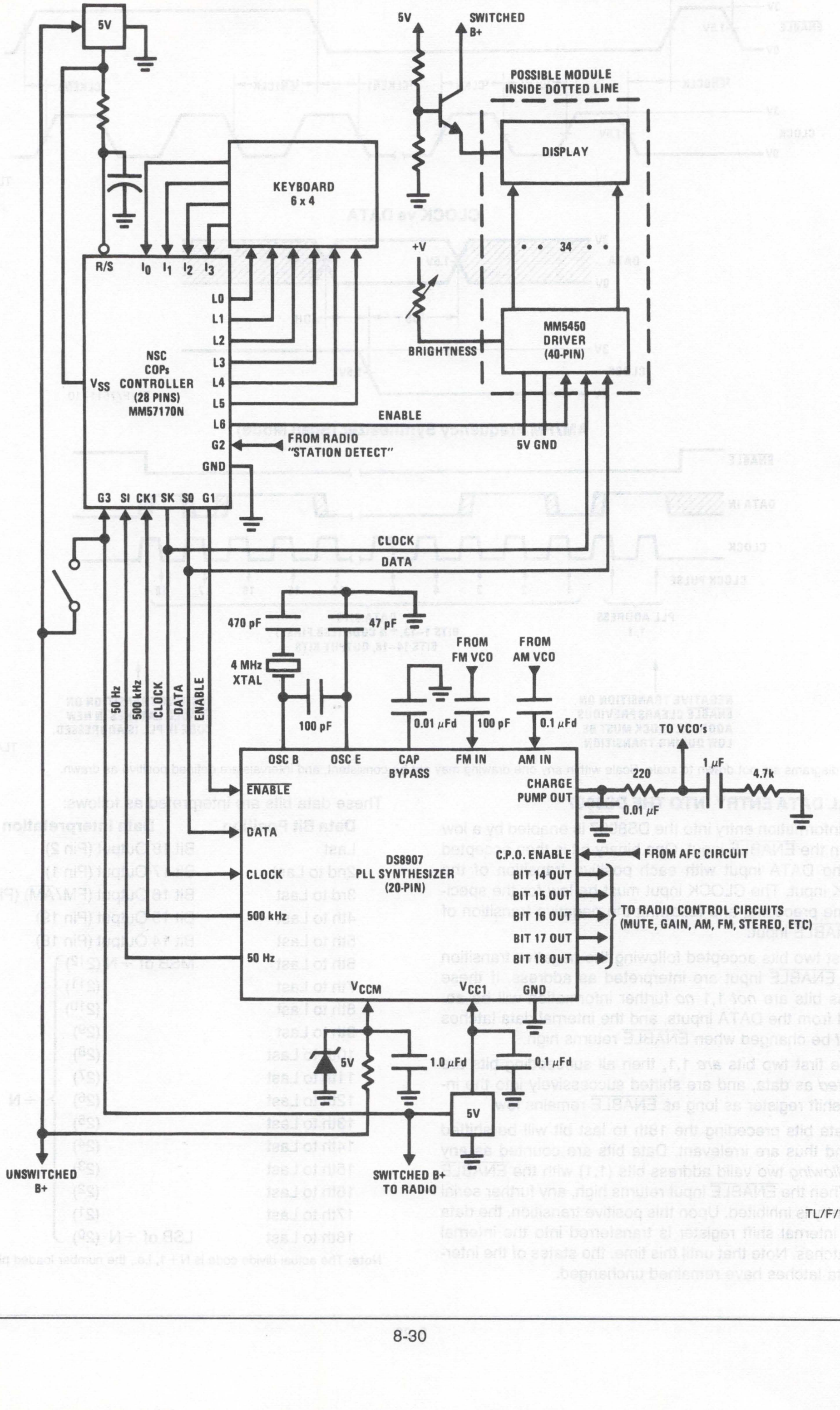
These data bits are interpreted as follows:

Data Bit Position	Data Interpretation	
Last	Bit 18 Output (Pin 2)	
2nd to Last	Bit 17 Output (Pin 1)	
3rd to Last	Bit 16 Output (FM/$\overline{\text{AM}}$) (Pin 20)	
4th to Last	Bit 15 Output (Pin 19)	
5th to Last	Bit 14 Output (Pin 18)	
6th to Last	MSB of ÷N (2^{12})	÷N
7th to Last	(2^{11})	
8th to Last	(2^{10})	
9th to Last	(2^{9})	
10th to Last	(2^{8})	
11th to Last	(2^{7})	
12th to Last	(2^{6})	
13th to Last	(2^{5})	
14th to Last	(2^{4})	
15th to Last	(2^{3})	
16th to Last	(2^{2})	
17th to Last	(2^{1})	
18th to Last	LSB of ÷N (2^{0})	

Note: The actual divide code is N+1, i.e., the number loaded plus 1.

Typical Application

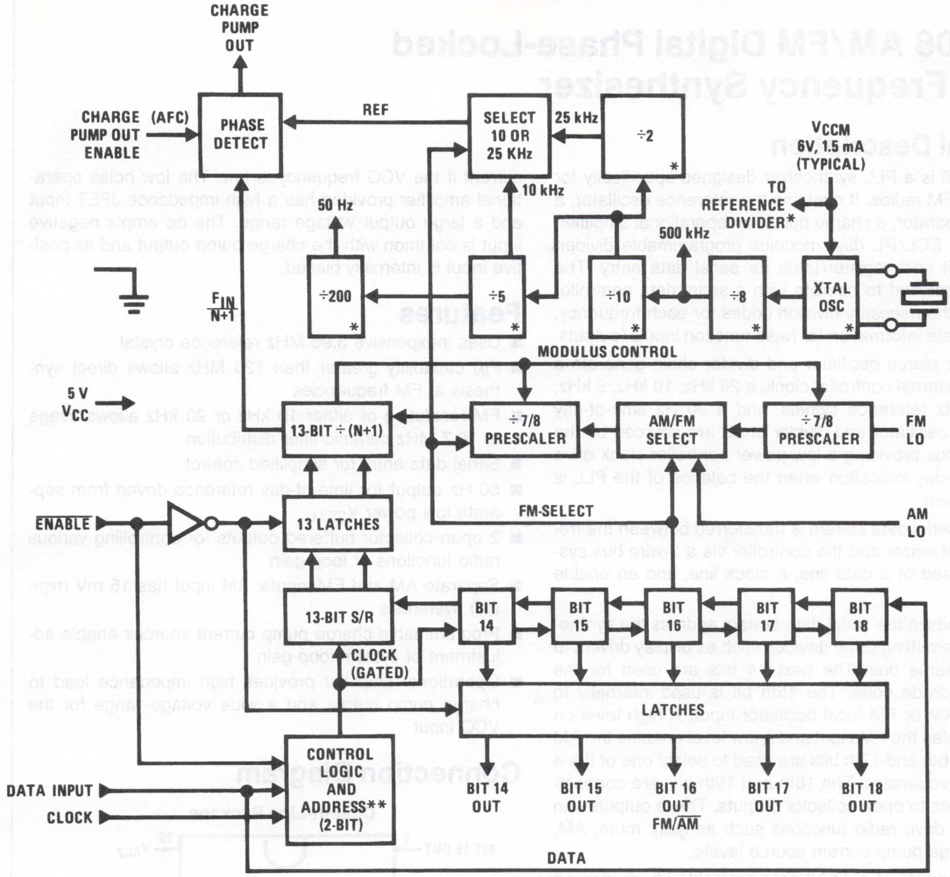
Electronically Tuned Radio Controller System; Direct Drive LED


5V
5V
SWITCHED B+
POSSIBLE MODULE INSIDE DOTTED LINE
DISPLAY
KEYBOARD 6 x 4
+V
34
R/S
I0
I1
I2
I3
L0
L1
L2
L3
L4
L5
L6
G2
GND
NSC COPs CONTROLLER (28 PINS) MM57170N
VSS
BRIGHTNESS
MM5450 DRIVER (40-PIN)
ENABLE
FROM RADIO "STATION DETECT"
5V GND
G3
SI
CK1
SK
S0
G1
CLOCK
DATA
470 pF
47 pF
4 MHz XTAL
100 pF
FROM FM VCO
FROM AM VCO
0.01 μFd
100 pF
0.1 μFd
TO VCO's
50 Hz
500 kHz
CLOCK
DATA
ENABLE
OSC B
OSC E
CAP BYPASS
FM IN
AM IN
CHARGE PUMP OUT
220
1 μF
4.7k
0.01 μF
ENABLE
DATA
CLOCK
500 kHz
50 Hz
DS8907 PLL SYNTHESIZER (20-PIN)
C.P.O. ENABLE
FROM AFC CIRCUIT
BIT 14 OUT
BIT 15 OUT
BIT 16 OUT
BIT 17 OUT
BIT 18 OUT
TO RADIO CONTROL CIRCUITS (MUTE, GAIN, AM, FM, STEREO, ETC)
VCCM
VCC1
GND
5V
1.0 μFd
0.1 μFd
5V
UNSWITCHED B+
SWITCHED B+ TO RADIO

TL/F/7511-12

Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)


CHARGE PUMP OUT
CHARGE PUMP OUT ENABLE
(AFC)
PHASE DETECT
REF
SELECT 10 OR 25 KHz
25 kHz
÷2
*
VCCM 6V, 1.5 mA (TYPICAL)
TO REFERENCE DIVIDER*
10 kHz
50 Hz
500 kHz
XTAL OSC
4 MHz
FIN N+1
÷200
÷5
÷10
÷8
MODULUS CONTROL
5 V VCC
13-BIT ÷ (N+1)
÷7/8 PRESCALER
AM/FM SELECT
÷7/8 PRESCALER
FM LO
FM-SELECT
AM LO
ENABLE
13 LATCHES
13-BIT S/R
BIT 14
BIT 15
BIT 16
BIT 17
BIT 18
CLOCK (GATED)
LATCHES
CONTROL LOGIC AND ADDRESS** (2-BIT)
DATA INPUT
CLOCK
BIT 14 OUT
BIT 15 OUT
BIT 16 OUT FM/$\overline{AM}$
BIT 17 OUT
BIT 18 OUT
DATA

TL/F/7511–13

*Sections operating from V_{CCM} supply.

**Address (1, 1)

National Semiconductor

DS8908 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necesary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and a 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data steram is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL(N+1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

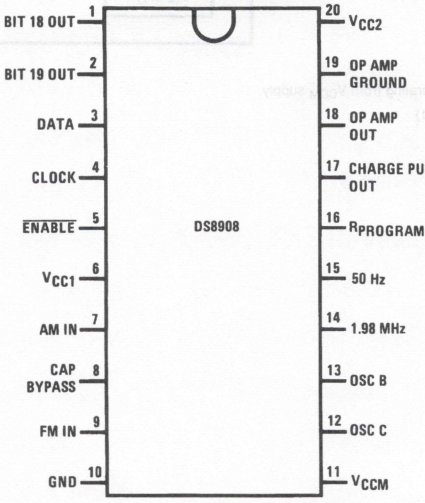
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N+1), N being the number loaded into the shift register. The programmable divider is clocked through a $\div 7/8$ prescaler by the AM input or through a $\div 63/64$ prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



TL/F/5111-1

Top View
Order Number DS8908N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(V_{CC1}) (V_{CCM})	7V
(V_{CC2})	17V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
V_{CC1}	4.5	5.5	V
V_{CC2}	V_{CC1} + 1.5	15.0	V
V_{CCM}	3.5	5.5	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	V_{OH} = 5.5V				50	μA
	1.98 MHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 1.98 MHz Output	I_{OL} = 250 μA				0.5	V
	1.98 MHz Output	I_{OL} = 20 μA, T_A > 70°C I_{OL} = 20 μA, T_A ≤ 70°C				0.3 0.4	V V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High				160	mA
I_{CCM}	V_{CCM} Supply Current	V_{CCM} = 5.5V, All Other Pins Open			2.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	3.33k ≤ R_{PROG} ≤ 33.3k I_{OUT} Measured between Pin 17 and Pin 18 I_{PROG} = V_{CC1}/2 R_{PROG}	Pump Up	−20	I_{PROG}	+20	%
			Pump Down	−20	I_{PROG}	+20	%
			TRI-STATE®		0	11	nA
I_{CC2}	V_{CC2} Supply Current	V_{CCM} = 5V, V_{CC1} = 5.5V, V_{CC2} = 15V All Other Pins Open			6.7	11	mA
OP_{VOH}	Op Amp Minimum High Level	V_{CC1} = 4.5V, I_{OH} = −750 μA		V_{CC2} −0.4			V
OP_{VOL}	Op Amp Maximum Low Level	V_{CC1} = 5.5V, I_{OL} = 750 μA				0.6	V
CPO_{BIAS}	Charge Pump Bias Voltage Delta	CPO Shorted to Op Amp Output CPO = TRI-STATE Op Amp I_{OL}: 750 μA vs −750 μA				100	mV

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r ≤ 10 ns, t_f ≤ 10 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C			20	100	mV(rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C		1000	1500		mV(rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms −40°C ≤ T_A ≤ 85°C	AM	0.5		15	MHz
			FM	80		120	MHz
R_{IN}(FM)	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		600			Ω
R_{IN}(AM)	AC Input Resistance, AM	15 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz (FM), 15 MHz (AM)		3	6	10	pF
t_{EN1}	Minimum ENABLE High Pulse Width				625	1250	ns

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \le 10$ ns, $t_f \le 10$ ns (Continued)

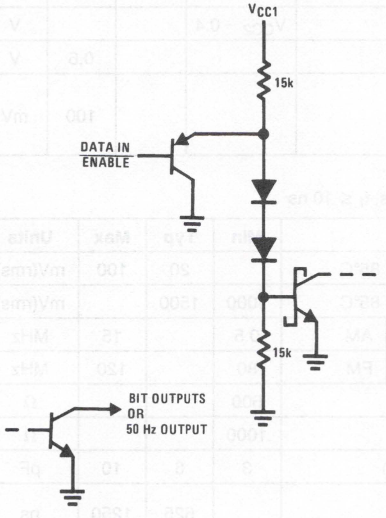
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width			375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Be Low			−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Remain Low			275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High That Last Positive CLOCK Edge May Occur			300	600	ns
$t_{\overline{EN}1CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes High before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Set-Up Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

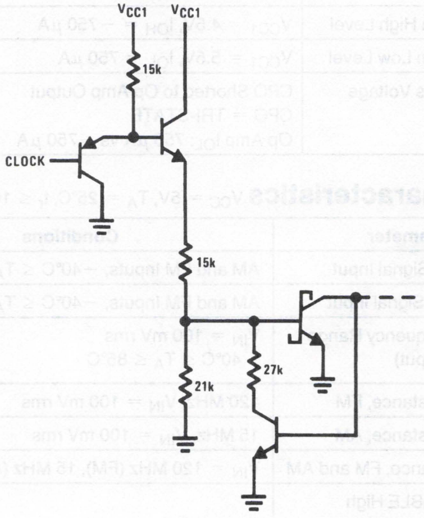
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8908.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

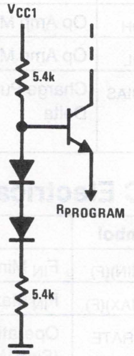
Schematic Diagrams (DS8908 AM/FM PLL Typical Input/Output Schematics)



TL/F/5111-2

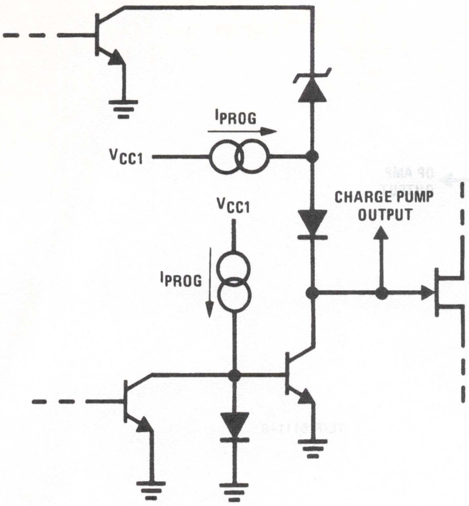


TL/F/5111-3

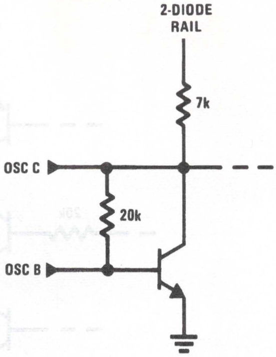


TL/F/5111-4

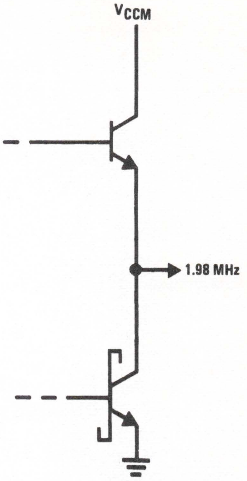
Schematic Diagrams (Continued)


I_PROG
V_CC1
V_CC1
I_PROG
CHARGE PUMP OUTPUT

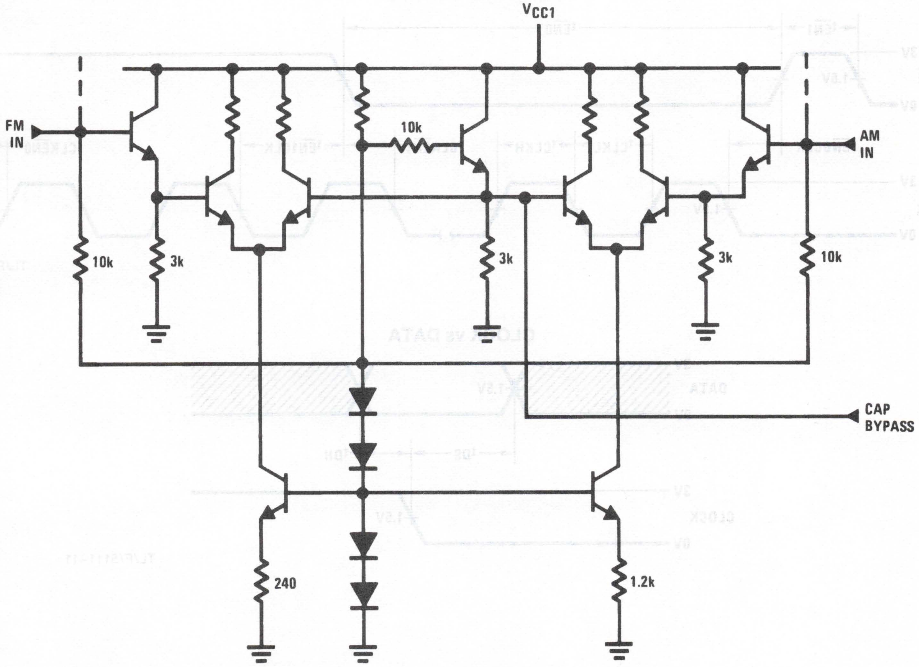
TL/F/5111-5


2-DIODE RAIL
7k
OSC C
20k
OSC B

TL/F/5111-6

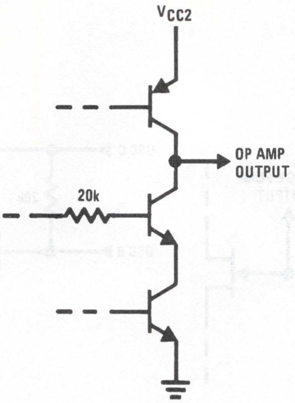

V_CCM
1.98 MHz

TL/F/5111-7


V_CC1
FM IN
10k
AM IN
10k
3k
3k
3k
10k
CAP BYPASS
240
1.2k

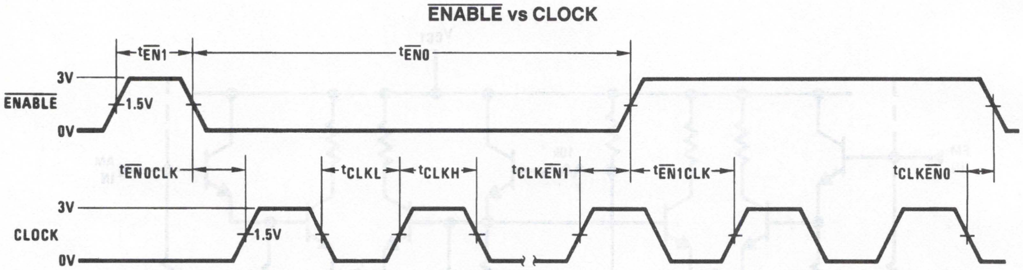
TL/F/5111-8

Schematic Diagrams (Continued)

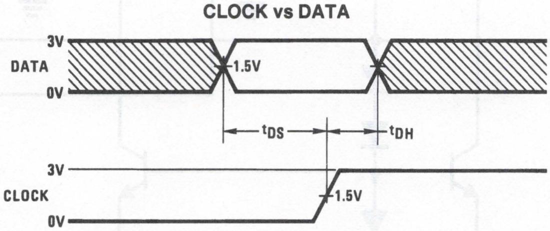

V_{CC2}
OP AMP OUTPUT
20k

TL/F/5111-9

Timing Diagrams*


$\overline{\text{ENABLE}}$ vs CLOCK
$t_{\overline{EN}1}$
$t_{\overline{EN}0}$
3V
$\overline{\text{ENABLE}}$
0V
1.5V
$t_{\overline{EN}0CLK}$
t_{CLKL}
t_{CLKH}
$t_{CLK\overline{EN}1}$
$t_{\overline{EN}1CLK}$
$t_{CLK\overline{EN}0}$
3V
CLOCK
0V
1.5V

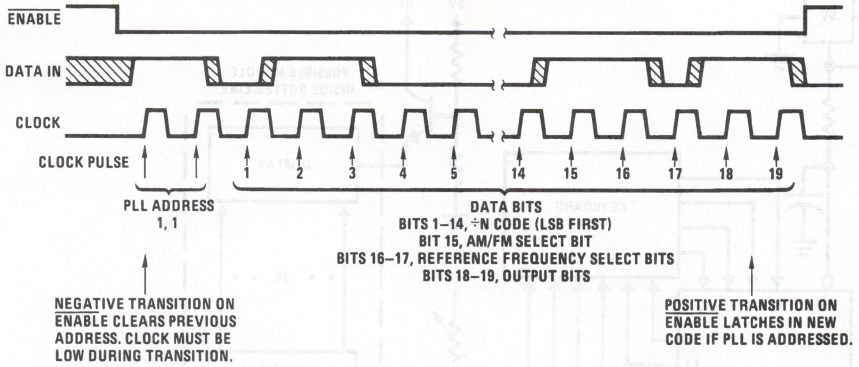
TL/F/5111-10


CLOCK vs DATA
3V
DATA
0V
1.5V
t_{DS}
t_{DH}
3V
CLOCK
0V
1.5V

TL/F/5111-11

Timing Diagrams*

AM/FM Frequency Synthesizer (Scan Mode)


ENABLE
DATA IN
CLOCK
CLOCK PULSE
1
2
3
4
5
14
15
16
17
18
19
PLL ADDRESS
1, 1
DATA BITS
BITS 1–14, ÷N CODE (LSB FIRST)
BIT 15, AM/FM SELECT BIT
BITS 16–17, REFERENCE FREQUENCY SELECT BITS
BITS 18–19, OUTPUT BITS
NEGATIVE TRANSITION ON ENABLE CLEARS PREVIOUS ADDRESS. CLOCK MUST BE LOW DURING TRANSITION.
POSITIVE TRANSITION ON ENABLE LATCHES IN NEW CODE IF PLL IS ADDRESSED.

TL/F/5111-12

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8908

Serial information entry into the DS8908 is enabled by a low level on the ENABLE input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the ENABLE input.

The first two bits accepted following the negative transition of the ENABLE input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted fromt he DATA inputs, and the internal data latches *will not* be changed when ENABLE returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as ENABLE remains low.

Any data bits preceding the 19th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the ENABLE low. When the ENABLE input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

Data Bit Position	Data Interpretation	
Last	Bit 19 Output (Pin 2)	
2nd to Last	Bit 18 Output (Pin 1)	
3rd to Last	Ref. Freq. Select Bit[1] 17	
4th to Last	Ref. Freq. Select Bit[1] 16	
5th to Last	AM/FM Select Bit 15	
6th to Last	(2^{13})	÷N[2]
7th to Last	(2^{12})	
8th to Last	(2^{11})	
9th to Last	(2^{10})	
10th to Last	(2^{9})	
11th to Last	(2^{8})	
12th to Last	(2^{7})	
13th to Last	(2^{6})	
14th to Last	(2^{5})	
15th to Last	(2^{4})	
16th to Last	(2^{3})	
17th to Last	(2^{2})	
18th to Last	(2^{1})	
19th to Last	LSB of ÷N(2^{0})	

Note 1: See Reference Frequency Select Truth Table.

Note 2: The actual divide code is N+1, ie., the number loaded plus 1.

Truth Table

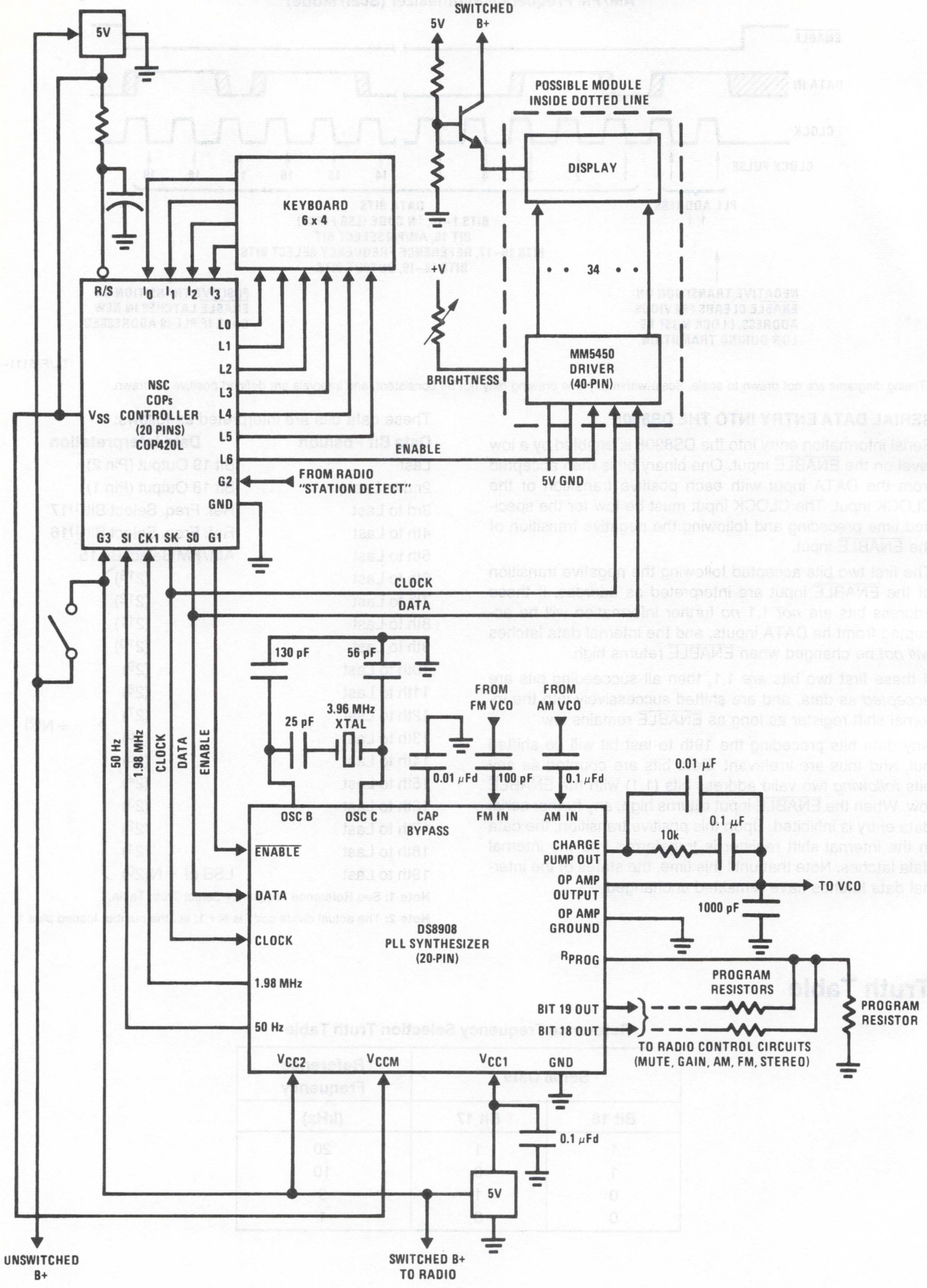
Reference Frequency Selection Truth Table

Serial Data		Reference Frequency
Bit 16	**Bit 17**	**(kHz)**
1	1	20
1	0	10
0	1	9
0	0	1

Typical Application

Additional application notes are located at the back of section 11.

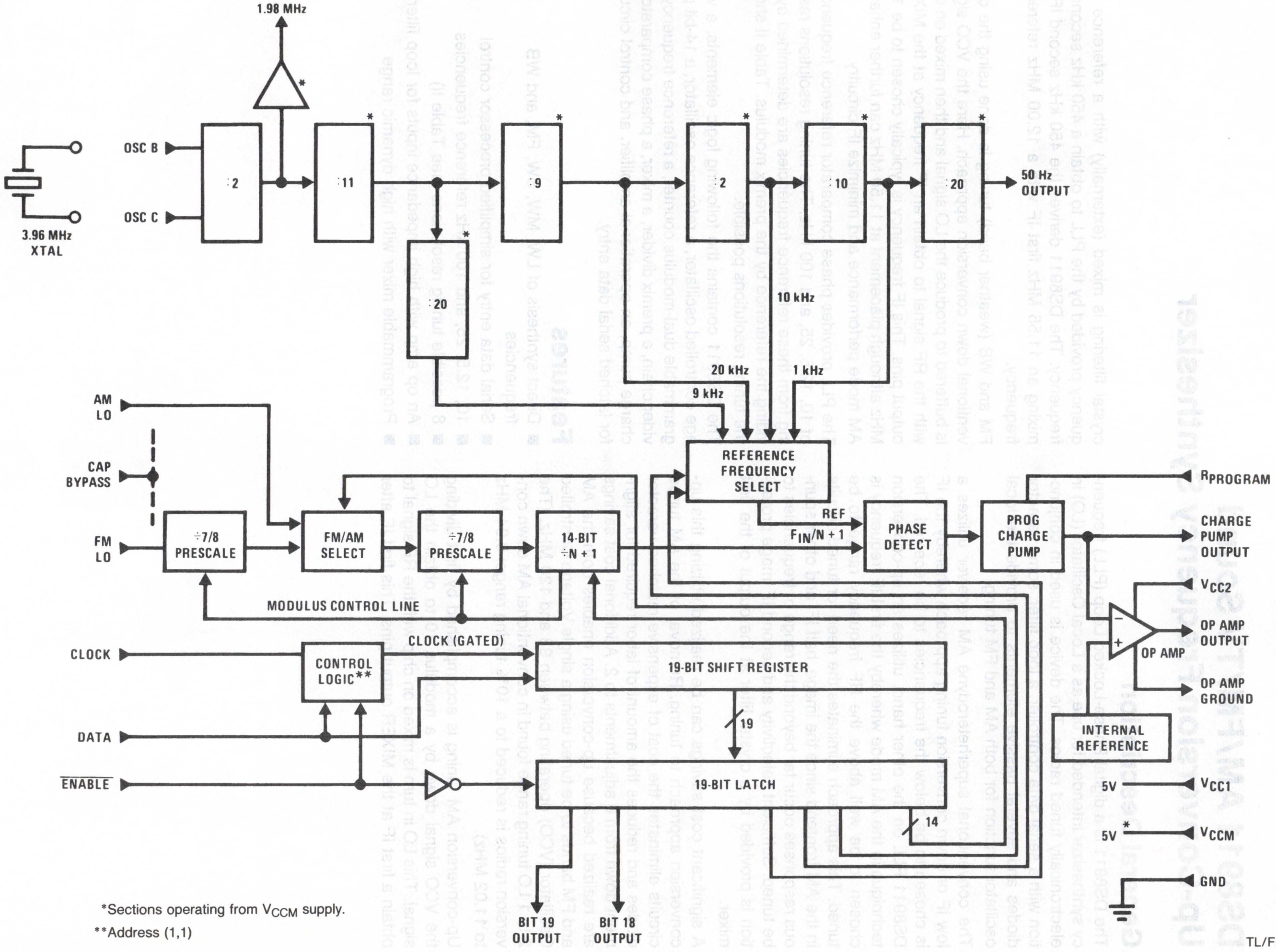
Electronically Tuned Radio Controller System; Direct Drive LED


5V
R/S
I$_0$
I$_1$
I$_2$
I$_3$
L0
L1
L2
L3
L4
L5
L6
G2
GND
G3 SI CK1 SK S0 G1
V$_{SS}$
NSC
COPs
CONTROLLER
(20 PINS)
COP420L
KEYBOARD
6 x 4
SWITCHED
5V
B+
+V
BRIGHTNESS
POSSIBLE MODULE
INSIDE DOTTED LINE
DISPLAY
34
MM5450
DRIVER
(40-PIN)
5V GND
ENABLE
FROM RADIO
"STATION DETECT"
CLOCK
DATA
130 pF
56 pF
25 pF
3.96 MHz
XTAL
50 Hz
1.98 MHz
CLOCK
DATA
ENABLE
FROM
FM VCO
FROM
AM VCO
0.01 μFd
100 pF
0.1 μFd
0.01 μF
OSC B
OSC C
CAP
BYPASS
FM IN
AM IN
0.1 μF
10k
CHARGE
PUMP OUT
OP AMP
OUTPUT
TO VCO
1000 pF
OP AMP
GROUND
R$_{PROG}$
PROGRAM
RESISTORS
PROGRAM
RESISTOR
BIT 19 OUT
BIT 18 OUT
TO RADIO CONTROL CIRCUITS
(MUTE, GAIN, AM, FM, STEREO)
ENABLE
DATA
CLOCK
1.98 MHz
50 Hz
DS8908
PLL SYNTHESIZER
(20-PIN)
V$_{CC2}$
V$_{CCM}$
V$_{CC1}$
GND
0.1 μFd
5V
UNSWITCHED
B+
SWITCHED B+
TO RADIO

TL/F/5111-13

Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)


1.98 MHz
3.96 MHz XTAL
OSC B
OSC C
÷2
÷11
÷9
÷2
÷10
÷20
÷20
50 Hz OUTPUT
10 kHz
20 kHz
1 kHz
9 kHz
AM LO
CAP BYPASS
FM LO
÷7/8 PRESCALE
FM/AM SELECT
÷7/8 PRESCALE
14-BIT ÷N + 1
REFERENCE FREQUENCY SELECT
REF
$F_{IN}/N + 1$
PHASE DETECT
PROG CHARGE PUMP
$R_{PROGRAM}$
CHARGE PUMP OUTPUT
V_{CC2}
OP AMP OUTPUT
OP AMP
OP AMP GROUND
INTERNAL REFERENCE
MODULUS CONTROL LINE
CLOCK (GATED)
CLOCK
CONTROL LOGIC**
19-BIT SHIFT REGISTER
19
DATA
ENABLE
19-BIT LATCH
14
5V
V_{CC1}
5V
V_{CCM}
GND
BIT 19 OUTPUT
BIT 18 OUTPUT

*Sections operating from V_{CCM} supply.

**Address (1,1)

TL/F/5111–14

National Semiconductor

DS8911 AM/FM/TV Sound Up-Conversion Frequency Synthesizer

General Description

The DS8911 is a digital Phase-Locked Loop (PLL) frequency synthesizer intended for use as a Local Oscillator (LO) in electronically tuned radios. The device is used in conjunction with a serial data controller, a loop filter, some varactor diodes and several passive elements to provide the local oscillator function for both AM and FM tuning.

The conventional superheterodyne AM receiver utilizes a low IF or down conversion tuning approach whereby the IF is chosen to be below the frequencies to be received. The DS8911 PLL on the other hand, utilizes an up-conversion technique in the AM mode whereby the first IF frequency is chosen to be well above the RF frequency range to be tuned. This approach eliminates the need for tuned circuits in the AM frontend since the image, half IF, and other spurious responses occur far beyond the range of frequencies to be tuned. Sufficient selectivity and second IF image protection is provided by a crystal filter at the output of the first mixer.

A significant cost savings can be realized utilizing this up-conversion approach to tuning. Removal of the AM tuned circuits eliminates the cost of expensive matched varactor diodes and reduces the amount of labor required for alignment down from 6 adjustments to 2. Additional cost savings are realized because up-conversion enables both the AM and FM bands to be tuned using a single Voltage Controlled Oscillator (VCO) operating between 98 and 120 MHz. (The 2 to 1 LO tuning range found in conventional AM down conversion radios is reduced to a 10% tuning range; 9.94 MHz to 11.02 MHz).

Up-conversion AM tuning is accomplished by first dividing the VCO signal down by a modulus 10 to obtain the LO signal. This LO in turn is mixed on chip with the RF signal to obtain a first IF at the MIXER output pins. This first IF after crystal filtering is mixed (externally) with a reference frequency provided by the PLL to obtain a 450 kHz second IF frequency. The DS8911 derives the 450 kHz second IF by mixing an 11.55 MHz first IF with a 12.00 MHz reference frequency.

FM and WB (weather band) tuning is done using the conventional down conversion approach. Here the VCO signal is buffered to produce the LO signal and then mixed on chip with the RF signal to obtain an IF frequency at the MIXER output pins. This IF frequency is typically chosen to be 10.7 MHz although placement at 11.50 MHz can further enhance AM mode performance and minimize IF circuitry.

The PLL provides phase comparator reference frequencies of 10, 12.5, 25, and 100 kHz. The tuning resolutions resulting from these reference frequencies are determined by dividing the reference by the premix modulus. Table II shows the tuning resolutions possible.

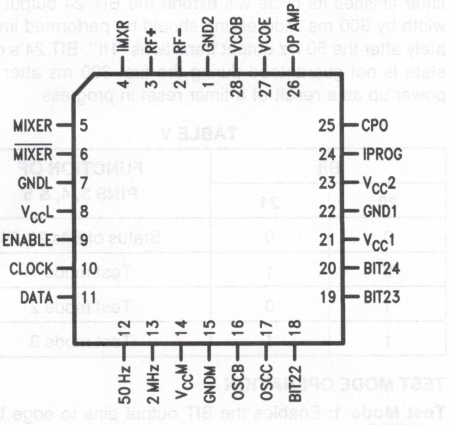
The DS8911 contains the following logic elements: a voltage controlled oscillator, a reference oscillator, a 14-bit programmable dual-modulus counter, a reference frequency divider chain, a premix divider, a mixer, a phase comparator, a charge pump, an operational amplifier, and control circuitry for latched serial data entry.

Features

- Direct synthesis of LW, MW, SW, FM, and WB frequencies
- Serial data entry for simplified processor control
- 10, 12.5, 25, and 100 kHz reference frequencies
- 8 possible tuning resolutions (see Table II)
- An op amp with high impedance inputs for loop filtering
- Programmable mixer with high dynamic range

Connection Diagram

Plastic Chip Carrier



TL/F/7398-8

Top View

Order Number DS8911V
See NS Package Number V28A

Pin Descriptions

V_{CC1}: The V_{CC1} pin provides a 5V supply source for all circuitry except the reference divider chain, op amp and mixer sections of the die.

V_{CC2}: The V_{CC2} pin provides a 12V supply source for the Op amp.

V_{CCL}: The V_{CCL} pin provides an isolated 5V supply source for the premix divider and mixer functions.

V_{CCM}: The V_{CCM} pin provides a 5V supply source for the reference oscillator and divider chain down through the 50 Hz output, thus enabling low standby current for time-of-day clock applications.

GND1, GND2, GNDL and GNDM: Provide isolated circuit ground for the various sections of the device.

DATA and CLOCK: The DATA and CLOCK inputs are for serial data entry from a controller. They are CMOS inputs with TTL logic thresholds. The 24-bit data stream is loaded into the PLL on the positive transition of the CLOCK. The first 14 bits of the data stream select PLL divide code in binary form MSB first. The 15th through 24th bits select the premix modulus, the reference frequency, the bit output status, and the test/operate modes as shown in Tables I through V.

ENABLE: The ENABLE input is a CMOS input with a TTL logic threshold. The ENABLE input enables data when at a logic "one" and latches data on the transition to a logic "zero".

BIT Outputs: The open-collector BIT outputs provide either the status of shift register bits 22, 23, and 24 or enable access to key internal circuit test nodes. The mode for the bit outputs is controlled by shift register bits 20 and 21. In operation, the bit outputs are intended to drive radio functions such as gain, mute, and AM/FM status. These outputs can also be used to program the loop gain by connection of an external resistor to IPROG. Bit 24 output can also be used as a 300 millisecond timer under control of shift register bit 19. During service testing, these pins can be used for the purpose of either monitoring or driving internal logic points as indicated in the TEST MODES description under Table V.

VCOb and VCOe: The Voltage Controlled Oscillator inputs drive the 14-bit programmable counter and the premix divider. These inputs are the base and emitter leads of a transistor which require connection of a coil, varactor, and several capacitors to function as a Colpitts oscillator. The VCO is designed to operate up to 225 MHz. The VCO's minimum operating frequency may be limited by the choice of reference frequency and the 961 minimum modulus constraint of the 31/32 dual modulus counter.

RF+ and RF−: The Radio Frequency inputs are fed differentially into the mixer.

IMXR: The bias current for the mixer is programmed by connection of an external resistor to this pin. The total mixer output current equals 4 times the current entering this pin.

MIXER and $\overline{\text{MIXER}}$: The MIXER outputs are the collectors of the double balanced pair mixer transistors. They are intended to operate at voltages greater than V_{CC1}.

OSCb and OSCc: The Reference Oscillator inputs are part of an on-chip Pierce oscillator designed to work in conjunction with 2 capacitors and a crystal resonator. The DS8911 requires a 12 MHz crystal to derive the reference frequencies shown in Table II.

The 12 MHz OSC signal is also used externally as the 2nd AM LO to obtain a 450 kHz 2nd IF frequency in the AM mode.

2 MHz: The 2 MHz output is provided to drive a controller's clock input.

50 Hz: The 50 Hz output is provided as a time reference for radios with time-of-day clocks.

IPROG: The IPROG pin enables the charge pump to be programmed from 0.25 mA to 1.0 mA by connection of an external resistor to ground.

CPO: The Charge Pump Output circuit sources current if the VCO frequency is high and sinks current if the VCO frequency is low. The CPO is wired directly to the negative input of the loop filter op amp.

OP AMP: The OP AMP output is provided for loop filtering. The op amp has high impedance PMOS gate inputs and is wired as a transconductance amplifier/filter. The op amp's positive input is internally referenced while its negative input is common with the CPO output.

Reference Tables

TABLE I

Bit 15	Premix Modulus
0	÷1
1	÷10

TABLE II

Bit		Reference Frequency	Tuning Resolution	
16	17		÷1 Premix	÷10 Premix
0	0	10 kHz	10 kHz	1 kHz
0	1	12.5 kHz	12.5 kHz	1.25 kHz
1	0	25 kHz	25 kHz	2.5 kHz
1	1	100 kHz	100 kHz	10 kHz

TABLE III

Bit 18	Mode
0	Normal Operation*
1	Production Test Mode Only

*The user should always load Bit 18 low.

TABLE IV

Bit 19	Timer
0	Bit 24 Status
1	Bit 24 for 300 ms

TIMER OPERATION

The timer function is provided for use as a retriggerable "one shot" to enable muting for approximately 300 milliseconds after station changes. The timer is enabled at bit 24's output if the normal operating mode is selected (shift register bits 20 and 21 = "LOW") and shift register bit 19 data is latched as a "HI". The timer's output state will invert immediately upon latching bit 19 "HI" and remain inverted for approximately 300 milliseconds. If the user readdresses the device with bit 19 data "LOW" before the timer finishes its cycle the timer's BIT 24 output will finish out the 300 ms pulse. Readdressing the device with bit 19 "HI" before the timer finishes its cycle will extend the BIT 24 output pulse width by 300 ms. Addressing should be performed immediately after the 50 Hz output transitions "HI". BIT 24's output state is not guaranteed during the first 300 ms after V_{CC_1} power up as a result of a timer reset in progress.

TABLE V

Bit		FUNCTION OF PINS 3, 4, & 5
20	21	
0	0	Status of Bits 22-24
0	1	Test mode 1
1	0	Test mode 2
1	1	Test mode 3

TEST MODE OPERATION

Test Mode 1: Enables the BIT output pins to edge trigger the phase comparator inputs and monitor an internal lock detector. BIT 22 negative edge triggers the reference divider input of the phase comparator if the reference divider state is low. BIT 23 provides the open collector ORing of the phase comparator's pump up and down outputs. BIT 24 negative edge triggers the N counter input of the phase comparator if the N counter state is preconditioned low.

Test Mode 2: Enables the BIT outputs to clock the programmable N counter, monitor its output, and force either its load or count condition. BIT 22 provides the N counter output which negative edge triggers the phase comparator and which appears low one N counter clock pulse before it reloads. BIT 23 positive edge triggers the N counter's clock input if the prescaler's output is preconditioned HI. BIT 24 clears the N counter output so that loading will occur on the next N counter clock edge.

Test Mode 3: Enables the BIT outputs to clock the 50 Hz and 10 kHz reference dividers and monitor the reference divider input to the phase comparator. BIT 22 positive edge clocks the 10 kHz reference divider chain if the 10 kHz output is preconditioned HI. BIT 23 positive edge clocks the 50 Hz divider chain. BIT 24 is the reference divider negative edge trigger input to the phase comparator.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CCM}	7V
V_{CC1}	7V
V_{CC2}	15V
Input Voltage	7V
Output Voltage	
Logic	7V
Op Amp and Mixer Outputs	15V
ESD Sensitivity	1000V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CCM}	3.5	5.5	V
V_{CC1}	4.5	5.5	V
V_{CC2}	7.0	12.0	V
Temperature, T_A	−40	+85	°C
Mixer I_{BIAS} (Mixer + $\overline{\text{Mixer}}$ Current)	1	20	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage				2.0			V
V_{IL}	Logic "0" Input Voltage						0.8	V
I_{IH}	Logic "1" Input Current		$V_{IN} = 5.5V$				10	μA
I_I	Logic "1" Input Current		Data, Clock and Enable Inputs, $V_{IN} = 7V$				100	μA
I_{IL}	Logic "0" Input Current		Data, Clock and Enable Inputs, $V_{IN} = 0V$				−10	μA
V_{OH}	Logic "1" Output Voltage	2 MHz	$I_{OH} = -20\ \mu A$		$V_{CCM}-0.3$			V
			$I_{OH} = -400\ \mu A$		$V_{CCM}-2$			V
		Op Amp	$I_{OH} = -1.0\ mA$		$V_{CC2}-1.5$			V
V_{OL}	Logic "0" Output Voltage	2 MHz	$I_{OL} = 20\ \mu A$				0.3	V
			$I_{OL} = 400\ \mu A$				0.4	V
		50 Hz	$I_{OL} = 250\ \mu A$				0.3	V
		Bit Outputs	$I_{OL} = 1\ mA$				0.3	V
		Op Amp	$I_{OL} = 1.0\ mA$				1.5	V
V_{BIAS}	Op Amp Input VΔ		Op Amp I/O Shorted, $V_{CC1} = 5.5V$, $V_{CC2} = 12V$, CPO = TRI-STATE®, Op Amp I_{OH} vs. I_{OL} Applied				200	mV
I_{CEX}	High Level Output Current	Bit Outputs	$V_{CC1} = 4.5V$, $V_O = 8.8V$				100	μA
		50 Hz	$V_{CCM} = 3.5V$, $V_O = 5.5V$				10	μA
		Mixers	$V_{CCL} = V_{CC1} = 4.5V$, $V_O = 12V$				100	μA
I_{CPO}	Charge Pump Program Current		$0.25\ mA < I_{CPO} < 1.0\ mA$ $2\ I_{PROG} = V_{CC1}/R_{PROG}$, Measured I_{PROG} to CPO	Pump-up	−30	$2\ I_{PROG}$	+30	%
				Pump-down	−30	$2\ I_{PROG}$	+30	%
				TRI-STATE		0	100	nA
I_{CCM}	V_{CCM} Supply Current (Static)		$V_{CCM} = 5.5V$, OSCC = High			0.5	1.0	mA
$I_{CC1} + I_{CCL}$	$V_{CC1} + V_{CCL}$ Supply Current		$V_{CC} = 5.5V$, Bits Hi, I_{MXR} and I_{PROG} Open			25	35	mA
I_{CC2}	V_{CC2} Supply Current		$V_{CC2} = 12V$			1.5	2.5	mA
Mixer I_{BIAS}	Mixer + $\overline{\text{Mixer}}$ Current (Note 4)		$V_{CC1} = V_{CCL} = 5.5V$, Mixer = $\overline{\text{Mixer}}$ = 12V		−25	$4\ I_{MXR}$	+25	%
RF_{IN}	Mixer Input Max Signal Level		Mixer $I_{BIAS} = 20\ mA$ RF+ or RF− Signal Level			300		mVrms

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range.

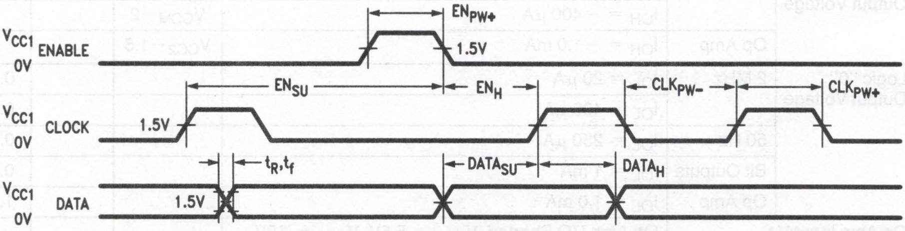
Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Note 4: Total mixer output current (Mixer + $\overline{\text{Mixer}}$) ≅ 4 times the current into the I_{MXR} pin.

AC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	20%–80% Rise Time			200		ns
t_f	80%–20% Fall Time			200		ns
$DATA_{SU}$	Data Setup Time	V_{CC1} = 4.5V to 5.5V	100			ns
$DATA_H$	Data Hold Time		100			ns
EN_{SU}	Enable Setup Time		100			ns
EN_H	Enable Hold Time		100			ns
EN_{PW+}	Enable Positive Pulse Width		200			ns
CLK_{PW+}	Clock Positive Pulse Width		200			ns
CLK_{PW-}	Clock Negative Pulse Width		200			ns
VCO f_{max}	VCO Max Frequency	See Typical Wiring Diagram	20		225	MHz
OSC f_{max}	Reference Oscillator Max Frequency	V_{CCM} = 3.5V		12		MHz

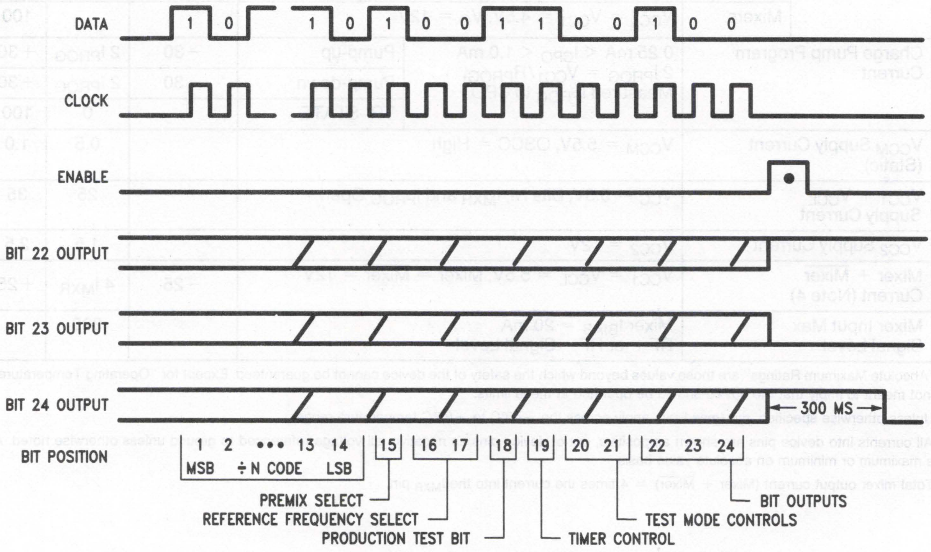
Timing Diagram



ENPW+
VCC1
ENABLE
0V
1.5V
ENSU
ENH
CLKPW-
CLKPW+
VCC1
CLOCK
0V
1.5V
tR,tf
DATASU
DATAH
VCC1
DATA
0V
1.5V

TL/F/7398-10

MICROWIRE™ Bus Format



DATA
1 0 1 0 1 0 0 1 1 0 0 1 0 0
CLOCK
ENABLE
BIT 22 OUTPUT
BIT 23 OUTPUT
BIT 24 OUTPUT
300 MS
BIT POSITION
1 2 ••• 13 14
MSB ÷N CODE LSB
15 16 17 18 19 20 21 22 23 24
PREMIX SELECT
REFERENCE FREQUENCY SELECT
PRODUCTION TEST BIT
TIMER CONTROL
TEST MODE CONTROLS
BIT OUTPUTS

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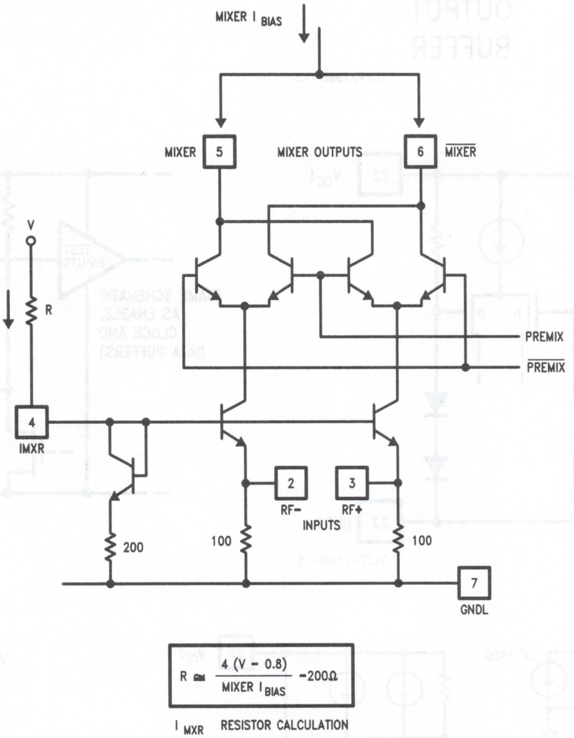
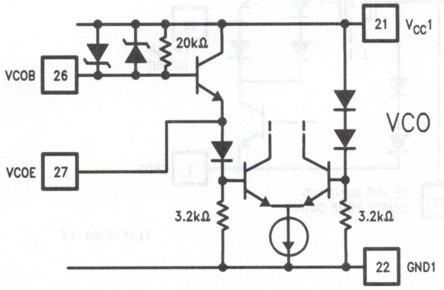
TABLE VI. DS8911 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	11.55/.450	.145–.290	112.4–114.1	10	10	1	22–23
MW	11.55/.450	.515–1.61	99.4–110.2	10	10, 12.5, 25, 100	1, 1.25, 2.5, 10	21–23
SW	11.55/.450	5.94–6.2	53.5 to 56.1	10	10, 12.5, 25	1, 1.25, 2.5	28–30
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142
TV_1	10.7	59.75–87.75	70.45–98.45	1	25	25	81–109
TV_2	10.7	179.75–215.75	169.1–205.1	1	25	25	158–194

Input and Output Schematics

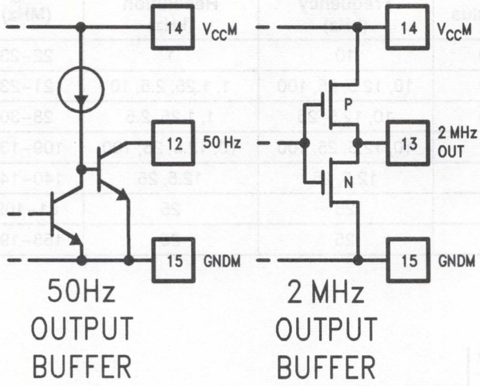

MIXER I BIAS
MIXER
5
MIXER OUTPUTS
6
MIXER
V
I MXR
R
PREMIX
PREMIX
4
IMXR
2
3
RF−
RF+
INPUTS
200
100
100
7
GNDL
$R \cong \frac{4(V-0.8)}{\text{MIXER } I_{BIAS}} - 200\Omega$
I MXR RESISTOR CALCULATION

TL/F/7398-11


20kΩ
21
$V_{CC}1$
VCOB
26
VCO
VCOE
27
3.2kΩ
3.2kΩ
22
GND1

TL/F/7398-12

Input and Output Schematics (Continued)


14
$V_{CC}M$
12
50 Hz
15
GNDM
50Hz OUTPUT BUFFER
14
$V_{CC}M$
P
13
2 MHz OUT
N
15
GNDM
2 MHz OUTPUT BUFFER

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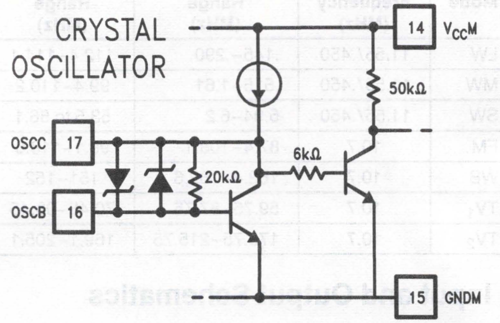
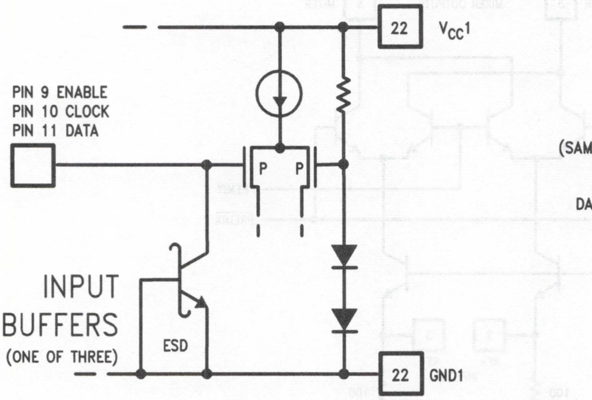
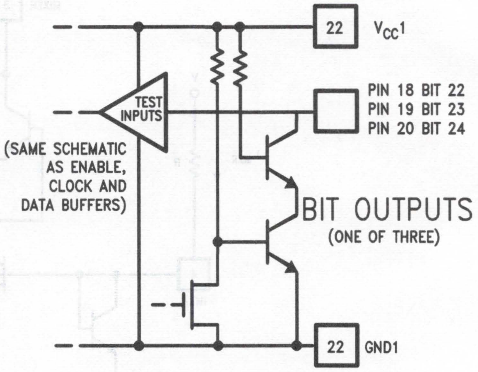

CRYSTAL OSCILLATOR
14
$V_{CC}M$
50kΩ
OSCC
17
6kΩ
20kΩ
OSCB
16
15
GNDM

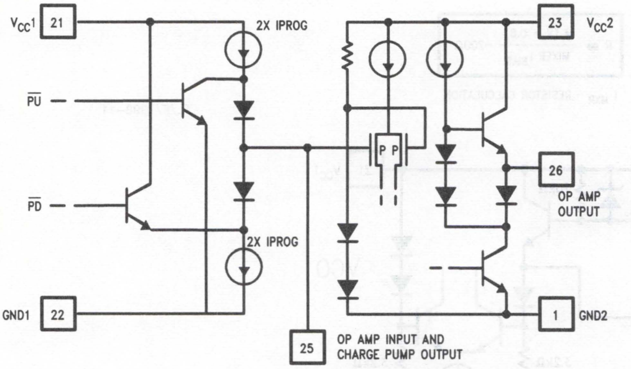
TL/F/7398-14


22
$V_{CC}1$
PIN 9 ENABLE
PIN 10 CLOCK
PIN 11 DATA
P
P
INPUT BUFFERS
(ONE OF THREE)
ESD
22
GND1

TL/F/7398-15


22
$V_{CC}1$
TEST INPUTS
PIN 18 BIT 22
PIN 19 BIT 23
PIN 20 BIT 24
(SAME SCHEMATIC AS ENABLE, CLOCK AND DATA BUFFERS)
BIT OUTPUTS
(ONE OF THREE)
22
GND1

TL/F/7398-16


$V_{CC}1$
21
2X IPROG
PU
PD
2X IPROG
GND1
22
P P
23
$V_{CC}2$
26
OP AMP OUTPUT
1
GND2
25
OP AMP INPUT AND CHARGE PUMP OUTPUT

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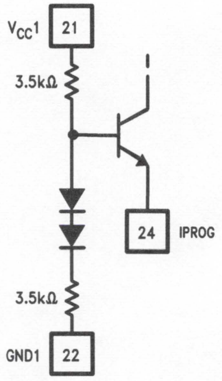
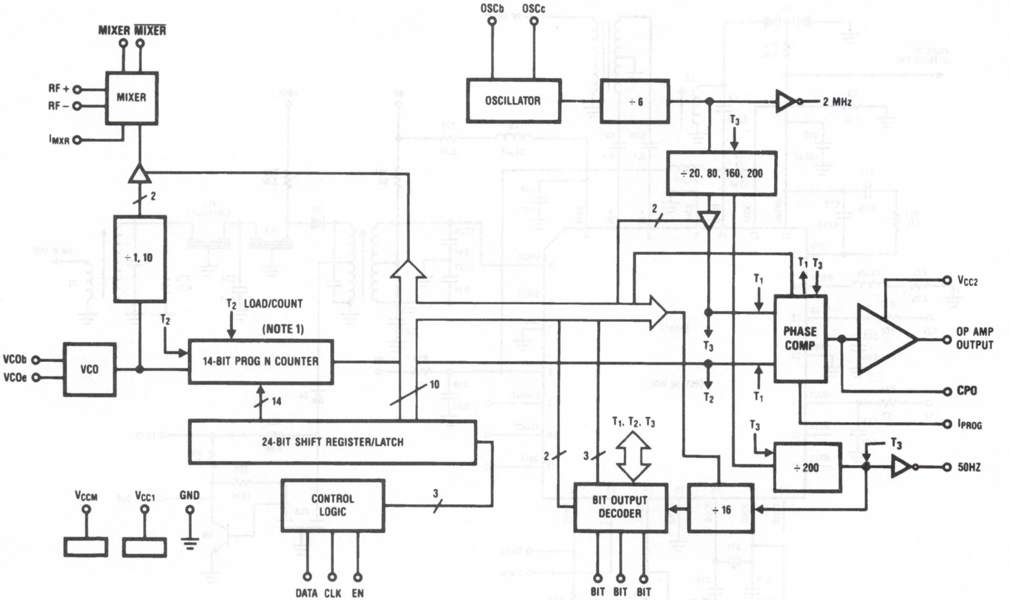

$V_{CC}1$
21
3.5kΩ
24
IPROG
3.5kΩ
GND1
22

TL/F/7398-18

Logic Diagram

DS8911 PLL Synthesizer


OSCb
OSCc
MIXER
MIXER
RF +
RF −
MIXER
I_MXR
OSCILLATOR
÷ 6
2 MHz
T3
÷ 20, 80, 160, 200
2
2
÷ 1, 10
T2 LOAD/COUNT
(NOTE 1)
T2
T1 T3
T1
Vcc2
PHASE COMP
OP AMP OUTPUT
VCOb
VCOe
VCO
14-BIT PROG N COUNTER
T3
T2
T1
CPO
10
14
IPROG
T1, T2, T3
T3
T3
24-BIT SHIFT REGISTER/LATCH
÷ 200
50HZ
2
3
VCCM
VCC1
GND
CONTROL LOGIC
3
BIT OUTPUT DECODER
÷ 16
DATA
CLK
EN
BIT 22
BIT 23
BIT 24

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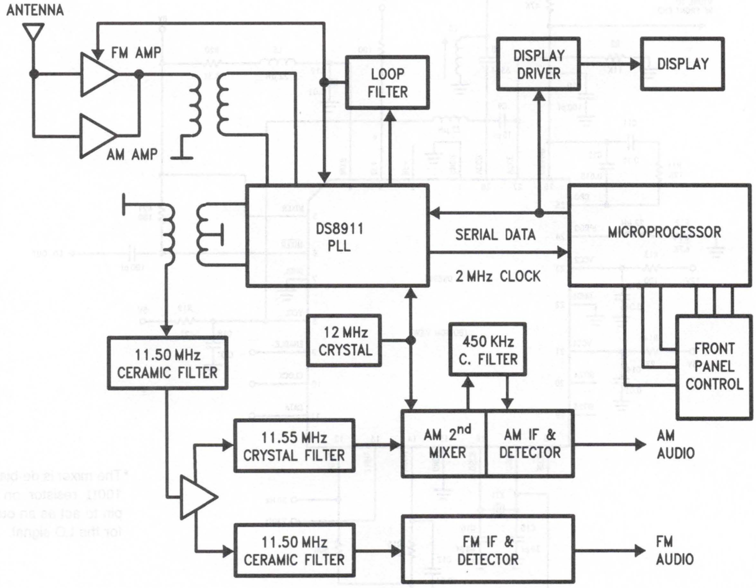
Note 1: The 14 bit programmable N counter is a dual modulus counter with 31/32 prescaler. The minimum continuous modulus of the N counter is 961. (There are a limited number of valid modulus codes below 961.)

Typical Application Diagram

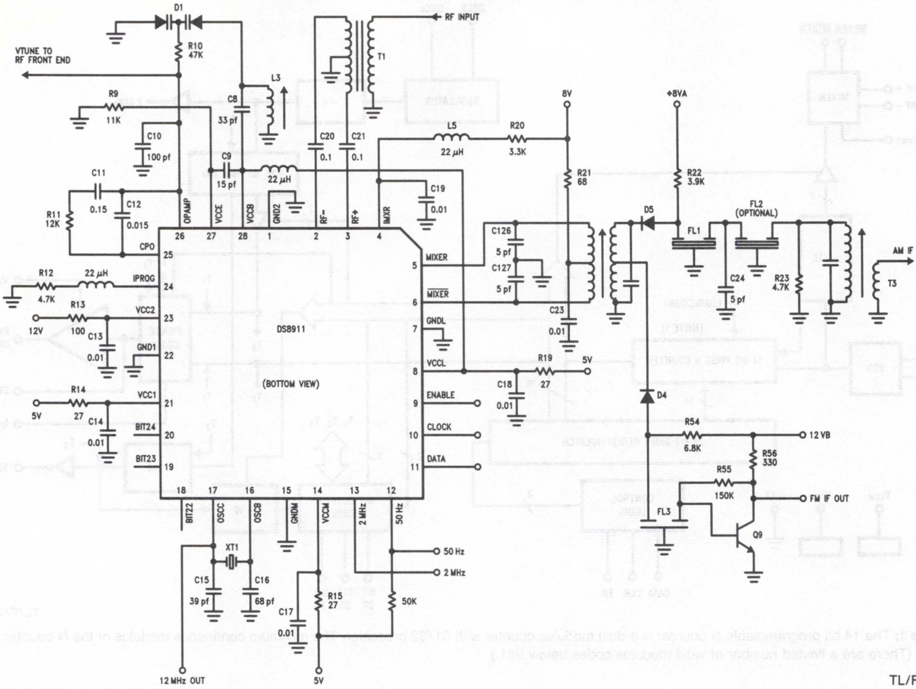
AM/FM ETR Radio Application


ANTENNA
FM AMP
AM AMP
LOOP FILTER
DISPLAY DRIVER
DISPLAY
DS8911 PLL
SERIAL DATA
2 MHz CLOCK
MICROPROCESSOR
12 MHz CRYSTAL
450 KHz C. FILTER
11.50 MHz CERAMIC FILTER
FRONT PANEL CONTROL
11.55 MHz CRYSTAL FILTER
AM 2nd MIXER
AM IF & DETECTOR
AM AUDIO
11.50 MHz CERAMIC FILTER
FM IF & DETECTOR
FM AUDIO

TL/F/7398–5

Wiring Diagrams

Configuration Using PLL and First Mixer Functions


D1
R10
47K
VTUNE TO
RF FRONT END
R9
11K
C8
33 pf
L3
RF INPUT
T1
C10
100 pf
C20
0.1
C21
0.1
L5
22 µH
R20
3.3K
8V
+8VA
C9
15 pf
22 µH
C11
0.15
C12
0.015
R11
12K
C19
0.01
R21
68
R22
3.9K
D5
FL2
(OPTIONAL)
FL1
OPAMP
VCCE
VCCB
GND2
RF−
RF+
IMXR
26
27
28
1
2
3
4
CPO
25
C126
5 pf
C127
5 pf
MIXER
5
MIXER
6
C24
5 pf
R23
4.7K
AM IF OUT
T3
R12
4.7K
22 µH
IPROG
24
R13
12V
100
VCC2
23
C13
0.01
GND1
22
C23
0.01
GNDL
7
DS8911
R19
27
5V
VCCL
8
C18
0.01
(BOTTOM VIEW)
ENABLE
9
D4
R14
5V
27
VCC1
21
C14
0.01
BIT24
20
CLOCK
10
R54
6.8K
12 VB
R56
330
BIT23
19
DATA
11
R55
150K
FM IF OUT
18
17
16
15
14
13
12
BIT22
OSCC
OSCB
GNDM
VCCM
2 MHz
50 Hz
FL3
Q9
XT1
50 Hz
2 MHz
C15
39 pf
C16
68 pf
R15
27
50K
C17
0.01
12 MHz OUT
5V

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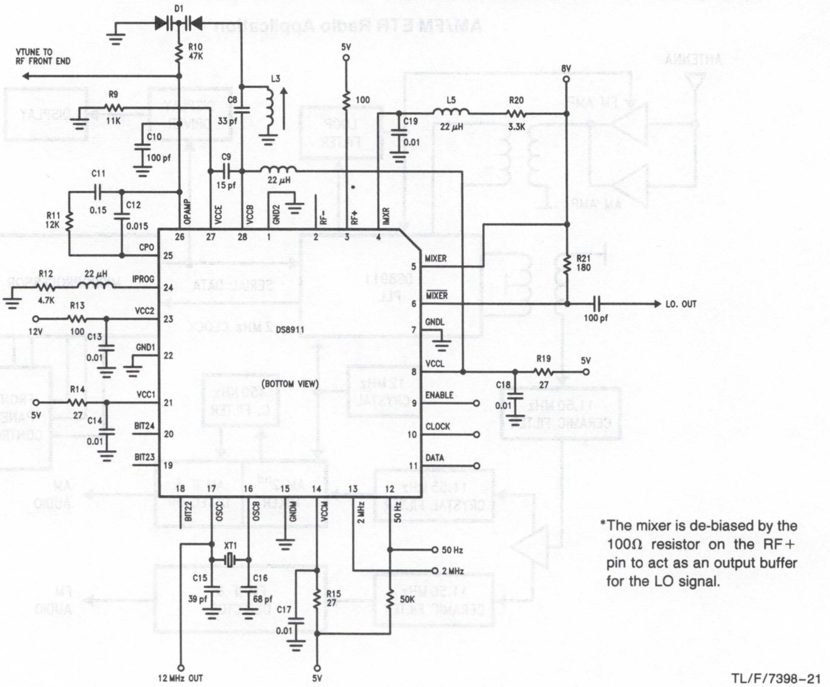
Configuration Using PLL with LO Bypassing Mixer


D1
R10
47K
VTUNE TO
RF FRONT END
5V
L3
8V
100
R9
11K
C8
33 pf
C19
0.01
L5
22 µH
R20
3.3K
C10
100 pf
C9
15 pf
22 µH
C11
0.15
C12
0.015
R11
12K
OPAMP
VCCE
VCCB
GND2
RF−
RF+
IMXR
26
27
28
1
2
3
4
CPO
25
MIXER
5
R21
180
R12
4.7K
22 µH
IPROG
24
MIXER
6
LO. OUT
100 pf
R13
12V
100
VCC2
23
DS8911
GNDL
7
C13
0.01
GND1
22
R19
27
5V
VCCL
8
(BOTTOM VIEW)
C18
0.01
R14
5V
27
VCC1
21
ENABLE
9
C14
0.01
BIT24
20
CLOCK
10
BIT23
19
DATA
11
18
17
16
15
14
13
12
BIT22
OSCC
OSCB
GNDM
VCCM
2 MHz
50 Hz
XT1
50 Hz
2 MHz
C15
39 pf
C16
68 pf
R15
27
50K
C17
0.01
12 MHz OUT
5V

*The mixer is de-biased by the 100Ω resistor on the RF+ pin to act as an output buffer for the LO signal.

TL/F/7398–21

Digital PLL Synthesis

National Semiconductor
Application Note 335
Craig Davis
Tom Mills
Keith Mueller

I. System Concepts

INTRODUCTION

Digital tuning systems are fast replacing the conventional mechanical systems in AM/FM and television receivers. The desirability of the digital approach is mainly due to the following features:

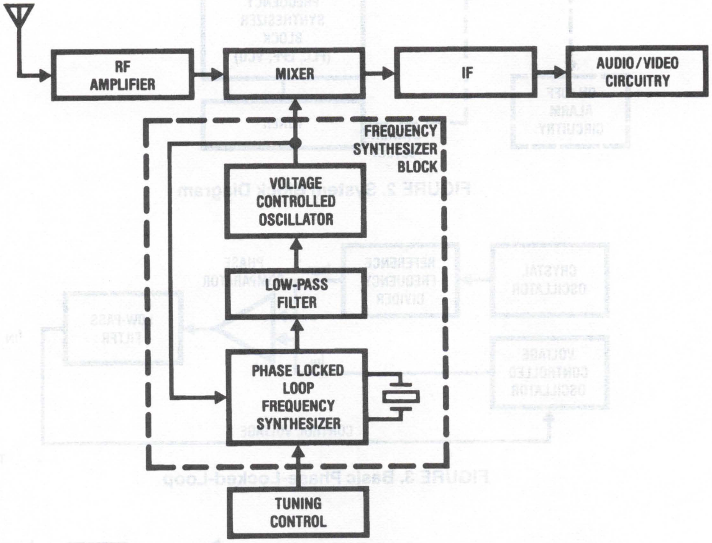
- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive. System partitioning is extremely important in optimizing this cost-benefit picture, as will be discussed.

SYSTEM DESCRIPTION

A simplified block diagram of a typical digitally tuned receiver is shown in *Figure 1*. Notice this receiver could be one for AM, FM, marine radio, or television; it makes no difference. The frequency synthesizer block generates the local oscillator frequency for the receiver, just as a conventional mechanical tuner would. However, the phase-locked-loop (PLL) acts as an integral frequency multiplier of an accurate crystal controlled reference frequency while the mechanical type provides a continuously variable frequency output with no reference. Some method of controlling the value of the multiplier for channel tuning must be provided. The other RF, IF, and audio/video circuitry will be the same as in the mechanical tuning method.

There are many different ways to partition the frequency synthesizer system to perform the digital tuning function.


RF AMPLIFIER
MIXER
IF
AUDIO/VIDEO CIRCUITRY
FREQUENCY SYNTHESIZER BLOCK
VOLTAGE CONTROLLED OSCILLATOR
LOW-PASS FILTER
PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
TUNING CONTROL

TL/F/5269–1

FIGURE 1. Block Diagram of a Digitally Tuned Receiver

PROGRAMMABLE CONTROLLER FUNCTION

The most cost-effective application of different IC process technologies is shown in *Figure 2*. The controller is separate from the PLL. The controller can be as simple as a mask programmable microcontroller* or as complicated as a high-powered microprocessor system. It can be done most economically with NMOS technology because of the logic density possible and the small size of the RAM/ROM memory cells. It could also be CMOS for extremely low power consumption in standby mode.

BASIC PHASE-LOCKED-LOOP FUNCTION

The DS8906/7/8 series of PLLs utilize a dual-modulus frequency synthesis technique. The reasons for this and the PLL itself will now be discussed.

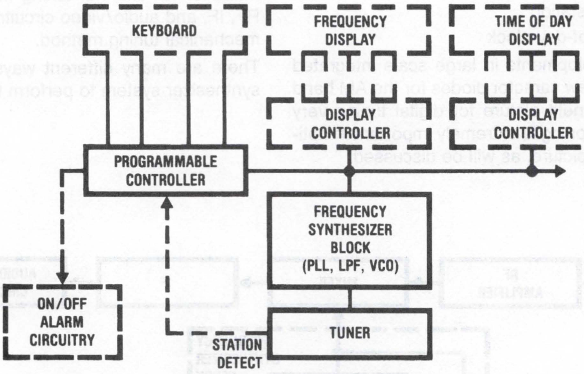
Figure 3 is a diagram of the most simple phase-locked-loop. A particular reference frequency is generated by a crystal oscillator and some fixed divider, and this goes into one side of a digital phase comparator. A voltage controlled oscillator (VCO) feeds directly into the other input of the phase comparator. The output of the phase comparator is an error signal which is filtered and fed back to the VCO as a DC control voltage.

In lock, the phase error must be zero, so f_{IN} equals f_{REF}. This system provides only one output frequency, that being equal to the reference frequency.

Figure 4 is basically the same but now a programmable divide-by-N counter is between the VCO and the phase comparator. The input to the phase comparator (f_{IN}) now becomes the output frequency of the VCO (f_{OUT}) divided by N, where N is the division code loaded into the programmable counter. This means f_{OUT}/N must equal f_{REF}. Thus, the VCO output frequency becomes N × f_{REF}, and f_{OUT} can now be changed in integral steps of f_{REF} by merely changing N.

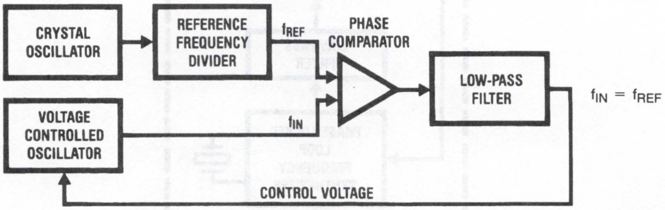
---

*Such as National's COP™ family.


KEYBOARD
FREQUENCY DISPLAY
TIME OF DAY DISPLAY
DISPLAY CONTROLLER
DISPLAY CONTROLLER
PROGRAMMABLE CONTROLLER
FREQUENCY SYNTHESIZER BLOCK (PLL, LPF, VCO)
ON/OFF ALARM CIRCUITRY
TUNER
STATION DETECT

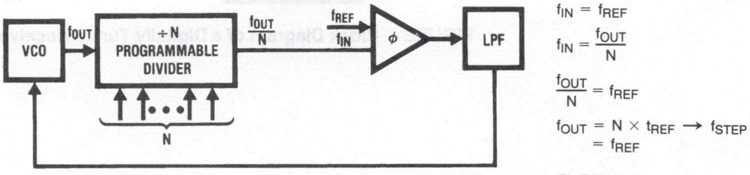
TL/F/5269–2

FIGURE 2. System Block Diagram


CRYSTAL OSCILLATOR
REFERENCE FREQUENCY DIVIDER
fREF
PHASE COMPARATOR
LOW-PASS FILTER
fIN = fREF
VOLTAGE CONTROLLED OSCILLATOR
fIN
CONTROL VOLTAGE

TL/F/5269–3

FIGURE 3. Basic Phase-Locked-Loop

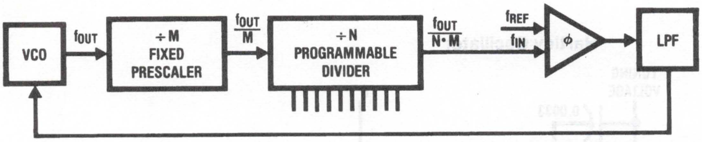

VCO
fOUT
÷N PROGRAMMABLE DIVIDER
fOUT/N
fREF
fIN
φ
LPF
N
fIN = fREF
fIN = fOUT/N
fOUT/N = fREF
fOUT = N × tREF → fSTEP = fREF

TL/F/5269–4

FIGURE 4. Basic PLL Frequency Synthesizer

In applications where the output frequency desired exceeds the maximum clock frequency of available programmable dividers, a common solution is to add a prescaler preceding the programmable divider, as shown in *Figure 5*. In this case $f_{OUT} = N (M \times f_{REF})$ and so the output frequency step size becomes $M \times f_{REF}$. So, while this technique allows higher frequency operation, it does so at the expense of either increased channel spacing for a given reference frequency, or decreased reference frequency if a specific channel spacing is required. This latter limitation is often undesirable as it can cause increased lock-on time, decreased scanning rates, and sidebands at undesirable frequencies.

Figure 6 shows the basic dual-modulus scheme. Here, a dual-modulus prescaler is substituted for the fixed prescaler and the modulus is controlled by programmable counters. The advantage to this approach is that the step size is again equal to the reference frequency while the prescaling still allows the programmable counters to operate at lower frequencies. As in the fixed prescale technique, only the prescaler needs to be high speed. The DS8906/7/8 prescale by 7/8 for AM and in a similar fashion by 63/64 in FM.



VCO
fOUT
÷M
FIXED
PRESCALER
fOUT/M
÷N
PROGRAMMABLE
DIVIDER
fOUT/N·M
fREF
fIN
φ
LPF

$f_{IN} = f_{REF}$

$f_{IN} = \frac{f_{OUT}}{N \times M}$

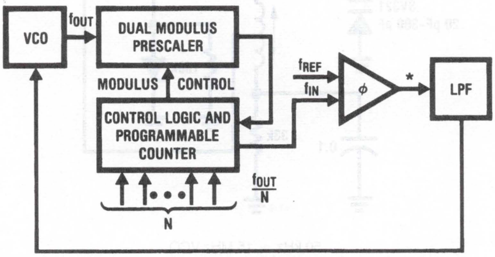
$\frac{f_{OUT}}{N \times M} = f_{REF}$

$f_{OUT} = (N \times M) f_{REF}$

$f_{OUT} = N (M \times f_{REF}) \rightarrow f_{STEP} = M \times f_{REF}$

TL/F/5269-5

FIGURE 5. PLL Frequency Synthesizer with Fixed Prescaler



VCO
fOUT
DUAL MODULUS
PRESCALER
MODULUS
CONTROL
CONTROL LOGIC AND
PROGRAMMABLE
COUNTER
N
fOUT/N
fREF
fIN
φ
*
LPF

$f_{IN} = \frac{f_{OUT}}{N} = f_{REF}$

$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP} = f_{REF}$

*if $f_{REF} = f_{IN}$, then "tuned"

if $f_{REF} \neq f_{IN}$, then "not tuned"

TL/F/5269-6

FIGURE 6. Basic Dual-Modulus Frequency Synthesizer

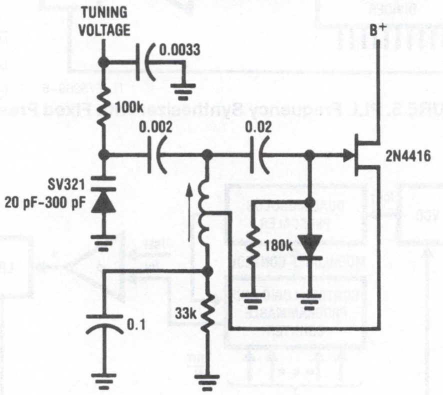
II. Application Hints

VOLTAGE CONTROLLED OSCILLATORS

In all radio and television applications, the voltage controlled oscillator (VCO) is a varactor tuned, LC type of circuit. The LC circuit is used over the various RC current controlled circuits because of their superior noise characteristics. *Figure 7* shows a collection of popular VCOs used in radio and television tuners. The AM VCO is a Hartley design chosen for wide tuning range. Commonly used varactors will show a capacitance change of 350 pF at 1V to 20 pF at 8V, which if used in a low capacitance oscillator circuit, can produce a tuning range approaching 3 to 1.

In the higher frequency ranges, above 50 MHz, Colpitts oscillators are used because stray circuit capacitance will be in parallel with desired feedback capacitance and not cause undesirable spurious resonances that might occur with the tapped coil Hartley design. The FM VCO shown is a grounded base design with feedback from collector to emitter. A UHF television oscillator is also shown. It too is a grounded base oscillator, but using a transmission line as the resonant element instead of a coil. The transmission line and tuning capacitors are arranged in π network which offers improved noise characteristics over a parallel tuned circuit. This circuit will tune over almost an octave.

Hartley Oscillator

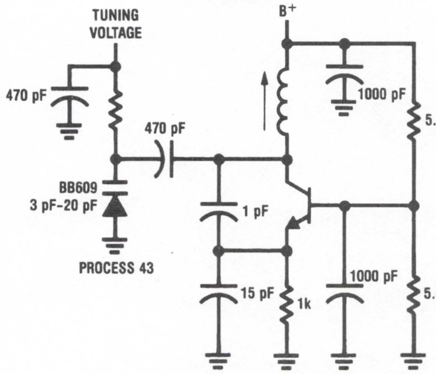

TUNING VOLTAGE
0.0033
B+
100k
0.002
0.02
2N4416
SV321
20 pF-300 pF
180k
33k
0.1

TL/F/5269-7

50 kHz ~ 15 MHz VCO

Tuning range ≅ 3:1

Colpitts Oscillator

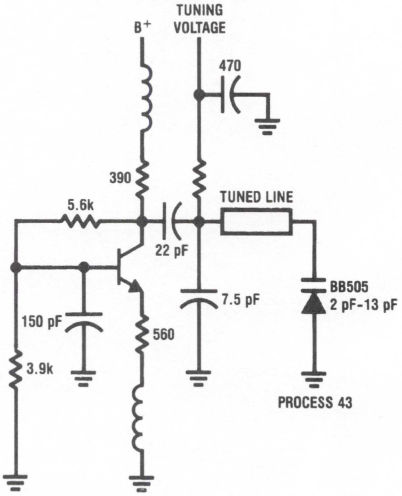

TUNING VOLTAGE
B+
470 pF
1000 pF
470 pF
5.6k
BB609
3 pF-20 pF
1 pF
PROCESS 43
1000 pF
15 pF
1k
5.6k

TL/F/5269-8

50 MHz ~ 300 MHz VCO

Tuning range ≅ 2:1

Colpitts Oscillator


B+
TUNING VOLTAGE
470
390
5.6k
TUNED LINE
22 pF
BB505
2 pF-13 pF
7.5 pF
150 pF
560
3.9k
PROCESS 43

TL/F/5269-9

500 MHz ~ 1000 MHz VCO

Tuning range ≅ 1.8:1

FIGURE 7. Typical VCO Circuits (Typical Values Shown)

PLL LOOP FILTER CALCULATIONS

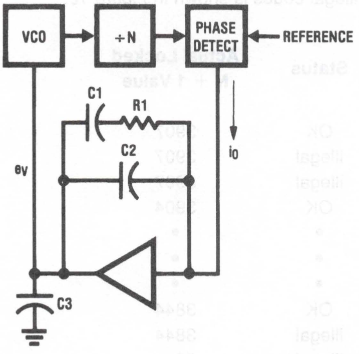
Andrzej Przedpelski, in two articles published in Electronic Design (#19, Sept. 13, 1978 and #10, May 10, 1978) explains how to calculate the three time constants associated with a third order type 2 loop which is typically used with the DS8906/7/8 series. *Figure 8* explains his method and shows a sample calculation. His articles illustrate how to calculate three time constants, and plot open loop gain and phase, and closed loop noise response.

It should be noted that VCO gain, K_V, is in terms of radians per second per volt, and phase detector gain, K_D, is in terms of amps per radian. The phase detector gain for the DS8906/7/8 series is $\pm I_{OUT}$ divided by 4π.

Figure 9 illustrates an example calculation of time constants, and a plot of open loop gain and phase based on the preceding analysis.

REFERENCES

1. Manassewitsch V., *"Frequency Synthesizers"* (Wiley, New York, 1976)
2. Rohde, A. L., *"Digital PLL Frequency Synthesizers"* (Prentice Hall, Englewood Cliffs, 1983)
3. Egan, W. F., *"Frequency Synthesis By Phase Lock"* (Wiley, New York, 1981)



TL/F/5269-10

$$T1 = R1C1$$

$$T1 = R1C2$$

$$\frac{e_V}{i_O} = \frac{1+ST1}{SC1\,(1+ST2)}$$

$$G(S) = \frac{K_D\,K_V}{NS^2C1}\left(\frac{1+ST1}{1+ST2}\right)$$

$$T2 = \frac{1-\tan\phi\cos\phi}{\omega_O\cos\phi}$$

$$T1 = \frac{1}{\omega_O{}^2T2}$$

$$C1 = \frac{K_D\,K_V}{N\omega_O{}^2}\left(\frac{-\omega_OT1-1}{\omega_OT2+1}\right)$$

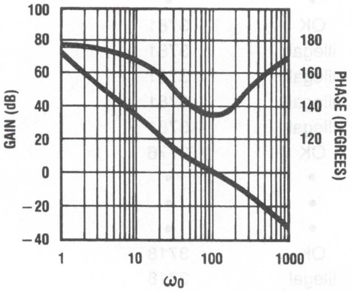
where θ = desired phase margin

ω_O = loop natural frequency

$\approx$ closed loop bandwidth

Note: DS8909 op amp required C3 $\approx$ 1000 pF for compensation.

FIGURE 8. Third Order Type 2 Loop



TL/F/5269-11

VHF loop, running at 100 MHz, ref = 10 kHz

K_V = 2.5 MHz/V = 15.7 Mrad/sec/V

$$K_D = \frac{400\ \mu A}{4\pi} = 31.8\ \mu A/\text{radian}$$

$$N = \frac{100\ \text{MHz}}{10\ \text{kHz}} = 10{,}000,\ \omega_O = 2\pi \times 100\ \text{Hz}$$

θ = 45° (desired phase margin)

$T2 = 6.6 \times 10^{-4}$ sec

$T1 = 3.84 \times 10^{-3}$ sec

C1 = 0.3 μF

so R1 = T1/C1 = 13 kΩ

C2 = T2/R1 = 0.05 μF

FIGURE 9. Example of Gain and Phase Calculation

DUAL-MODULUS COUNTING RANGE LIMITATIONS

- Minimum count limitations
- Maximum count limitations

The DS8906/7/8 series PLLs utilize a dual-modulus counting scheme internally based on a 63/64 prescale modulus in FM mode in order that all of the U.S. FM frequency assignments could be reached using a 25 kHz reference. The counter modulus N = 64A + B where B is the 6 least significant bits of N and A is the 7th and greater significant bits of N.

$$N = 64A + B$$
$$N = 64A + \overline{63} - B \; (B = 63 - \overline{B})$$
$$1 + N = 64A + 63 + 1 - 64\overline{B} + 63\overline{B}$$
$$1 + N = 64(A + 1 - \overline{B}) + 63\overline{B}$$

The last equation is in the final form used internally by the DS8906/7/8. The equation indicates that, if N is loaded into the device, it will solve for N + 1.

The minimum continuous N modulus (code) the equation dictates should occur when $A = \overline{B}$. $\overline{B}$ maximum = 63 implies $A = \overline{62}$, B = 63 should be an illegal N + 1 code (N + 1 = 3969). However, because this is just inside the lower FM band limits, extra circuitry was added to enable this particular code's operation. The actual minimum N + 1 code for these PLLs thus becomes the case when A = 61, $\overline{B}$ = 61, N + 1 minimum = 3907. There are legitimate N + 1 codes below this 3907 value, however, they are not continuous. (i.e., Starting at 3907 and counting down, one additional code is in error every 63 codes. Thereafter, these erroneous codes are the cases where $A < \overline{B}$.) The sequence of illegal codes is shown in *Figure 10.*

Loaded Value of N	A	$\overline{B}$	Status	Actual Locked N + 1 Value
3906	61	61	OK	3907
3905	61	62	illegal	3907
3904	61	63	illegal	3907
3903	60	0	OK	3904
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3843	60	60	OK	3844
3842	60	61	illegal	3844
3841	60	62	illegal	3844
3840	60	63	illegal	3844
3839	59	0	OK	3840
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3780	59	59	OK	3781
3779	59	60	illegal	3781
3778	59	61	illegal	3781
3777	59	62	illegal	3781
3776	59	63	illegal	3781
3775	58	0	OK	3776
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3717	58	58	OK	3718
3716	58	59	illegal	3718
3715	58	59	illegal	3718
3714	58	60	illegal	3718
3713	58	61	illegal	3718
3712	58	63	illegal	3718
3711	57	0	OK	3712
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

FIGURE 10. FM Mode Dual-Modulus Counting Below the Minimum Continuous N Code of 3906

Maximum code limits for these dual-modulus PLLs are determined by the N code bit length. The DS8906 and DS8908 have a 14-bit N counter allowing 16,383 counts. The DS8907 has a 13-bit N node length, allowing a maximum N count of 8,191. See *Figure 11* for table operating ranges of the DS8906, DS8907 and DS8908 PLLs.

CONCLUSION

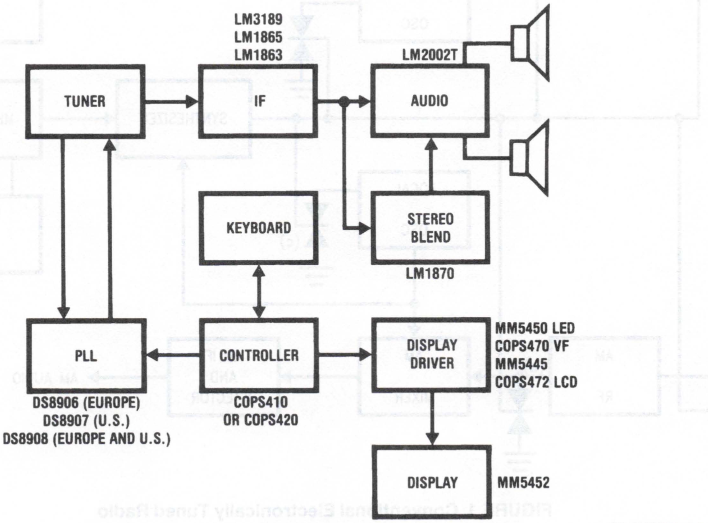
The major application for the DS8906/7/8 PLLs are synthesizers for AM-FM radios, and have been widely accepted in the marketplace. *Figure 12* shows the block diagram of such a radio. In this application the following performance relating to the PLL tuning system is realized.

PLL Loop Bandwidth	300 Hz
Reference Frequency Sidebands	>60 dB
Signal-to-Noise Ratio	
AM: 30% modulation	>50 dB
FM: 22.5 kHz deviation	>55 dB
Switching Speed (one channel)	<1.5 ms

Product	Input	Ref (Hz)	f_{IN} (Hz)	
			Min*	Max
DS8906	AM	500	24.5k	8.193M
	FM	12.5k	48.8375M	120M
DS8907	AM	10k	490k	15M
	FM	25k	97.675M	120M
DS8908	AM	1k	49k	15M
		9k	441k	15M
		10k	490k	15M
		20k	980k	15M
	FM	1k	3.907M	15M
		9k	35.163M	120M
		10k	39.07M	120M
		20k	78.14M	120M

*The minimum frequency shown is obtained when the minimum continuous N code is utilized and it assumes the edge rates >20V/μs.

FIGURE 11. Product Operating Frequency Range


LM3189
LM1865
LM1863
LM2002T
TUNER
IF
AUDIO
KEYBOARD
STEREO BLEND
LM1870
PLL
CONTROLLER
DISPLAY DRIVER
MM5450 LED
COPS470 VF
MM5445
COPS472 LCD
DS8906 (EUROPE)
DS8907 (U.S.)
DS8908 (EUROPE AND U.S.)
COPS410
OR COPS420
DISPLAY
MM5452

TL/F/5269–12

FIGURE 12. AM-FM Digitally Tuned Radio System

DS8911 AM/FM/TV Sound Up-Conversion Frequency Synthesizer

National Semiconductor
Application Note 512

INTRODUCTION

This application note describes an AM/FM radio implemented using the DS8911 Up-Conversion Frequency Synthesizer. This synthesizer was designed to utilize up-conversion techniques to reduce the manufacturing costs and labor requirements associated with alignment of an AM radio front end.

The conventional high performance AM radio requires at least three tuned circuits for AM reception (see *Figure 1*). These tuned circuits include 3 varactor diodes which must be matched to ensure tracking over a wide Local Oscillator (LO) operating range. The cost of these matched varactors and labor associated with alignment of the three stages is significant.

The three circuits are:

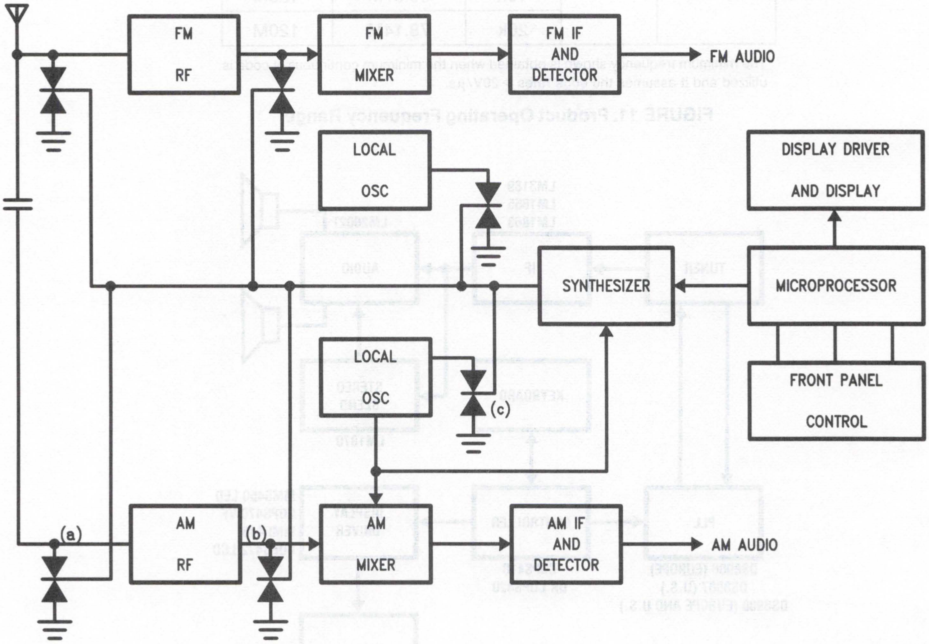
a. RF antenna input
b. RF amplifier output
c. Local oscillator

THE UP-CONVERSION AM RADIO USING THE DS8911

In an up-conversion AM radio the local oscillator and first IF frequency are chosen to be much higher in frequency than the received signal. This totally eliminates image problems since the image is far above the band of interest. In this application an IF of 11.55 MHz was chosen. This enables the RF front end to be untuned. A simple low pass filter is included to roll off frequencies above 2 MHz. The first mixer in an up-conversion design is subjected to the entire AM band and thus a very high dynamic range mixer (provided as part of the DS8911) is essential to prevent overload due to strong signals. *Figure 2* shows the block diagram of the radio using an up-conversion scheme. Notice the three AM tuned stages mentioned in the conventional down-conversion scheme have been eliminated.

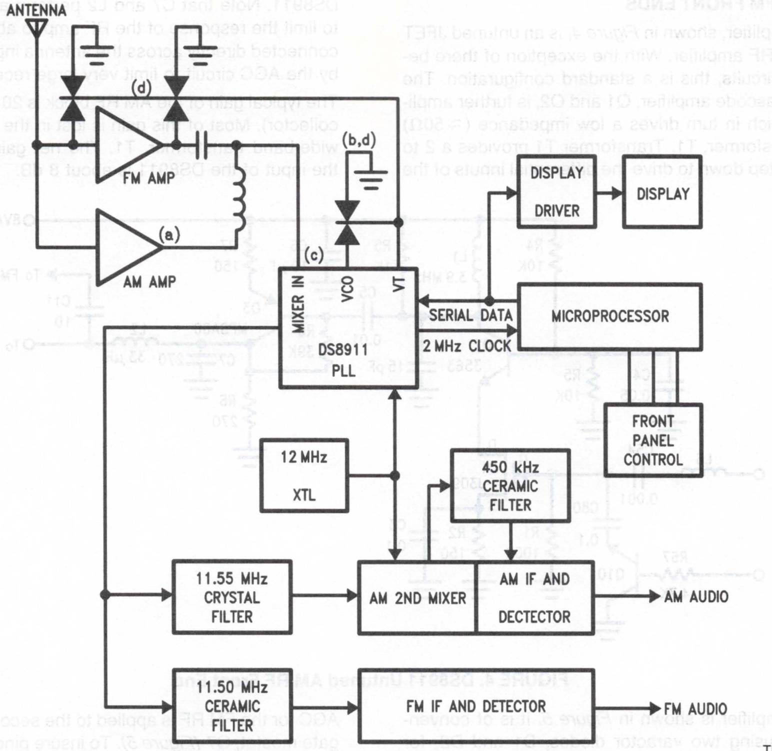
Note the dramatic simplification summarized below:

a. Untuned AM RF amplifier
b. One VCO internally generates the LO for both AM and FM modes
c. A common AM/FM mixer
d. Reduced number of tuning and tracking adjustments



TL/F/9449-1

FIGURE 1. Conventional Electronically Tuned Radio

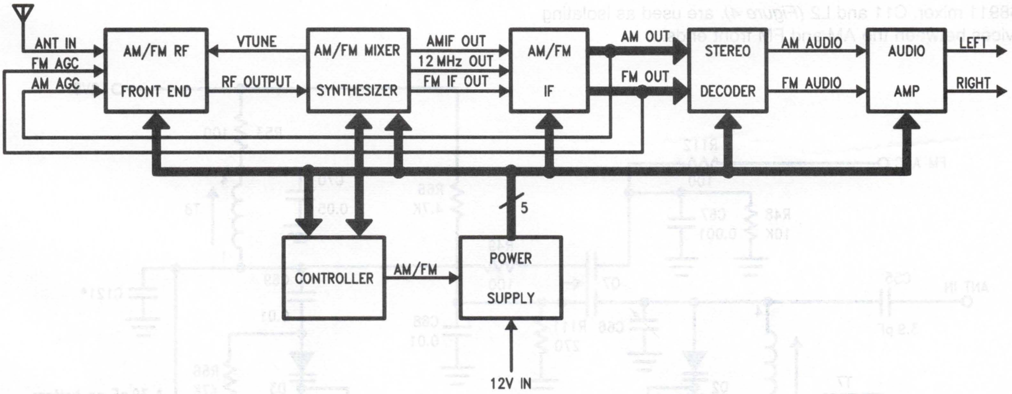

ANTENNA
(d)
FM AMP
(b,d)
(a)
AM AMP
(c)
MIXER IN
VCO
VT
DS8911
PLL
SERIAL DATA
2 MHz CLOCK
DISPLAY
DRIVER
DISPLAY
MICROPROCESSOR
FRONT
PANEL
CONTROL
12 MHz
XTL
450 kHz
CERAMIC
FILTER
11.55 MHz
CRYSTAL
FILTER
AM 2ND MIXER
AM IF AND
DECTECTOR
AM AUDIO
11.50 MHz
CERAMIC
FILTER
FM IF AND DETECTOR
FM AUDIO

TL/F/9449-2

FIGURE 2. Up-Conversion Electronically Tuned Radio

THE DS8911 IN AN ACTUAL RECEIVER APPLICATION

Shown below is a block diagram of the DS8911 demonstration radio.


ANT IN
FM AGC
AM AGC
AM/FM RF
FRONT END
VTUNE
RF OUTPUT
AM/FM MIXER
SYNTHESIZER
AMIF OUT
12 MHz OUT
FM IF OUT
AM/FM
IF
AM OUT
FM OUT
STEREO
DECODER
AM AUDIO
FM AUDIO
AUDIO
AMP
LEFT
RIGHT
CONTROLLER
AM/FM
POWER
SUPPLY
5
12V IN

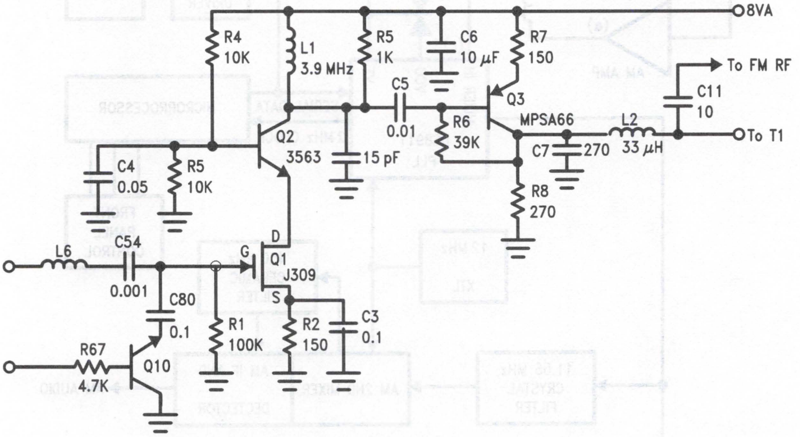
TL/F/9449-3

FIGURE 3. Block Diagram of DS8911 Up-Conversion Radio

THE AM AND FM FRONT ENDS

The AM RF amplifier, shown in *Figure 4,* is an untuned JFET input cascode RF amplifier. With the exception of there being no tuned circuits, this is a standard configuration. The output of the cascode amplifier, Q1 and Q2, is further amplified by Q3, which in turn drives a low impedance ($\approx 50\Omega$) wide band transformer, T1. Transformer T1 provides a 2 to 1 impedance step down to drive the differential inputs of the DS8911. Note that C7 and L2 perform a low pass function to limit the response of the RF amp to about 2 MHz. Q10 is connected directly across the antenna input and is activated by the AGC circuit to limit very large received signals.

The typical gain of the AM RF block is 20 dB (antenna to Q3 collector). Most of this gain is lost in the low pass filter and wide-band transformer, T1. The net gain from antenna to the input of the DS8911 is about 8 dB.


8VA
R4
10K
L1
3.9 MHz
R5
1K
C6
10 μF
R7
150
To FM RF
C5
0.01
Q3
C11
10
Q2
3563
15 pF
R6
39K
MPSA66
L2
33 μH
To T1
C7
270
C4
0.05
R5
10K
R8
270
L6
C54
0.001
G
D
Q1
J309
S
C80
0.1
R1
100K
R2
150
C3
0.1
R67
4.7K
Q10

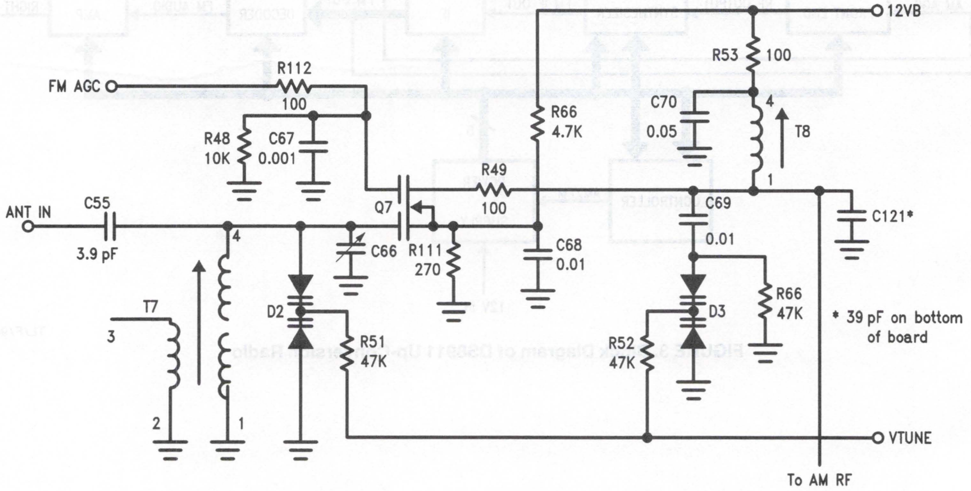
TL/F/9449-4

FIGURE 4. DS8911 Untuned AM RF Front End

The FM RF amplifier is shown in *Figure 5.* It is of conventional design, using two varactor diodes, D1 and D2, for tuning. These diodes and the LO varactor, D1, are driven directly by the DS8911 Mixer/Synthesizer's tuning voltage output (OPAMP OUT).

Note that the wide-band transformer, T1, shown in *Figure 6,* serves as both the AM and FM differential input for the DS8911 mixer. C11 and L2 *(Figure 4),* are used as isolating devices between the AM and FM front ends.

AGC for the FM RF is applied to the second gate of the dual gate mosfet, Q7 *(Figure 5).* To insure pinch off action during AGC, R68 biases the source of Q7 so that the source cannot drop below about 650 mV. Note that R49 is used in the drain of Q7. This is designed to limit gain and add circuit stability. The approximate gain of the FM RF amplifier is 10 dB.


12VB
R53
100
FM AGC
R112
100
C70
0.05
4
T8
R66
4.7K
R48
10K
C67
0.001
R49
100
1
ANT IN
C55
3.9 pF
Q7
C69
0.01
C121*
4
C66
R111
270
C68
0.01
T7
3
D2
R51
47K
D3
R66
47K
* 39 pF on bottom of board
R52
47K
2
1
VTUNE
To AM RF

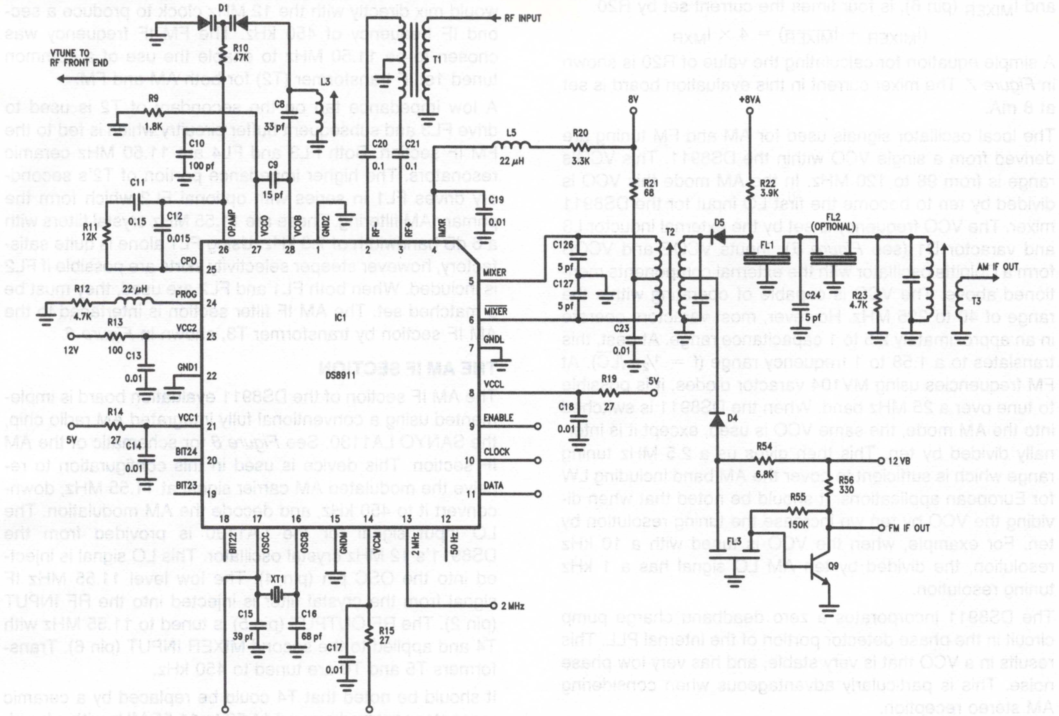
TL/F/9449-5

FIGURE 5. FM RF Front End

THE DS8911 MIXER AND IF FILTER SECTION

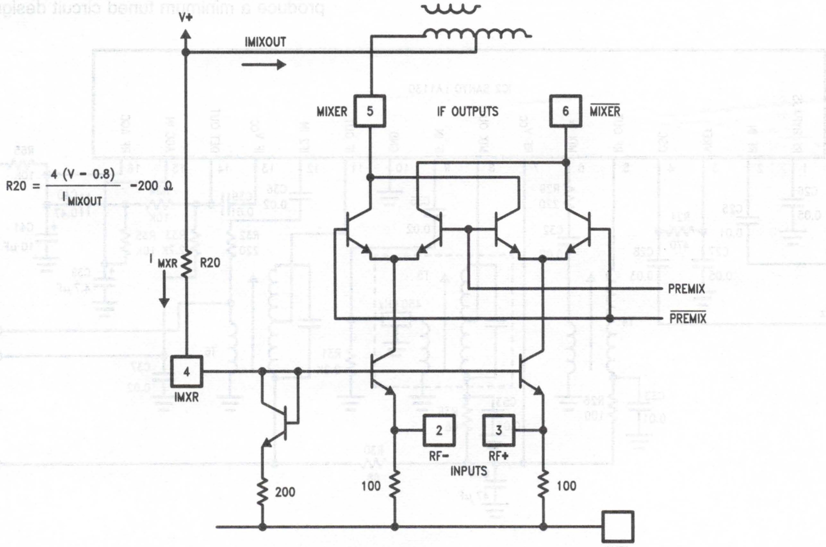
A mixer is provided on the DS8911 IC for both the FM conversion to 11.50 MHz and the AM first conversion to 11.55 MHz. The 2nd AM conversion to 450 kHz is provided by the mixer within the AM IF IC. If other partitioning constraints require that the first mixer be external to the DS8911, the RF inputs of the mixer can be de-biased which results in passing the internally generated LO signal to the mixer output pins.

The DS9811 Mixer/Synthesizer section is shown in *Figure 6.*


RF INPUT
VTUNE TO RF FRONT END
D1
R10 47K
T1
L3
R9 1.8K
C8 33 pf
C10 100 pf
C9 15 pf
C11
C20 0.1
C21 0.1
L5 22 µH
R20 3.3K
8V
+8VA
R21 68
R22 3.9K
C19 0.01
R11 12K
0.15
C12 0.015
OPAMP
VCCO
VCCB
GND2
RF−
RF+
IMXR
26 27 28 1 2 3 4
CPO 25
T2
D5
FL1
FL2 (OPTIONAL)
AM IF OUT
T3
C126 5 pf
C127 5 pf
C24 5 pf
R23 4.7K
C23 0.01
MIXER 5
MIXER 6
GNDL 7
VCCL 8
ENABLE 9
CLOCK 10
DATA 11
R12 4.7K
22 µH
PROG 24
R13 100
VCC2 23
12V
C13 0.01
GND1 22
IC1
DS8911
R19 27
5V
C18 0.01
D4
R14 27
VCC1 21
C14 0.01
BIT24 20
BIT23 19
R54 6.8K
12 VB
R56 330
R55 150K
FM IF OUT
FL3
Q9
18 17 16 15 14 13 12
BIT22 OSCC OSCB GNDM VCCM 2 MHz 50 Hz
XT1
C15 39 pf
C16 68 pf
2 MHz
R15 27
C17 0.01
12 MHz OUT
5V

TL/F/9449–6

FIGURE 6. DS8911 Mixer/Synthesizer Section


V+
4
IMIXOUT
MIXER 5
IF OUTPUTS
6 MIXER
R20 = 4 (V − 0.8) / IMIXOUT − 200 Ω
IMXR
R20
PREMIX
PREMIX
4
IMXR
2 RF−
3 RF+
INPUTS
200
100
100
GNDL

TL/F/9449–7

FIGURE 7. Mixer Bias Circuitry

The DS8911 double balanced mixer is differentially driven by center-tapped T1 into the RF+ and RF− inputs. These are emitter inputs with an approximate impedance of 25Ω.

Current through the double balanced mixer is set by R20, shown in *Figure 7.* The total bias current through the sum of the mixer transistors whose collectors are at $I_{\overline{MIXER}}$ (pin 5) and I_{MIXER} (pin 6), is four times the current set by R20.

$$(I_{MIXER} + I_{\overline{MIXER}}) = 4 \times I_{MXR}$$

A simple equation for calculating the value of R20 is shown in *Figure 7.* The mixer current in this evaluation board is set at 8 mA.

The local oscillator signals used for AM and FM tuning are derived from a single VCO within the DS8911. This VCO's range is from 98 to 120 MHz. In the AM mode this VCO is divided by ten to become the first LO input for the DS8911 mixer. The VCO frequency is set by the external inductor L3 and varactor D1 (see *Figure 6*). Inputs VCOE and VCOB form a Colpitts oscillator with the external components mentioned above. The VCO is capable of operating within the range of 40 to 225 MHz. However, most varactors operate in an approximately 2.5 to 1 capacitance range. At best, this translates to a 1.58 to 1 frequency range ($f = \frac{1}{2}\pi\sqrt{LC}$). At FM frequencies using MV104 varactor diodes, it is possible to tune over a 25 MHz band. When the DS8911 is switched into the AM mode, the same VCO is used, except it is internally divided by ten. This then gives us a 2.5 MHz tuning range which is sufficient to cover the AM band including LW for European applications. It should be noted that when dividing the VCO by ten we increase the tuning resolution by ten. For example, when the VCO is tuned with a 10 kHz resolution, the divided by ten AM LO signal has a 1 kHz tuning resolution.

The DS8911 incorporates a zero deadband charge pump circuit in the phase detector portion of the internal PLL. This results in a VCO that is very stable, and has very low phase noise. This is particularly advantageous when considering AM stereo reception.

DS8911 IF FILTERS

Referring to *Figure 6,* the output of the DS8911 mixer is a differential output, MIXER, $\overline{\text{MIXER}}$; pins 5 and 6 respectively. This output is applied to the center-tapped primary of T2, the mixer output transformer, which is tuned to 11.55 MHz.

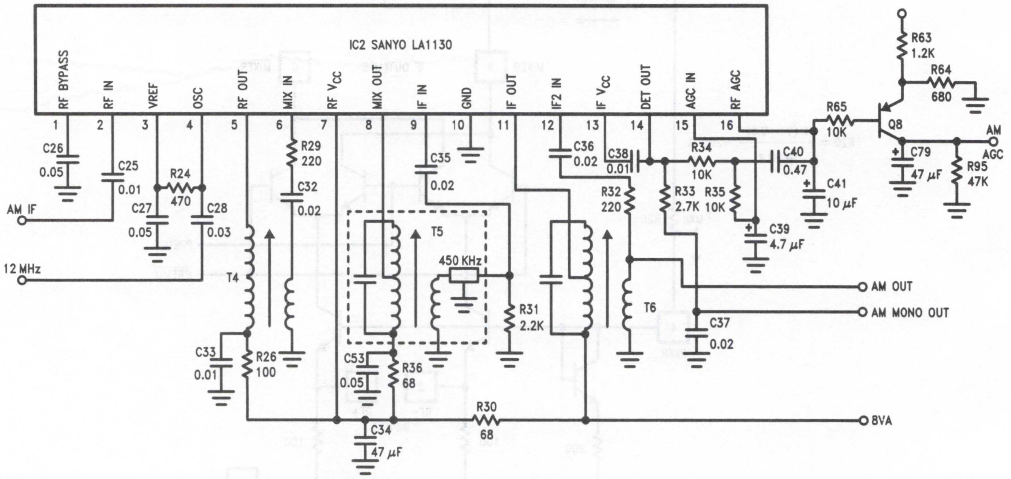
The AM IF frequency was chosen to be 11.55 MHz so that it would mix directly with the 12 MHz clock to produce a second IF frequency of 450 kHz. The FM IF frequency was chosen to be 11.50 MHz to enable the use of a common tuned 1st IF transformer (T2) for both AM and FM.

A low impedance tap on the secondary of T2 is used to drive FL3 and subsequent buffer circuitry which is fed to the FM IF section. Both FL3 and FL4 are 11.50 MHz ceramic resonators. The higher impedance portion of T2's secondary drives FL1 in series with optional FL2 which form the primary AM filtering. These are 11.55 MHz crystal filters with a 6 dB bandwidth of 7.5 kHz. Using FL1 alone is quite satisfactory, however steeper selectivity skirts are possible if FL2 is included. When both FL1 and FL2 are used, they must be a matched set. The AM IF filter section is interfaced to the AM IF section by transformer T3, shown in *Figure 6.*

THE AM IF SECTION

The AM IF section of the DS8911 evaluation board is implemented using a conventional fully integrated AM radio chip, the SANYO LA1130. See *Figure 8* for schematic of the AM IF section. This device is used in this configuration to receive the modulated AM carrier signal at 11.55 MHz, downconvert it to 450 kHz, and decode the AM modulation. The LO input signal for the LA1130 is provided from the DS8911's 12 MHz crystal oscillator. This LO signal is injected into the OSC pin (pin 4). The low level 11.55 MHz IF signal from the crystal filter is injected into the RF INPUT (pin 2). The RF OUTPUT (pin 5) is tuned to 11.55 MHz with T4 and applied to the second MIXER INPUT (pin 6). Transformers T5 and T6 are tuned to 450 kHz.

It should be noted that T4 could be replaced by a ceramic resonator centered around 11.50 to 11.55 MHz with a bandwidth of several hundred kHz. Transformer T5 could be eliminated and T6 replaced with a 450 kHz resonator to produce a minimum tuned circuit design.



TL/F/9449-8

FIGURE 8. AM IF Circuitry

Detected audio is available at pin 14 (Mono AM out test point). AGC is generated internal to the LA1130, buffered by Q8 and applied to Q10, located in the AM front end.

THE FM IF SECTION

The FM IF filtering is done by FL3 *(Figure 6)* and FL4 *(Figure 9)* which precede the IF amplifier chip IC6, an LM3089. FM quadrature detection is done on chip. External inductor T9 is adjusted for correct FM demodulation. Audio output is made available on pin 6 (FM mono out test point). This is fed to the stereo decoder IC8. *(Figure 11)*

THE STEREO DECODER SECTION

The stereo decoders are a standard configuration with their outputs resistively summed into the dual volume control potentiometer, R_{vol}.

Device IC7, shown in *Figure 10,* is a Motorola MC13020P, an AM stereo decoder designed to decode the C-Quam AM stereo format. Because this chip needs a relatively high level 450 kHz IF signal to operate, transistors Q4 and Q5 boost the IF signal from T6 and apply it to pin 3 of IC7.

The FM stereo decoder, shown in *Figure 11,* is IC8, an LM1800. This device performs the FM stereo multiplex decoding. This circuit is standard and used in numerous consumer applications, therefore is mentioned only briefly.

The audio output section, shown in *Figure 12,* consists of two LM386 devices, IC3 and IC11. These are used simply to drive a pair of monitor loud speakers. No special de-emphasis of the audio has been done in this evaluation board. This should be taken into account if performance measurements are done on this board.

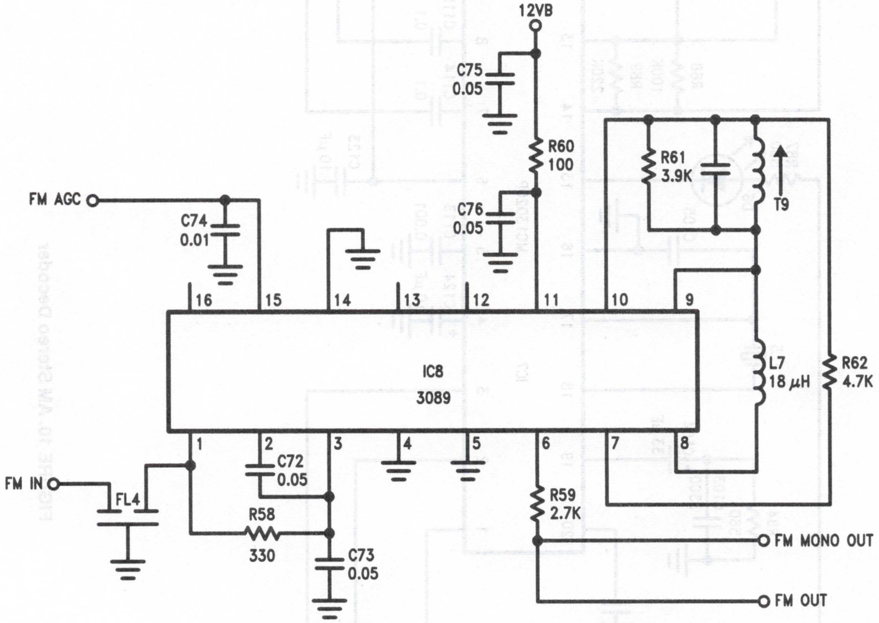


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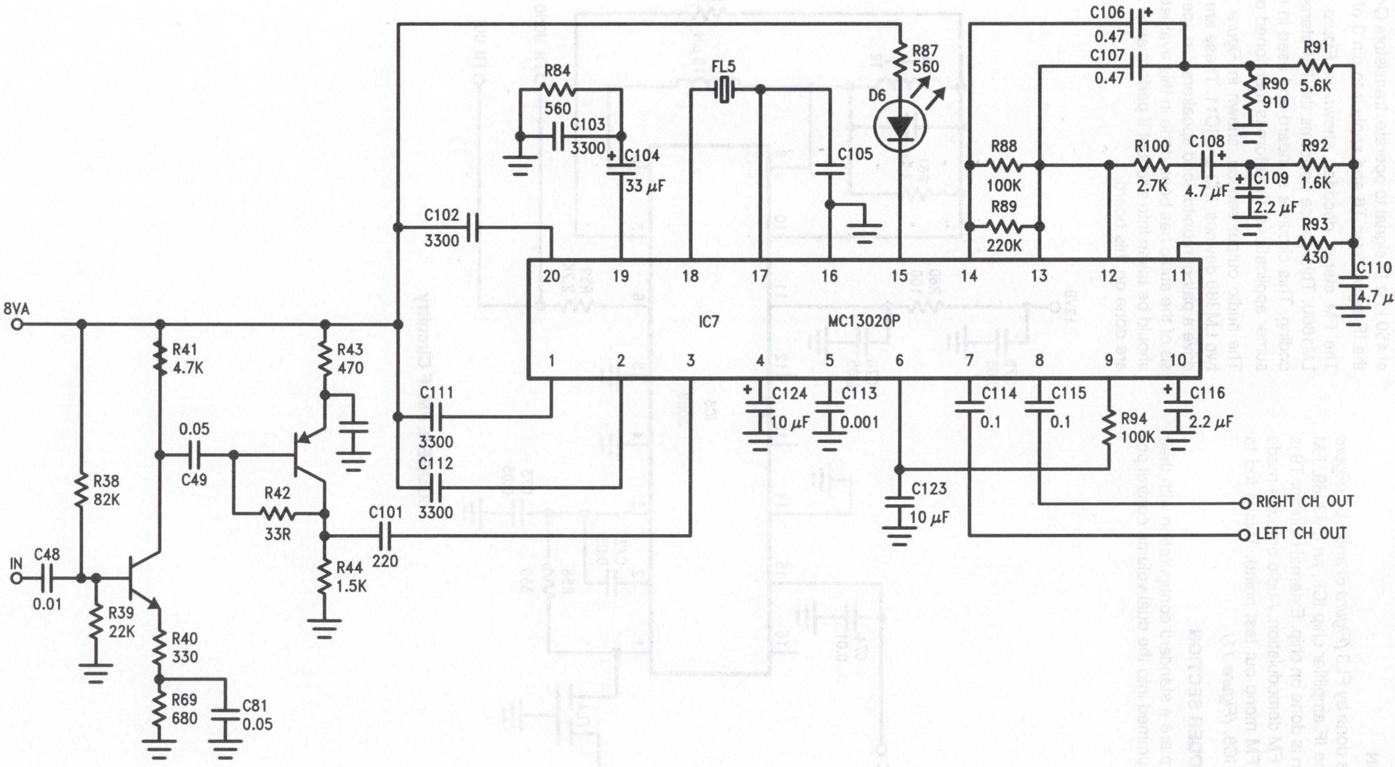
FIGURE 9. FM IF Circuitry


8VA
IN
C48
0.01
R38
82K
R39
22K
R41
4.7K
R40
330
R69
680
C81
0.05
0.05
C49
R42
33R
R43
470
R44
1.5K
C101
220
C111
3300
C112
3300
C102
3300
R84
560
C103
3300
C104
33 µF
FL5
C105
R87
560
D6
20
19
18
17
16
15
14
13
12
11
IC7
MC13020P
1
2
3
4
5
6
7
8
9
10
C124
10 µF
C113
0.001
C123
10 µF
C114
0.1
C115
0.1
R94
100K
C116
2.2 µF
R88
100K
R89
220K
R100
2.7K
C108
4.7 µF
C109
2.2 µF
C106
0.47
C107
0.47
R90
910
R91
5.6K
R92
1.6K
R93
430
C110
4.7 µF
RIGHT CH OUT
LEFT CH OUT

TL/F/9449-10

FIGURE 10. AM Stereo Decoder

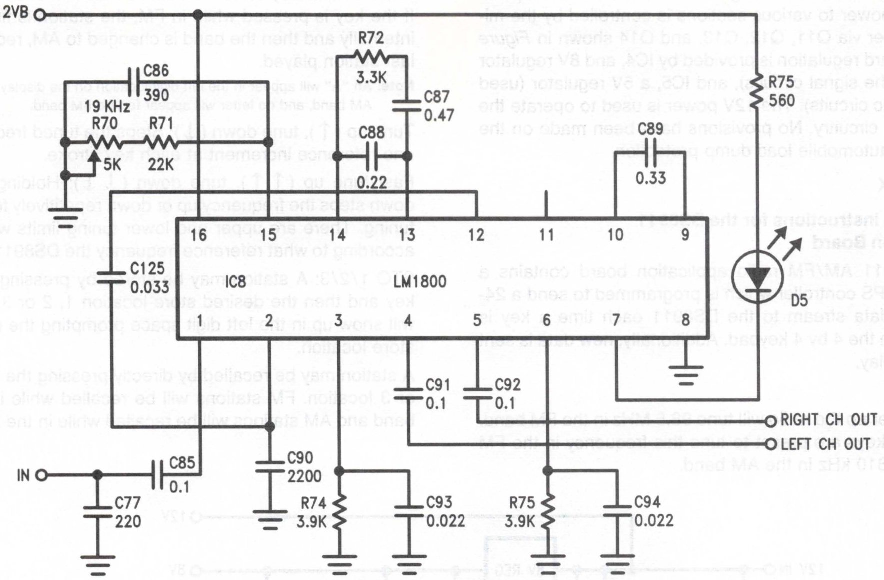

12VB
R72
3.3K
C86
390
C87
0.47
19 KHz
R70
R71
5K
22K
C88
0.22
R75
560
C89
0.33
16
15
14
13
12
11
10
9
C125
0.033
IC8
LM1800
1
2
3
4
5
6
7
8
D5
C91
0.1
C92
0.1
RIGHT CH OUT
LEFT CH OUT
IN
C85
0.1
C90
2200
C77
220
R74
3.9K
C93
0.022
R75
3.9K
C94
0.022

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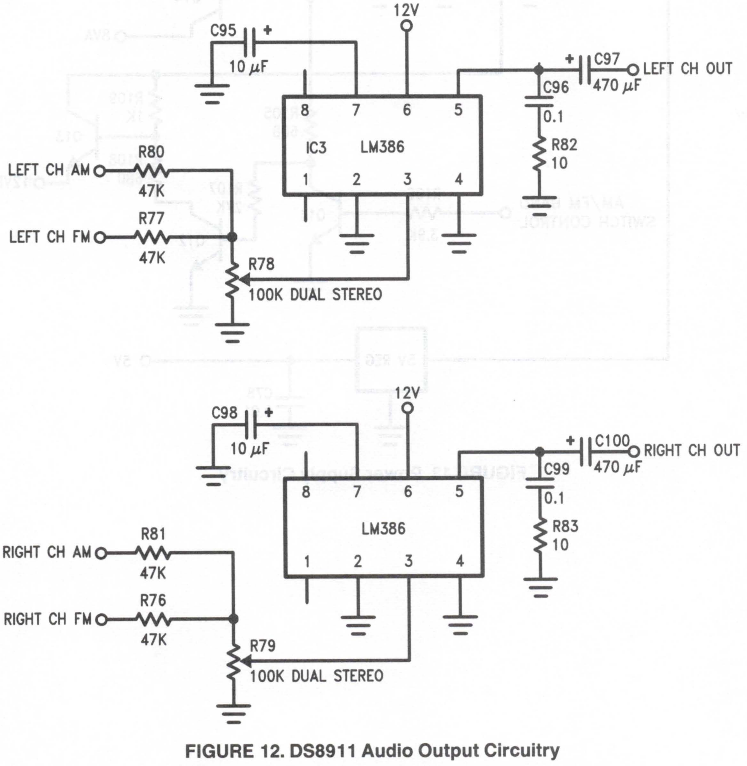
FIGURE 11. FM Stereo Decoder


12V
C95
+
10 µF
+
C97
470 µF
LEFT CH OUT
C96
0.1
R82
10
8
7
6
5
IC3
LM386
1
2
3
4
LEFT CH AM
R80
47K
LEFT CH FM
R77
47K
R78
100K DUAL STEREO
12V
C98
+
10 µF
+
C100
470 µF
RIGHT CH OUT
C99
0.1
R83
10
8
7
6
5
LM386
1
2
3
4
RIGHT CH AM
R81
47K
RIGHT CH FM
R76
47K
R79
100K DUAL STEREO

TL/F/9449–12

TL/F/9449–13

FIGURE 12. DS8911 Audio Output Circuitry

POWER SUPPLIES

The evaluation board is designed for 12 VdC nominal operation. The power to various sections is controlled by the microcontroller via Q11, Q12, Q13, and Q14 shown in *Figure 13.* On board regulation is provided by IC4, and 8V regulator (used for the signal circuits), and IC5, a 5V regulator (used for the logic circuits). The 12V power is used to operate the rest of the circuitry. No provisions have been made on the board for automobile load dump protection.

APPENDIX

Operating instructions for the DS8911 Application Board

The DS8911 AM/FM radio application board contains a built-in COPS controller which is programmed to send a 24-bit serial data stream to the DS8911 each time a key is pressed on the 4 by 4 keypad. Additionally, new data is sent to the display.

Power up.

Upon power up the radio will tune 98.5 MHz in the FM band. The store keys are preset to tune this frequency in the FM band and 810 kHz in the AM band.

Key Functions.

AM/FM: This key switches between the AM and FM bands. If the key is pressed while in FM, the station is first stored internally and then the band is changed to AM, recalling the last station played.

Note: An "A" will appear in the left digit location on the display while in the AM band, and no letter will appear for the FM band.

Tune up (↑), tune down (↓): Steps the tuned frequency by one reference increment at each key stroke.

Fast tune up (↑↑), tune down (↓↓): Holding this key down steps the frequency up or down repetitively for speedy tuning. There are upper and lower tuning limits which vary according to what reference frequency the DS8911 is using.

STO 1/2/3: A station may be stored by pressing the STO key and then the desired store location 1, 2 or 3 . An "S" will show up in the left digit space prompting the user for a store location.

A station may be recalled by directly pressing the store 1, 2 or 3 location. FM stations will be recalled while in the FM band and AM stations will be recalled while in the AM band.

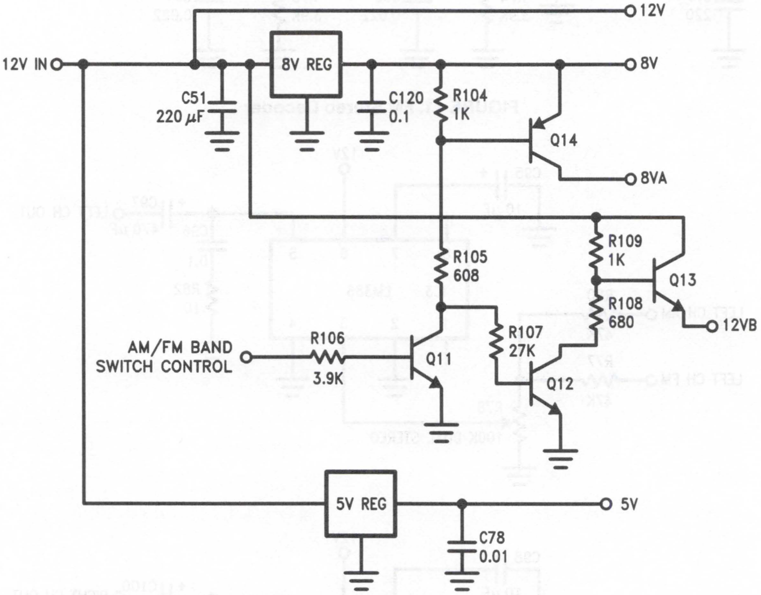


FIGURE 13. Power Supply Circuitry

Column	Row	Function
M	D	ST0
N	D	1
G	D	3
F	D	3
M	E	AMFM
N	E	LO
G	E	T/M
F	E	REF
M	P	—
N	P	B22
G	P	B23
F	P	B24
M	Q	STEP UP
N	Q	SCAN UP
G	Q	SCAN DOWN
F	Q	STEP DOWN

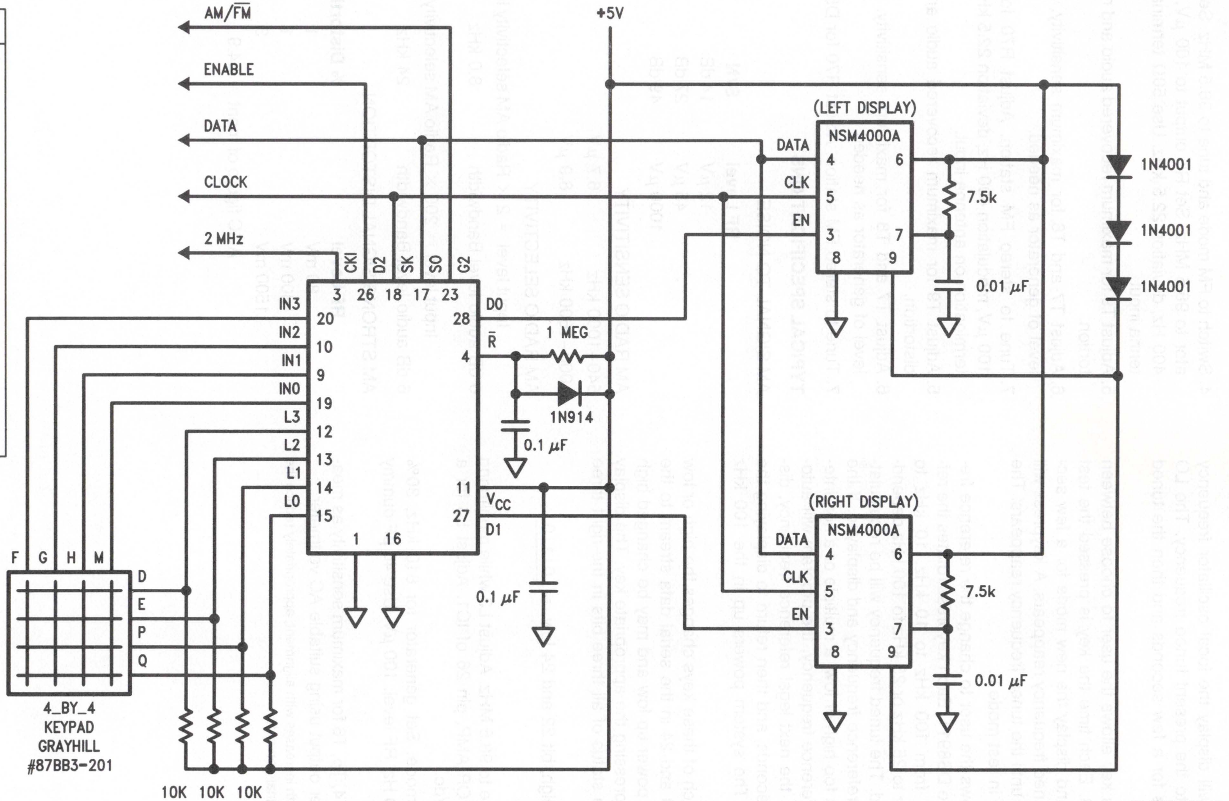

AM/$\overline{FM}$
ENABLE
DATA
CLOCK
2 MHz
+5V
CKI
D2
SK
SO
G2
3
26
18
17
23
IN3
IN2
IN1
IN0
L3
L2
L1
L0
20
10
9
19
12
13
14
15
1
16
D0
28
$\overline{R}$
4
11
V_{CC}
27
D1
1 MEG
1N914
0.1 µF
0.1 µF
(LEFT DISPLAY)
NSM4000A
DATA
CLK
EN
4
5
3
8
6
7
9
7.5k
0.01 µF
1N4001
1N4001
1N4001
(RIGHT DISPLAY)
NSM4000A
DATA
CLK
EN
4
5
3
8
6
7
9
7.5k
0.01 µF
F
G
H
M
D
E
P
Q
4_BY_4
KEYPAD
GRAYHILL
#87BB3-201
10K
10K
10K

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FIGURE 14. Microprocessor Control and Display Section

LO: The LO key will display the local oscillator frequency that corresponds to the present tuned frequency. The LO frequency displays for a few seconds and then the tuned frequency returns.

TEST MODE: This key allows the user to choose between mode 0, 1, 2 or 3. Each time the key is pressed the test mode will rotate and display the new mode for a few seconds before the tuned frequency reappears. A keypress will not be recognized until the tuned frequency reappears. The system powers up in test mode 0.

REF: This key allows the user to change the reference frequency used by the DS8911. Each keypress rotates the reference frequency from 100 kHz to 10 kHz, 10 kHz to 12.5 kHz, 12.5 kHz to 25 kHz or 25 kHz to 100 kHz depending where it started. The tuned frequency will be recalculated using the new reference frequency and displayed. If the tuned frequency is too high or low, a multiple or a non-integer of the new reference frequency, the program will automatically rotate to the next legal reference frequency, display it for a few seconds, and then return to displaying the tuned frequency. The system powers up in the 100 kHz mode.

BIT 22, 23, 24: Each of these keys changes the high or low state of bit 22, 23 and 24 in the serial data stream to the DS8911. The bits power up low and may be changed high independently by pressing the appropriate key. The display will then show the status of all three bits in the right three digit spots.

Example: Bit 23 high, bit 22 and 24 low. = |0|1|0|

ALIGNMENT

1. In FM mode tune to 98.5 MHz. Adjust L3 while monitoring DC voltage on OP AMP, pin 26 of IC1. Adjust L3 for a reading of 3.4 Vdc.
2. Switch to AM mode. Set generator for 810 kHz, 30% modulation, 400 Hz. RF level: 100 μV. Use 40 pF dummy antenna.
3. Adjust T2, T3, T4, T5, T6 for maximum sensitivity as measured at speaker output using suitable AC voltmeter.

Note: As signal strength increases with alignment, appropriately reduce the RF output of signal generator.

4. Switch to FM mode and tune to 98.5 MHz. Set FM generator to 98.5 MHz. Set RF output to 100 μV, modulation 400 Hz, deviation 22.5 kHz. Use 50Ω termination on antenna input.
5. Adjust T9 for maximum recovered audio and mininum distortion.
6. Adjust T7 and T8 for maximum sensitivity. Reduce RF level of generator as needed.
7. Tune to stereo FM station. Adjust R70 for D5 "On." 100 μV, modulation 400 Hz, deviation 22.5 kHz. Use 50Ω termination on antenna input.
5. Adjust T9 for maximum recovered audio and minimum distortion.
6. Adjust T7 and T8 for maximum sensitivity. Reduce RF level of generator as needed.
7. Tune to stereo FM station. Adjust R70 for D5 "On".

TYPICAL SPECIFICATIONS

AM SIGNAL-TO-NOISE

RF Level	S/N
12 μV	14 dB
45 μV	27 dB
1000 μV	49 dB

AM RADIO SENSITIVITY

540–1000 kHz	6.7 μV
1000–1600 kHz	8.9 μV

AM RADIO SELECTIVITY

Input level = 2 × Radio AM selectivity level

6 dB audio level Bandwidth	8.0 kHz

Input level = 200 × Radio AM selectivity level

6 dB audio level Bandwidth	24 kHz

AM STRONG SIGNAL DISTORTION

RF Level	% Distortion
80 mV	1
800 mV	1
1500 mV	3

AGC figure of merit = 54.9

AM SPURIOUS RESPONSE

Freq. kHz	dB
700	−15
850	−9.5
913	−12
1051	−8
1074	−11
1198	−16

AM CROSS MODULATION

Ref. Gen. Level = 200 μV (Radio tuned to Ref. Gen.)

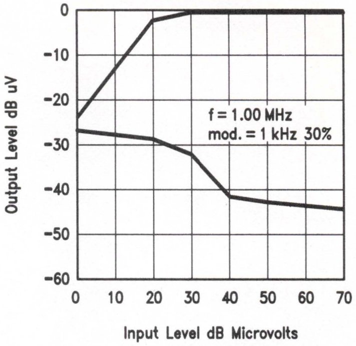
Frequency = 1.01 MHz

Gen #2 Level = 10,000 μV

Gen #2 signal appears 30 dB down*

Frequency = 1.05 MHz

AM Signal to Noise



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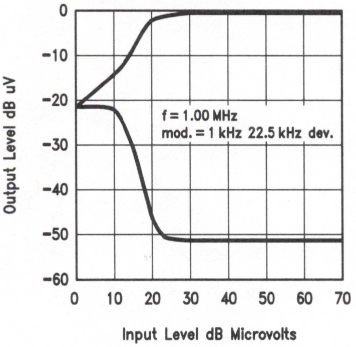
FM Signal to Noise



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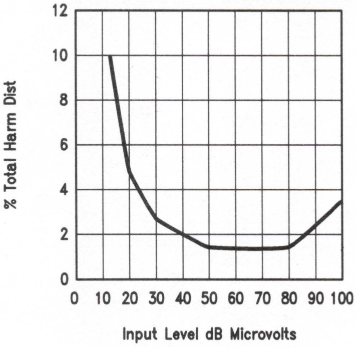
AM Percent Harmonic Distortion



TL/F/9449–17

Section 9
Hi-Rel Interface

Section 9 Contents

Hi-Rel Interface—Introduction 9-3
National's A+ Program 9-13
Hi-Rel Interface—Selection Guide 9-15

National Semiconductor

Military/Aerospace Programs from National Semiconductor

This section is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

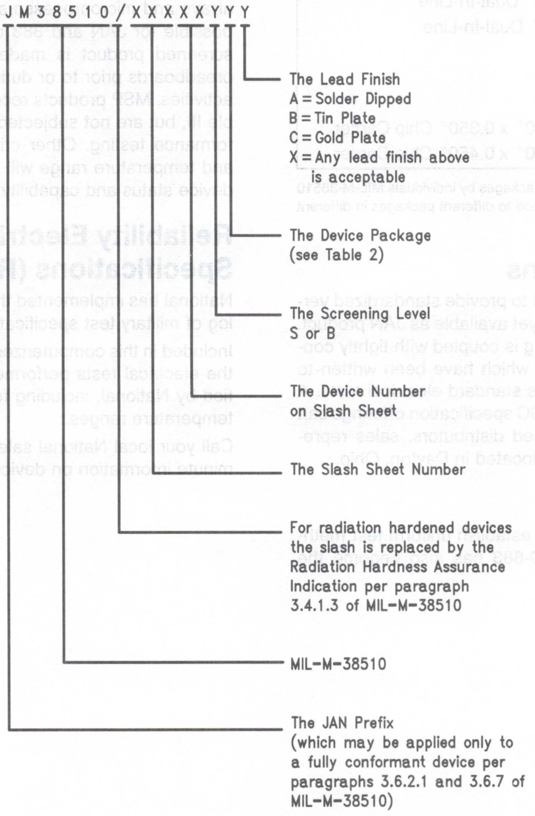
There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table 3.

Tables 1 and 2 explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

TABLE I. The MIL-M-38510 Part Marking


JM38510/XXXXXYYY
The Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable
The Device Package (see Table 2)
The Screening Level S or B
The Device Number on Slash Sheet
The Slash Sheet Number
For radiation hardened devices the slash is replaced by the Radiation Hardness Assurance Indication per paragraph 3.4.1.3 of MIL-M-38510
MIL-M-38510
The JAN Prefix (which may be applied only to a fully conformant device per paragraphs 3.6.2.1 and 3.6.7 of MIL-M-38510)
TL/XX/0113-1

MIL-M-38510 (Continued)

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin ¼″ x ¼″ (Metal) Flat Pack
B	14-Pin 3/15″ x ¼″ Flat Pack
C	14-Pin ¼″ x ¾″ Dual-In-Line
D	14-Pin ¼″ x ⅜″ (Ceramic) Flat Pack
E	16-Pin ¼″ x ⅞″ Dual-In-Line
F	16-Pin ¼″ x ⅜″ (Metal or Ceramic) Flat Pack
G	8-Pin TO-99 Can or Header
H	10-Pin ¼″ x ¼″ (Metal) Flat Pack
I	10-Pin TO-100 Can or Header
J	24-Pin ½″ x 1¼″ Dual-In-Line
K	24-Pin ⅜″ x ⅝″ Flat Pack
L	24-Pin ¼″ x 1¼″ Dual-In-Line
M	12-Pin TO-101 Can or Header
N	(Note 1)
P	8-Pin ¼″ x ⅜″ Dual-In-Line
Q	40-Pin 3/16″ x 2 1/16″ Dual-In-Line
R	20-Pin ¼″ x 1 1/16″ Dual-In-Line
S	20-Pin ¼″ x ½″ Flat Pack
T	(Note 1)
U	(Note 1)
V	18-Pin ⅜″ x 15/16″ Dual-In-Line
W	22-Pin ⅜″ x 1⅛″ Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-Terminal 0.350″ x 0.350″ Chip Carrier
3	28-Terminal 0.450″ x 0.450″ Chip Carrier

Note 1: These letters are assigned to packages by individuals MIL-M-38510 detail specifications and may be assigned to different packages in different specifications.

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales representatives, of DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883, but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product, but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

Reliability Electrical Test Specifications (RETS™)

National has implemented the first realtime, electronic catalog of military test specifications called RETS.

Included in this computerized directory is a detailed listing of the electrical tests performed on all military devices qualified by National, including forcing functions, test limits and temperature ranges.

Call your local National sales office for essential up-to-the-minute information on device testing.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		
2. Nondestructive Bond Pull (Note 14)	2023	100%		
3. Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake (Note 16)	1008, Condition C, Min. 24 hrs. Min.	100%	1008, Condition C, Min., 24 hrs. Min.	100%
5. Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E Min. Y_1 Orientation Only	100%	2001, Condition E, Min. Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9. Serialization	(Note 5)	100%		
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		
14. Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15. PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test (Note 15)				
a) Static Tests				
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I 5005)		100%		100%
b) Dynamic Tests or Functional Tests	Per Applicable Device Specification		Per Applicable Device Specification	
1) 25°C (Subgroups 4 or 7)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005)		100%		100%
c) Switching Tests 25°C (Subgroups 9 Table I, 5005)		100%		100%
17. Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18. Radiographic (Note 10)	2012 Two Views	100%		
19. Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20. External Visual (Note 12)	2009	100%		100%

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE III. 100% Screening Requirements (Continued)

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

TABLE IV. Group A Electrical Tests

Subgroup (Notes 1, 2)	LTPD
Subgroup 1 Static Tests at 25°C	2
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	3
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	5
Subgroup 4 Dynamic Tests at 25°C	2
Subgroup 5 Dynamic Tests at Maximum Rated Operating Temperature	3
Subgroup 6 Dynamic Tests at Minimum Rated Operating Temperature	5
Subgroup 7 Functional Tests at 25°C	2
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temperatures	5
Subgroup 9 Switching Tests at 25°C	2
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	3
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	5

Note 1: The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.

Note 2: A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.

Note 3: Group A testing by subgroup or within subgroups may be performed in any sequence, unless otherwise specified.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE V. Group B (Class B)

Test (Note 1)	Method	Condition	LTPD
Subgroup 1			
Physical Dimensions (Note 2)	2016		2 Devices (No Failures)
Subgroup 2			
Resistance to Solvents	2015		4 Devices (No Failures)
Subgroup 3			
Solderability (Note 3)	2003 or 2002	Soldering Temperature of 245 ±5°C	10
Subgroup 4			
Internal Visual and Mechanical (Note 4)	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document	1 Device (No Failures)
Subgroup 5			
Bond Strength (Note 5)			
1) Thermocompression	2011	1) Condition C or D	15
2) Ultrasonic of Wedge		2) Condition C or D	
3) Flip-Chip		3) Condition F	
4) Beam Lead		4) Condition H	
Subgroup 6			
Internal Water-Vapor Content (Note 6)	1018	1,000 ppm Maximum Water Content at 100°C	3 Devices (0 Failures) (Note 7) or 5 Devices (1 Failure)
Subgroup 7			
Seal (Note 8)			
1) Fine	1014	As Applicable	5
2) Gross			
Subgroup 8 (Note 9)			
Electrical Parameters	2015	Group A, Subgroup 1	15 (0)
Electrostatic Discharge Sensitivity			
Electrical Parameters		Group A, Subgroup 1	

Note 1: Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required, except for devices submitted to subgroup 7.

Note 2: Not required for qualification or quality conformance inspections where Group D inspection is being performed on samples from the same inspection lot.

Note 3: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot-solder dipped or have undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

Note 4: Test samples for internal visual and mechanical shall be selected at any point following the seal operation.

Note 5: Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (precap) inspection provided all other specification requirements are satisfied. Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 10 devices, and for conditions F or H is the number of dice (not bonds) (see Method 2011).

Note 6: This test is required only if the package contains a desiccant.

Note 7: Test 3 devices, if 1 fails, test 2 additional devices with no failure.

Note 8: This test is not required if either the 100% screen or sample test is performed between steps 14 and 18 and 100% screening of Table 3 of this section.

Note 9: Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE VI. Group B (Class S)

Test (Note 1)	Method	Condition	Quality/(Accept No.) or LTPD
Subgroup 1			
a) Physical Dimensions (Note 2)	2016		2 (0)
b) Internal Water-Vapor (Notes 2, 3)	1018	5,000 ppm Maximum Water Content at 100°C	3 (0) or 5 (1) (Note 4)
Subgroup 2 (Note 5)			
a) Resistance to Solvents	2015		4 (0)
b) Internal Visual and Mechanical	2013 & 2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document	2 (0)
c) Bond Strength (Note 6)	2011		LTPD = 10
1) Thermocompression		1) Condition C or D	
2) Ultrasonic		2) Condition C or D	
3) Flip-Chip		3) Condition F	
4) Beam Lead		4) Condition H	
d) Die Shear Test	2019	Per Method 2019 for the Applicable Die Size	3 (0)
Subgroup 3			
Solderability (Note 7)	2003 or 2022	Soldering Temperature or 245 ± 5°C	LTPD = 15
Subgroup 4			
Lead Integrity (Note 5)	2004	Condition B_2, Lead Fatigue	2 (0)
Seal	1014	As Applicable	
1) Fine			
2) Gross			
Lid Torque (Note 3)		As Applicable	
Subgroup 5 (Notes 8, 9)			
a) Electrical Parameters (Note 11)		Group A, Subgroups 1, 2, 3: Read and Record Group A, Subgroups 4-11: Attributes	LTPD = 5
b) Steady State Life	1005	Condition C, D or E: 1000 hours	
c) Electrical Parameters		Groups A, Subgroups 1, 2, 3: Read and Record Group A, Subgroup 4-11: Attributes	
Subgroup 6 (Note 5)			
a) Electrical Parameters (Note 11)		Group A, Subgroups 1, 2, 3: Read and Record	LTPD = 5
b) Temperature Cycling	1010	Condition C, 100 Cycles/min.	
c) Constant Acceleration	2001	Test Condition E: Y_1 Orientation Only	
d) Seal	1014		
1) Fine			
2) Gross			
e) Electrical Parameters		Group A, Subgroups 1, 2, 3: Read and Record	
Subgroup 7 (Note 12)			
a) Electrical Parameters		Group A, Subgroup 1	15 (0)
b) Electrostatic Discharge Sensitivity	3015		
b) Electrical Parameters		Group A, Subgroup 1	

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE VI. Group B (Class S) (Continued)

Note 1: Electrical reject devices from the same inspection may be used for all subgroups where electrical end-point measurements are not required.

Note 2: Not required for qualification or quality conformance inspections where Group D inspection is being performed on samples from the same inspection lot.

Note 3: This test is required only if it is a glass-frit sealed package.

Note 4: Test 3 devices; if 1 fails, test 2 additional devices with no failures.

Note 5: All samples for subgroup B2 must have been through the complete sequence of subgroup B6 tests.

Note 6: Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum of 4 devices and for conditions F and H is the number of dice (not bonds).

Note 7: All devices must be in the same lead finish that will be on the shipped product and shall have been through the temperature/time exposure of burn-in except for devices that have been hot-solder dipped or undergone tin fusing after burn-in. The LTPD applies to the number of leads inspected, except in no case shall less than 3 devices be used to provide the number of leads required.

Note 8: The alternate removal-of-bias provisions of Method 1005 shall not apply for test temperatures above 125°C.

Note 9: The same temperature must be employed for operating life that was used for the 100% burn-in.

Note 10: For leadless chip carriers, condition D will apply.

Note 11: Read and record data Group A of quality conformance is acceptable.

Note 12: Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum.

TABLE VII. Group C (Die-Related Tests for Class B and C Only)

Test	Method	Condition	LTPD
Subgroup 1			
Steady State Life Test	1005	Test Condition to be Specified (1,000 hours at 125°C)	5
End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 2			
Temperature Cycling	1010	Condition C	15
Constant Acceleration	2001	Condition E min, Y_1 Orientation Only (Note 1)	
Seal	1014	As Applicable	
a) Fine			
b) Gross			
Visual Examination		Per Visual Criteria of Method 1010 or 1011 as	
End-Point Electrical Parameters		Specified in the Applicable Device Specification	

Note 1: See paragraph 3 of Method 5005 for the procedure for large cavity package.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE VIII. Group D (Package-Related Tests for Classes)

Test	Method	Condition	LTPD
Subgroup 1 (Note 1)			
a) Physical Dimensions	2016		15
Subgroup 2 (Note 1, 4)			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue) (Note 10)	15
Seal	1014	As Applicable	
a) Fine			
b) Gross			
Subgroup 3 (Note 3)			
Thermal Shock	1011	Test Condition B Minimum, 15 Cycles Minimum	15
Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
Moisture Resistance (Note 4)	1004		
Seal	1014	As Applicable	
a) Fine			
b) Gross			
Visual Examination		Per Visual Criteria of Method 1004 or 1010	
End-Point Electrical Parameter (Note 4)		As Specified in the Applicable Device Specification	
Subgroup 4 (Note 3)			
Mechanical Shock	2002	Test Condition B Minimum	15
Vibration Variable Frequency	2007	Test Condition A Minimum	
Constant Acceleration	2001	Test Condition E Minimum	
		Y_1 Orientation Only (Note 6)	
Seal	1014	As Applicable	
a) Fine			
b) Gross			
Visual Examination		Per Visual Criteria of Method 1010 or 1011	
End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 5 (Note 1)			
Salt Atmosphere	1009	Test Condition A Minimum	15
Seal	1014	As Applicable	
a) Fine			
b) Gross			
Visual Examination		Per Visual Criteria of Method 1009	
Subgroup 6 (Note 1)			
Internal Water-Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	3 Devices (0 Failures) or 5 Devices (1 Failure)(Note 5)
Subgroup 7 (Note 1)			
Adhesion of Lead Finish (Notes 7, 8)	2025		15
Subgroup 8 (Note 1)			
Lid Torque (Note 2)	2024		5 (0)

Note 1: Electrical reject devices from that same inspection lot may be used for samples.

Note 2: Lid torque test shall apply only to packages which use a glass-frit seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

Note 3: Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in Subgroup 4 "Mechanical".

Note 4: At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

Note 5: Test 3 devices; if 1 fails, test 2 additional devices with no failures.

Note 6: See paragraph 3 of Method 5005 for the procedure for large cavity packages.

Note 7: Does not apply to leadless chip carriers.

Note 8: The LTPD applies to the number of leads to be tested.

Note 9: The lead bend stress initial conditioning is not required for leadless chip carriers.

Note 10: For leadless chip carriers only, condition D shall apply.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE IX. Group E (Radiation Hardness Assurance Tests)

Test (Note 1)	Method	Condition	Quantity (Accept Number = 0)	
			Class S	Class B
Subgroup 1 (Note 3)				
Neutron Irradiation	1017	25°C		
a) Qualification			11 per Wafer Lot	5 from each of 3 Wafer Lots
b) Quality Conformance			11 per Wafer Lot	11 per Wafer Lot
End-Point Electrical Parameters		Per Applicable Detail Specification		
Subgroup 2				
Steady-state Total Dose Irradiation	1019	25°C, Maximum Supply Voltage		
a) Qualification			(Note 2)	5 from each of 3 Wafer Lots
b) Quality Conformance			(Note 2)	11 per Wafer Lot
End-Point Electrical Parameters		Per Applicable Detail Specification		

Note 1: Parts used for one subgroup test may not be used for the other subgroup but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

Note 2: 4 per wafer for devices type S less than or equal to 4000 equivalent transistors per chip, 2 per wafer for larger dice. Samples will be selected at radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

Note 3: Subgroup 1 is not required for MOS devices.

Reliability Electrical Test Specifications (RETS™) (Continued)

TABLE X. Wafer Lot Acceptance Tests

Test	Conditions (Note 1)	Limits (Note 2)	Sampling Plan
1. Wafer Thickness (not required when the finished wafer design thickness is greater than 10 mils)	MIL-STD-977, Method 1580. Measurement shall be performed after final lap or polish. All readings shall be recorded.	Maximum deviation of ± 2 mil for approved design nominal 6 mil minimum.	Two wafers per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
2. Metallization thickness	MIL-STD-977 Method 5500. All readings shall be recorded.	a) Conductor: 8 kÅ minimum for single level metal and for the top level of multi-level metal: 6 kÅ minimum for lower levels, with a maximum deviation of ± 20% from the approved design nominal. b) Barrier: Maximum deviation of ± 30% from the approved design nominal.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
3. Thermal stability (applicable to: all linear; all MOS; all bipolar digital operating at 10V or more)	MIL-STD-977, Method 2500. Record V_{FB} or V_T. (Note 3)	a) ΔV_{FB} or $\Delta V_T \leq 0.75V$ for bipolar digital devices operating at $\geq$ 10V and all bipolar linear devices not containing MOS transistors. The monitor shall have an oxide and shall be metallized with the lot. b) ΔV_{FB} or $\Delta V_T \leq 1.0V$ for bipolar linear devices that operate above 5V and contain MOS transistors and digital devices that operate above 10V and contain MOS structures. c) ΔV_{FB} or $\Delta V_T \leq 0.4V$ for MOS devices.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer. Separate monitors may be used but must be oxidized and metallized with the lot. A monitor consisting of a gate oxide metallized with the lot shall be used.
4. SEM (Note 4)	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018. Lot acceptance basis.
5. Glassivation Thickness	MIL-STD-977, Method 5500. All readings shall be recorded.	6 kÅ minimum for SiO_2 and 2 kÅ minimum Si_3N_4 with maximum deviation of ±20% from approved design nominal.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
6. Gold backing thickness (when applicable)	MIL-STD-977, Method 5500. All readings shall be recorded.	Per approved design nominal thickness and tolerance.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

Note 1: Approved equivalent test methods may be used in lieu of the reference MIL-STD-977 methods.

Note 2: Approved design nominal values or tolerances shall be submitted for line certification per DESC-EQM-42.

Note 3: All reading shall be normalized to oxide thickness of 1000Å.

Note 4: When wafer lots fail to pass the SEM requirements of Method 2018, compliance with the current density requirement shall not be used to waiver the SEM requirement.

National Semiconductor

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who need better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction; the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

National's A+ Program (Continued)

Five Temperature Cycles (0°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

High Temperature (100°C) Functional Electrical Test

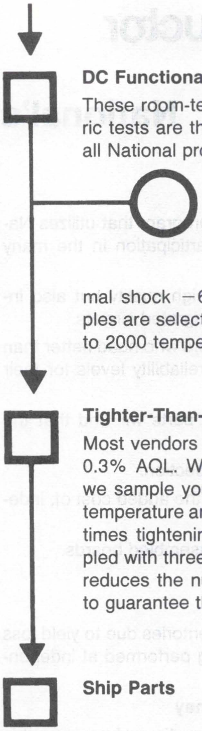
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-In Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96 eV activation energy (i.e., 23 hours at +155°C). All burn-in done under steady-state conditions unless otherwise specified.



DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National Semiconductor

Interface Hi-Rel Selection Guide

NSID	—MIL	/883	DESC SMD	JAN
DP7304B	X			
DP7311		X		
DP8216		X		
DP8228	X			
DP8238	X			
DS0026		X		
DS0056		X	X	
DS16F95		✓		
DS1603		X		
DS16179		X		
DS1631		X		
DS1632		X		
DS1634		X		
DS1649		X		
DS1651	X			
DS1652	X			
DS1674		X		
DS1687		X		
DS1691A		X		
DS26F31		✓		
DS26LS31		X	X	
DS26F32		✓		
DS26LS32		X		
DS26LS33		X		
DS35F86		✓		
DS35F87		✓		
DS55107A		X		X
DS55110A		X	X	
DS55113		X		
DS55122		X		
DS55451		X		
DS55452	X			
DS55453	X			
DS55461		X		
DS55462		X		
DS55463	X			
DS55464	X			
DS55494		X		
DS7640		X		
DS78C120		X		
DS78C20		X		
DS78LS120		X		
DS78L12	X			
DS7800		X		
DS7820A		X	X	
DS7820		X		
DS7830		X		
DS7831		X	X	
DS7832		X	X	
DS7833		X		
DS7834		X		
DS7835		X		
DS7836		X		
DS7837		X		
DS7838	X			
DS8T28	X			
DS96F172		✓		
DS96F173		✓		
DS96F174		✓		
DS96F175		✓		
DS96F177		✓		
DS96F178		✓		
DS9614		X		X
DS9615		X		X
DS9622		X	X	
DS9627		X		
DS9636A		X	X	
DS9637A		X	X	
DS9638		X	X	
DS9639A		X		
DS9667A		X		
MM5452	X			
μA55107A		X		X
μA55110A		X	X	
μA9614		X		X
μA9615		X		X
μA9622		X	X	
μA9627		X		
μA9636A		X	X	
μA9637A		X	X	
μA9638		X	X	
μA9639A		X		
μA9667A		X		

X = Available Now

✓ = Future Product

Section 10

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Data Bookshelf
Sales and Distribution Offices

National Semiconductor

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AN-512	DS8911 AM/FM/TV Sound Up-Conversion Frequency Synthesizer	8-56
AN-514	Timing Analysis of Synchronous and Asynchronous Busses	2-81

Technical Terms and Definitions

CURRENT

High-Level Input Current, I_{IH}

The current into* an input when a high-level voltage is applied to that input.

Input Current at Maximum Input Voltage, I_I

The current into* an input when maximum specified input voltage is applied.

Low-Level Input Current, I_{IL}

The current into* an input when a low-level voltage is applied to that input.

Low-Level Input Current HiZ, I_{ILZ}

The current into* an input when a low-level voltage is applied to the input with the device in the TRI-STATE condition.

High-Level Output Current, I_{OH}

The current into* an output with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Low-Level Output Current, I_{OL}

The current into* an output with input conditions applied that, according to the product specification, will establish a logic low level at the output.

Off-State Output Current, I_O (I_{CEX})

The current flowing into* an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits at a specified voltage usually greater then the V_{CC} supply.

Output Current of a TRI-STATE Device, I_{OZ}

The current* a TRI-STATE output having input conditions applied that, according to the product specification, will establish the high-impedance state at the output.

Short-Circuit Output Current, I_{OS}

The current into* an output when that output is short-circuited to ground or any other specified potential, with input conditions applied to establish the output logic level farthest from ground potential or any other specified potential.

Supply Current, I_{CCH}

The current into* the V_{CC} supply terminal of an integrated circuit when the outputs are in a logic high state.

Supply Current, I_{CCL}

The current into* the V_{CC} supply terminal of an integrated circuit when the outputs are in a logic low state.

VOLTAGE

High-Level Input Voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

*Current out of a terminal is given as a negative value.

Low-Level Input Voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Positive-Going Threshold Voltage, V_{TH}

The voltage level at a transition-operated input that, causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}.

Negative-Going Threshold Voltage, V_{TL}

The voltage level at a transition-operated input that, causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}.

Hysteresis, V_{HYS}

The absolute difference in voltage value between the positive going threshold and negative going threshold.

Input Clamp Voltage, V_{IK}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

High-Level Output Voltage, V_{OH}

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Low-Level Output Voltage, V_{OL}

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the output.

Off-State Output Voltage, $V_{O(off)}$

The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for the outputs not having internal pull-up elements.

On-State Output Voltage, $V_{O(on)}$

The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on-state.

Output Clamp Voltage, V_{OK}

An output voltage in a region of low differential resistance that serves to limit the voltage swing.

PROPAGATION TIME

Propagation Delay Time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one logic level (high or low) to the other logic level.

Technical Terms and Definitions (Continued)

Propagation Delay Time, Low-to-High-Level Output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the logic low level to the logic high level.

Propagation Delay Time, High-to-Low-Level Output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the logic high level to the logic low level.

Transition Time LOW to HIGH, t_{TLH}

The time between two specified reference points on a waveform, normally specified between the 10% and 90% points, that is changing from LOW to HIGH.

Transition Time HIGH to LOW, t_{THL}

The time between two specified reference points on a waveform, normally specified between the 90% and 10% points, that is changing from HIGH to LOW.

TRI-STATE DELAYS

Output Enable Time, t_{PZL}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from a high-impedance (off) state to the logic low level.

Output Enable Time, t_{PZH}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from a high-impedance (off) state to the logic high level.

Output Disable Time, t_{PLZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from the logic low level to a high-impedance (off) state.

Output Disable Time, t_{PHZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from the logic high level to a high-impedance (off) state.

CLOCK FREQUENCY

Maximum Clock Frequency, f_{MAX}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

PULSE WIDTH

Pulse Width, t_W

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

SETUP AND HOLD TIME

Setup Time, t_{SU}

The time interval between the application of a signal that is maintained at a specified input terminal prior to a consecutive active transition at another specified input terminal.

Note 1: The setup time is defined as the time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which proper operation of the logic element is guaranteed.

Note 2: The setup time may have a negative value in which case the minimum limit defines the longest interval of time between the active transition and the application of the other signal for which proper operation of the logic element is guaranteed.

Hold Time, t_h

The interval during which a signal is maintained at a specified input terminal after an active transition occurs at another specified input terminal.

Note 1: The hold time is defined as the time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval of time for which proper operation of the logic element is guaranteed.

Note 2: The hold time may have a negative value in which case the minimum limit defines the longest interval of time between the release of data and the active transition on the specified input for which proper operation of the logic element is guaranteed.

TRUTH TABLE EXPLANATIONS

Symbols generally associated with Functional Truth Tables.

H = Logic high level (steady-state)
L = Logic low level (steady-state)
_/¯ = Transition from a logic low to high level
= Transition from a logic high to low level
X = irrelevant (any input, including transitions)
Z = off state (high-impedance) of a TRI-STATE output
a..h = the level of steady-state inputs at inputs A through H respectively
Q_O = level of Q before the indicated steady-state input conditions were established
$\overline{Q}_O$ = complement of Q_O or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by _/¯ or

NOTE: If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the event sequence. The output logic state persists so long as the input configuration is maintained.

If, in the input columns, a row contains (H, L, and/or X) together with _/¯ and/or this means the output is valid whenever the input configuration is achieved. However, the transition(s) must occur following the application of the steady-state levels. If the output is shown as a level (H, L, Q_O or $\overline{Q}_O$), it will be maintained so long as the steady-state input levels and the levels that terminate the defined transitions are maintained. Unless otherwise specified, input transitions in the opposite direction to those shown have no effect on the steady state output.

National Semiconductor

Interface Cross Reference Guide

AMD to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
AMD		
AM26LS30DC	DS3691J	
AM26LS30PC	DS3691N	
AM26LS31DC	DS26LS31CN	
AM26LS31PC	DS26LS31CN	
AM26LS32DC	DS26LS32ACJ	DS26LS32CJ
AM26LS32PC	DS26LS32ACN	DS26LS32CN
AM26LS33DC	DS26LS33ACJ	DS26LS33CJ
AM26LS33PC	DS26LS33ACN	DS26LS33CN
AM26S10DC	DS26S10J	
AM26S10PC	DS26S10N	
AM26S11DC	DS26S11J	
AM26S11PC	DS26S11N	
AM26S12DC		DS8838J
AM26S12PC		DS8838N
AM2965DC		DP84240J
AM2965PC		DP84240N
AM2966DC		DP84244J
AM2966PC		DP84244N
N8T26AB	DS8T26AN	
N8T26AF	DS8T26AJ	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
D8212	DP8212J	
P8212	DP8212N	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
AM8224PC	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
AM8228PC	DP8228N	
D8228	DP8228J	
AM8238PC	DP8238N	
D8238	DP8238J	
DP8303J	DP8303AJ	
DP8303N	DP8303AN	
DP8304BJ	DP8304BJ	
DP8304BN	DP8304BN	
DP8307J	DP8307AJ	
DP8307N	DP8307AN	
DP8308J	DP8308J	
DP8308N	DP8308N	
DS8838J	DS8838J	
DS8838N	DS8838N	

The manufacturer's most current data sheets take precedence over this guide.

Intel to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
INTEL		
D3245	DS3245J	
D8212	DP8212J	
P8212	DP8212J	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
D8224	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
D8228	DP8228J	
D8228	DP8228N	
D8238	DP8238J	
P8238	DP8238N	
D8286	DP8304BJ	
P8286	DP8304BN	
D8287	DP8303AJ	
P8287	DP8303AN	

The manufacturer's most current data sheets take precedence over this guide.

Motorola to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
MOTOROLA		
MC12015P	DS8615N	
MC12016P	DS8616N	
MC12017P	DS8617N	
MC12071P	DS8621N	
MC1411P		DS2001N
MC1411P		µA9665PC
MC1412P		DS2002N
MC1412P		µA9666PC
MC1413P		DS2003N
MC1413P		µA9667PC
MC1416P		DS2004N
MC1416P		µA9668PC
MC1472P1		DS3632N
MC1472U		DS3632J-8
MC1488L	DS1488J	
MC1488P	DS1488N	
MC1489AL	DS1489AJ	
MC1489AP	DS1489AN	
MC1489L	DS1489J	
MC1489P	DS1489N	
AM26LS31DC	DS26LS31CJ	
AM26LS31PC	DS26LS31CN	
MC26S10L	DS26S10J	
MC26S10P	DS26S10N	
MC3430L	DS3651J	
MC3430P	DS3651N	
MC3431L		DS3651J
MC3431P		DS3651N
MC3432L	DS3653J	
MC3432P	DS3653N	
MC3433L		DS3653J
MC3433P		DS3653N
MC3437L	DS8837J	
MC3437P	DS8837N	
MC3438L	DS8838J	
MC3438P	DS8838N	
MC3450L		DS3650J
MC3450P		DS3650N
MC3452P	DS3652N	

The manufacturer's most current data sheets take precedence over this guide.

Device Designation	National's Direct Replacement	National's Closest Replacement
MOTOROLA (Continued)		
MC3486L	DS3486J	
MC3486P	DS3486N	
MC3487L	DS3487J	
MC3487P	DS3487N	
MC3488AP		DS9636AN
MC3488AP		µA9636AT
MC3491P		DS8889N
MC6880AL	DS8T26AJ	
MC6880AP	DS8T26AN	
MC6889L	DS8T28J	
MC6889P	DS8T28N	
MC75107L	DS75107J	
MC75107P	DS75107N	
MC75108L	DS75108J	
MC75108P	DS75108N	
MC75125L	DS75125J	
MC75125P	DS75125N	
MC75127L	DS75127J	
MC75127P	DS75127N	
MC75128L	DS75128J	
MC75128P	DS75128N	
MC75129L	DS75129J	
MC75129P	DS75129N	
MC75325L	DS75325J	
MC75491P	DS75491N	
MC75492P	DS75492N	
MC8T13L	DS75121J	
MC8T13P	DS75121N	
MC8T23L	DS75123J	
MC8T23P	DS75123N	
MC8T24L	DS75124J	
MC8T24P	DS75124N	
MC8T26AL	DS8T26AJ	DS8834J
MC8T26AP	DS8T26AN	DS8834N
MC8T28L	DS8T28J	
MC8T28P	DS8T28N	
DS8641N	DS8641N	
DS8641J	DS8641N	

The manufacturer's most current data sheets take precedence over this guide.

Signetics to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
SIGNETICS		
MC1488F	DS1488J	
MC1488N	DS1488N	
MC1489AN	DS1489AN	
MC1489AF	DS1489AJ	
MC1489F	DS1489J	
MC1489N	DS1489N	
NE582F		DS75494J
NE582N		DS75494N
75S107F		DS75107J
75S107N		DS75107N
75S108F		DS75108J
75S108N		DS75108N
75S208F		DS75208J
75S208N		DS75208N
NE5601N		DS2001N
NE5601N		μA9665PC
NE5602N		DS2002N
NE5602N		μA9666PC
NE5603N		DS2003N
NE5603N		μA9667PC
NE5604N		DS2004N
NE5604N		μA9668PC
N8T13F	DS75121J	
N8T13N	DS75121N	
N8T15F		DS75150J-8
N8T15N		DS75150N
N8T23F	DS75123J	
N8T23N	DS75123N	
N8T24F	DS75124J	
N8T24N	DS75124N	
N8T26AF	DS8T26AJ	
N8T26AN	DS8T26AN	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
N8T34F	DS8834J	
N8T34N	DS8834N	
N8T37F	DS8837J	
N8T37N	DS8837N	
N8T38F	DS8838J	
N8T38N	DS8838N	
N8T380F	DS8836J	DS8640J
N8T380N	DS8836N	DS8640N
DS8820AF	DS8820AJ	
DS8820AN	DS8820AN	
DS8820F	DS8820J	
DS8820N	DS8820N	
DS8830F	DS8830J	
DS8830N	DS8830N	
DS8880F	DS8880J	
DS8880N	DS8880N	
μLN2001N	μA9665PC	
μLN2003F	μA9667DC	
μLN2003N	μA9667PC	
μLN2004F	μA9668DC	
μLN2004N	μA9668PC	

The manufacturer's most current data sheets take precedence over this guide.

Sprague to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
SPRAGUE		
UDN3611H		DS3631J-8
UDN3611M		DS3631N
UDN3612H		DS3632J-8
UDN3612M		DS3632N
UDN3613H		DS3633J-8
UDN3613M		DS3633N
UDN3614M		DS3634N
ULN2001		DS2001
ULN2001		μA9665
ULN2002		DS2002
ULN2002		μA9666
ULN2003		DS2003
ULN2003		μA9667
ULN2004		DS2004
ULN2004		μA9668

The manufacturer's most current data sheets take precedence over this guide.

Texas Instruments to National's Interface

Device Designation	National's Direct Replacement	National's Closest Replacement
TEXAS INSTRUMENTS		
MC1488J	DS1488J	
MC1488N	DS1488N	
MC1489AJ	DS1489AJ	
MC1489AN	DS1489AN	
MC1489J	DS1489J	
MC1489N	DS1489N	
AM26LS31CJ	DS26LS31CJ	
AM26LS31CN	DS26LS31CN	
AM26LS32ACJ	DS26LS32ACJ	DS26LS32CJ
AM26LS32ACN	DS26LS32ACN	DS26LS32CN
AM26LS33AJ	DS26LS33ACJ	DS26LS33CJ
AM26LS33AN	DS26LS33ACN	DS26LS33CN
AM26S10CJ	DS26S10J	
AM26S10CN	DS26S10N	
AM26S11CJ	DS26S11J	
AM26S11CN	DS26S11N	
MC3486J	DS3486J	
MC3486N	DS3486N	
MC3487J	DS3487J	
MC3487N	DS3487N	
SN74LS424J	DS8224J	
SN74LS424N	DS8224N	
SN74S412J	DP8212J	
SN74S412N	DP8212N	
SN74S428N	DP8228N	
SN74S436N	DP36149N	
SN74S437N	DP36179N	
SN74S438N	DP8238N	
SN75107AJ		DS75107J
SN75107AN		DS75107N
SN75107BJ	DS75107J	
SN75107BN	DS75107N	
SN75108AJ		DS75108J
SN75108AN		DS75108N
SN75108BJ	DS75108J	
SN75108BN	DS75108N	
SN75110AD		DS75110AJ
SN75110AD		µA75110ADC
SN75110AN		DS75110AN
SN75110AN		µA75110APC
SN75113J	DS75113J	
SN75113N	DS75113N	
SN75114J	DS75114J	
SN75114N	DS75114N	
SN75115J	DS75115J	
SN75115N	DS75115N	
SN75121J	DS75121J	
SN75121N	DS75121N	
SN75123J	DS75123J	

The manufacturer's most current data sheets take precedence over this guide.

Device Designation	National's Direct Replacement	National's Closest Replacement
TEXAS INSTRUMENTS (Continued)		
SN75123N	DS75123N	
SN75124J	DS75124J	
SN75124N	DS75124N	
SN75125J	DS75125J	
SN75125N	DS75125N	
SN75127J	DS75127J	
SN75127N	DS75127N	
SN75128J	DS75128J	
SN75128N	DS75128N	
SN75129J	DS75129J	
SN75129N	DS75129N	
SN75150J	DS75150J-8	
SN75150N	DS75150N	
SN75154J	DS75154J	
SN75154N	DS75154N	
SN75160N	DS75160AN	
SN75160AN	DS75160AN	
SN75161N	DS75161AN	
SN75161AN	DS75161AN	
SN75162N	DS75162AN	
SN75162AN	DS75162AN	
SN75172	DS96172	
SN75172	µA96172	
SN75173	DS96173	
SN75173	µA96173	
SN75174	DS96174	
SN75174	µA96174	
SN75175	DS96175	
SN75175	µA96175	
SN75176A	DS75176A	
SN75176A	DS96176	
SN75176A	µA96176	
SN75176A	DS3695	
SN75176A		DS36F95
SN75177	DS96177	
SN75177	µA96177	
SN75177		DS96F177
SN75ALS056N	DS3696N	
SN75182J	DS8820AJ	
SN75182N	DS8820AN	
SN75183J	DS8830J	
SN75183N	DS8830N	
SN75188J	DS1488J	
SN75188N	DS1488N	
SN75189AJ	DS1489AJ	
SN75189AN	DS1489AN	
SN75189J	DS1489J	
SN75189N	DS1489N	
SN75208BJ	DS75208J	
SN75208J		DS75208J
SN75208N		DS75208N

The manufacturer's most current data sheets take precedence over this guide.

Texas Instruments to National's Interface (Continued)

TEXAS INSTRUMENTS (Continued)

Device Designation	National's Direct Replacement	National's Closest Replacement
SN75322		DS9643
SN75322		μA9643
SN75325J	DS75325J	
SN75325N	DS75325N	
SN75361AJG	DS75361J-8	
SN75361AP	DS75361N	
SN75363		DS9643
SN75363		μA9643
SN75365J	DS75365J	
SN75365N	DS75365N	
SN75369J		DS0026CJ-8
SN75369N		DS0026CN
SN75435		DS3668
SN75436		DS3658
SN75437A		DS3658
SN75438		DS3658
SN75440	DS3669	
SN75437ANE	DS3658N	
SN75437NE	DS3658N	
SN75438NE	DS3658N	
SN75450BJ	DS75450J	
SN75450BN	DS75450N	
SN75451BJG	DS75451J-8	
SN75451BP	DS75451N	
SN75452BJG	DS75452J-8	
SN75452BP	DS75452N	
SN75453BJG	DS75453J-8	
SN75453BP	DS75453N	
SN75454BJG	DS75454J-8	
SN75454BP	DS75454N	
SN75461JG	DS75461J-8	
SN75461P	DS75461N	
SN75462JG	DS75462J-8	
SN75462P	DS75462N	
SN75463JG	DS75463J-8	
SN75463P	DS75463N	
SN75464JG	DS75464J-8	
SN75464P	DS75464N	
SN75471JG		DS3631J-8
SN75471P		DS3631N

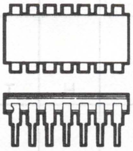
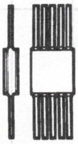
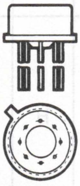
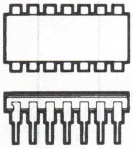
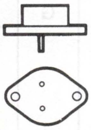
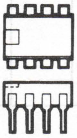
The manufacturer's most current data sheets take precedence over this guide.

TEXAS INSTRUMENTS (Continued)

Device Designation	National's Direct Replacement	National's Closest Replacement
SN75472JG		DS3632J-8
SN75472P		DS3632N
SN75473JG		DS3633J-8
SN75473P		DS3633N
SN75474P		DS3634N
SN75477JG		DS3632J-8
SN75477P		DS3632N
SN75480N	DS8880N	
SN75491AN		DS75491N
SN75491N	DS75491N	
SN75492AN		DS75492N
SN75492J	DS75492J	
SN75492N	DS75492N	
SN75494N		DS75494N
N8T13J	DS75121J	
N8T13N	DS75121N	
N8T23J	DS75123J	
N8T23N	DS75123N	
N8T24J	DS75124J	
N8T24N	DS75124N	
N8T26AJ	DS8T26AJ	
N8T26AN	DS8T26AN	
DS3680	DS3680	
DS8820AJ	DS8820AJ	
DS8820AN	DS8820AN	
DS8830J	DS8830J	
DS8830N	DS8830N	
DS8831J	DS8831J	
DS8831N	DS8831N	
DS8832J	DS8832J	
DS8832N	DS8832N	
μA9636A	DS9636A	
μA9636A	μA9636A	
μA9637A	DS9637A	
μA9637A	μA9637A	
μA9638	DS9638	
μA9638	μA9638	
μA9639	DS9639	
μA9639	μA9639	

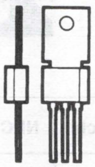
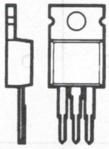
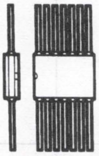
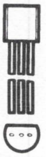
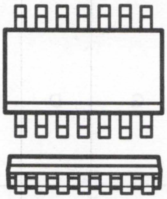
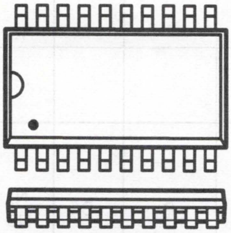
The manufacturer's most current data sheets take precedence over this guide.

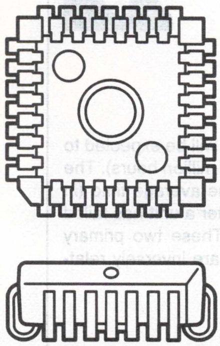
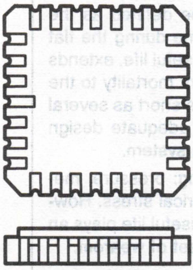
Industry Package Cross-Reference Guide

		NSC DP/DS	NSC µA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
	4/16 Lead Glass/Metal DIP	D	D	I	L		D	C	D	D
	Glass/Metal Flat Pack	F	F	Q	F	F, S	K	F		Q
	TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	S*, V1**		A	H
	8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J		G	D	J, J8
	TO-3 (Steel)	K			KS					K
	(Aluminum)	KC	K	DA	K	K				
	8-, 14- and 16-Lead Plastic DIP	N	T, P	V, A, B	P	P, N	E	P	C	N, N8

*With dual-in-line formed leads

**With radically formed leads

		NSC DP/DS	NSC μA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
	TO-202 (D-40, Durawatt)	P					KD			
	TO-220 3- & 5-Lead	T	U	U		KC		T	H	T
	TO-220 11-, 15- & 23-Lead	T								
	Low Temperature Glass Hermetic Flat Pack	W	F		F	W				
	TO-92 (Plastic)	Z	W	S	P	LP			H	Z
 	SO (Narrow Body)	M	S	D	D	D	M	MP	G	S
	SO (Wide Body)	WM				DW				

	NSC DP/DS	NSC μA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
 PCC	V	Q	A	FN	FN	Q	CP	L	
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	BJ	CG		

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

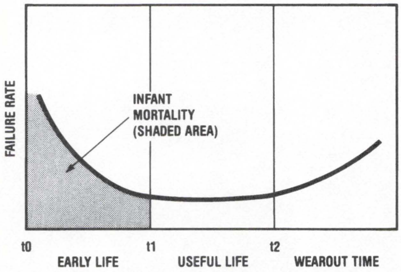


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

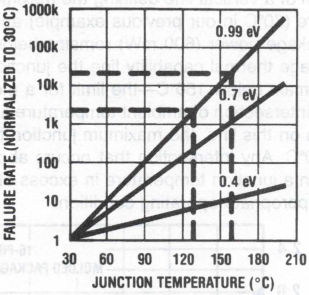

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

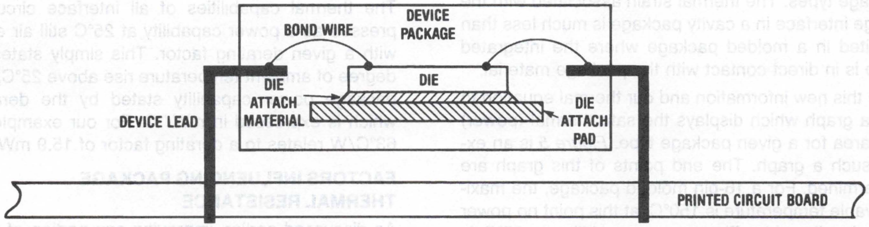

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

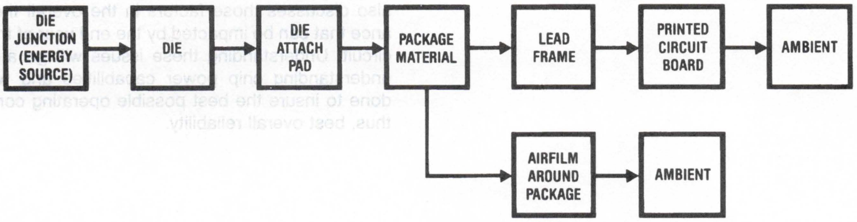

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D \text{ @ } 25°C = \frac{T_J(\text{max}) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = \frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

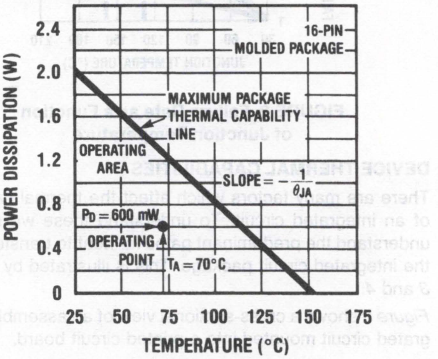

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

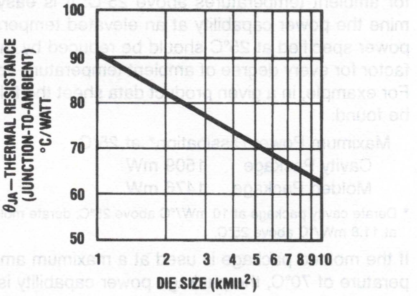

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

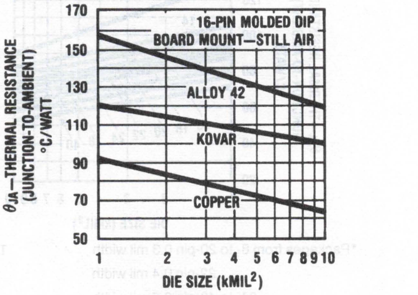

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

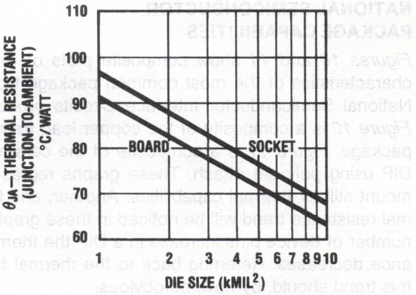

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

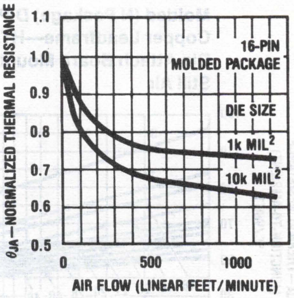

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

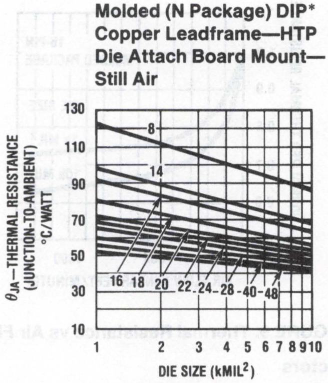
Maximum Power Dissipation* at 25°C

Cavity Package	1509 mW
Molded Package	1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70^\circ\text{C} = 1476\text{ mW} - (11.8\text{ mW}/^\circ\text{C}) \times (70^\circ\text{C} - 25^\circ\text{C}) = 945\text{ mW}$$



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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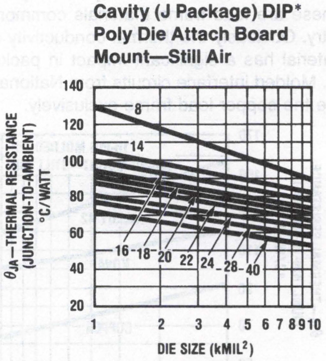
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/F/5280-11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

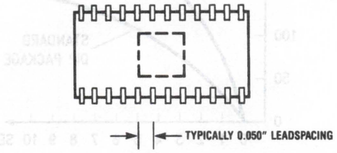
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliabilty

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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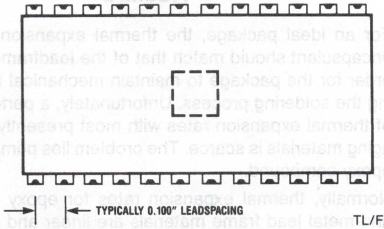
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

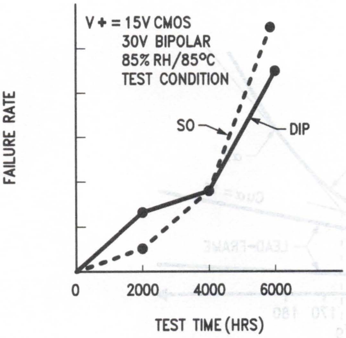

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

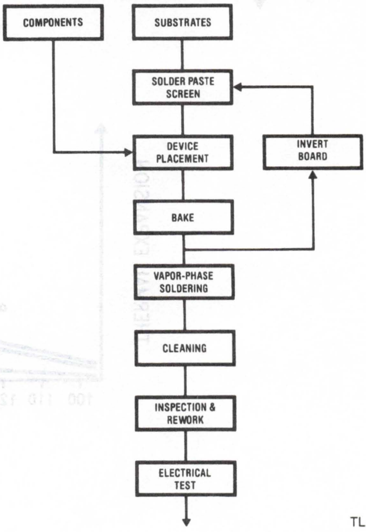
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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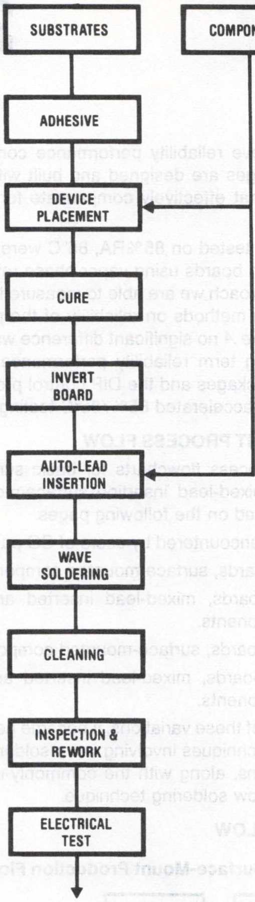
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766-5

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

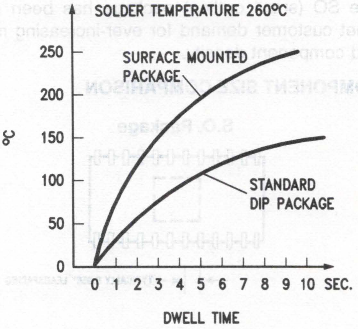


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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

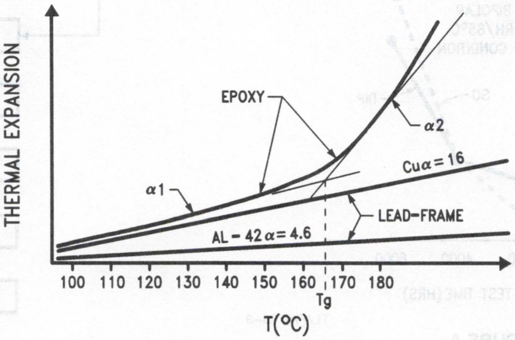

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package
Group 2 — SO packages vapor-phase reflow soldered on PC boards
Group 3–6 SO packages wave soldered on PC boards
Group 3 — dwell time 2 seconds
4 — dwell time 4 seconds
5 — dwell time 6 seconds
6 — dwell time 10 seconds

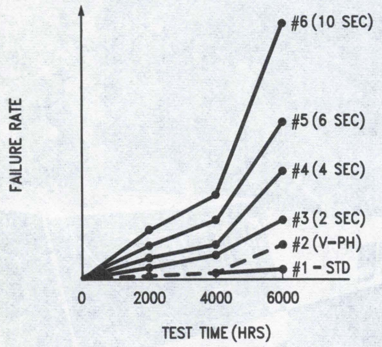

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement
- Fixed placement stations
- Boards indexed under head and respective components placed

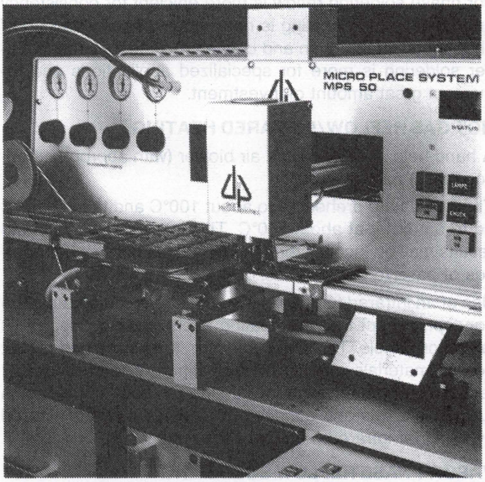
(b) Sequential placement
- Either a X-Y moving table system or a θ, X-Y moving pickup system used
- Individual components picked and placed onto boards

(c) Simultaneous placement
- Multiple pickup heads
- Whole array of components placed onto the PCB at the same time

(d) Sequential/simultaneous placement
- X–Y moving table, multiple pickup heads system
- Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

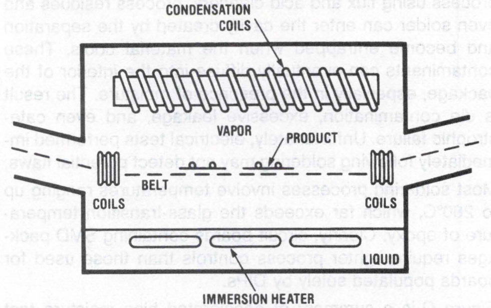
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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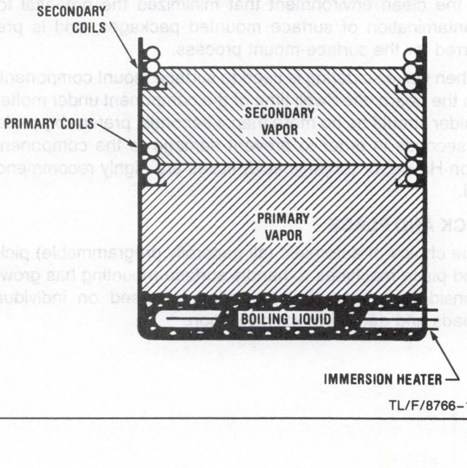
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

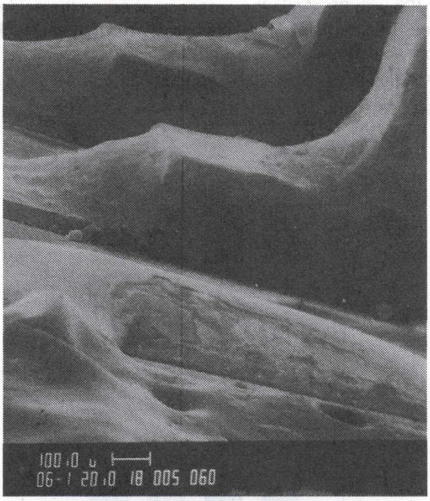
TL/F/8766-10

Batch-Fed Production Vapor-Phase Soldering Unit



TL/F/8766-11

Solder Joints on a SO-14 Package on PCB



TL/F/8766-12

Solder Joints on a SO-14 Package on PCB

100.0 u
06-1 20.0 20 005 060

TL/F/8766-13

PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed ⅛″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

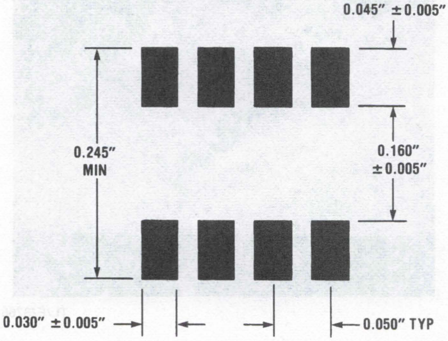
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

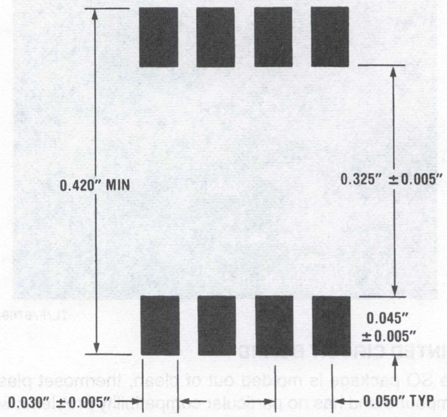
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16


0.045″ ±0.005″
0.245″ MIN
0.160″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

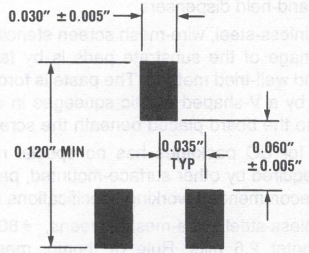
TL/F/8766–14

SO-16L, SO-20


0.420″ MIN
0.325″ ±0.005″
0.045″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

TL/F/8766–15

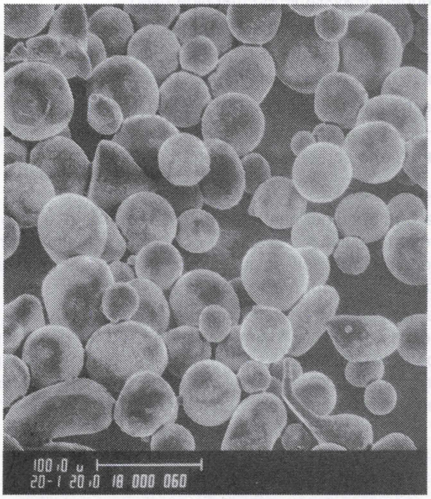
SOT-23


0.030″ ±0.005″
0.120″ MIN
0.035″ TYP
0.060″ ±0.005″

TL/F/8766–16

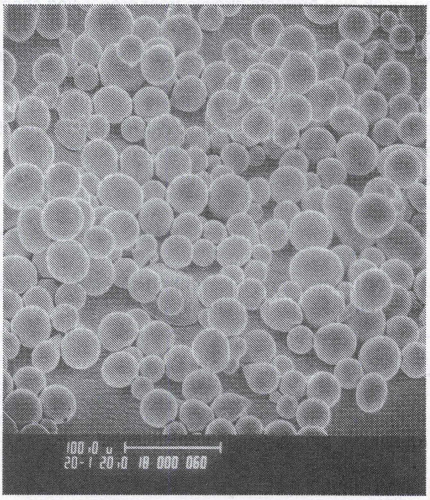
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)


100.0 u
20-1 20.0 18 000 060

TL/F/8766–17

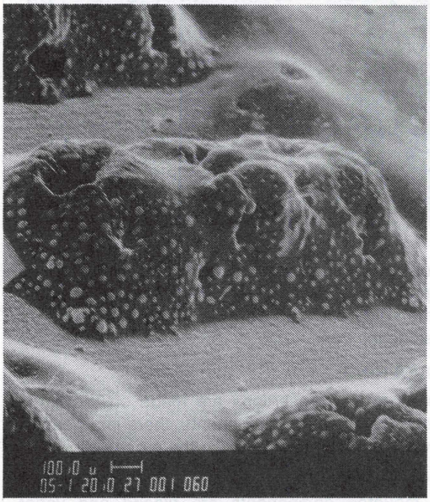
200 × Kester (63/37)


100.0 u
20-1 20.0 18 000 060

TL/F/8766–18

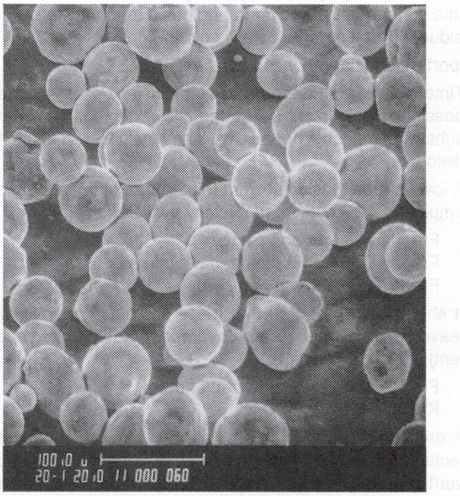
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads


100.0 u
05-1 20.0 27 001 060

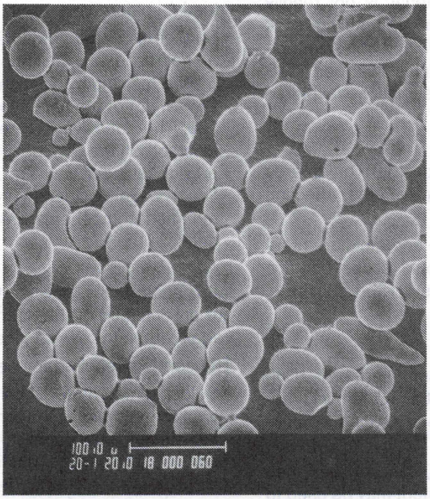
TL/F/8766–19

200 × Fry Metal (63/37)


100.0 u
20-1 20.0 11 000 060

TL/F/8766–20

200 ESL (63/37)


100.0 u
20-1 20.0 18 000 060

TL/F/8766–21

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

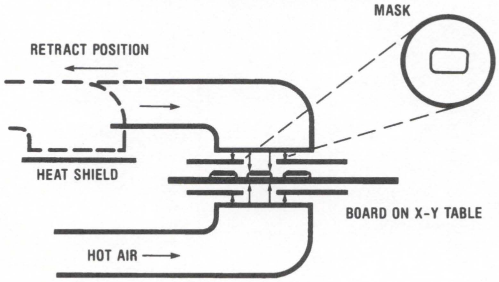
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

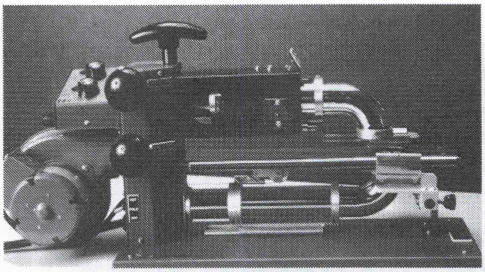
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766-22

Hot-Air Rework Machine



TL/F/8766-23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

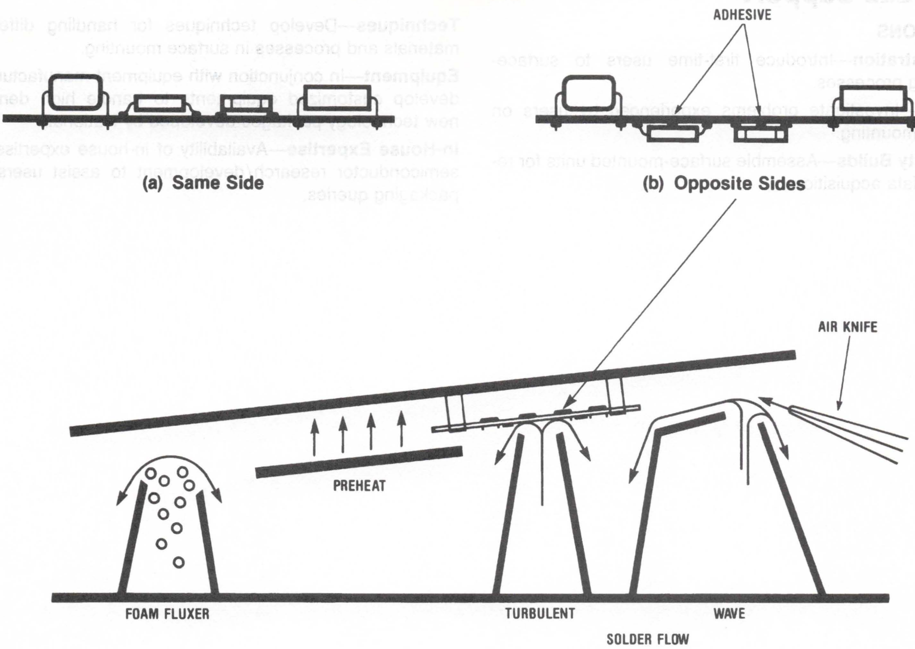
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



(a) Same Side

(b) Opposite Sides

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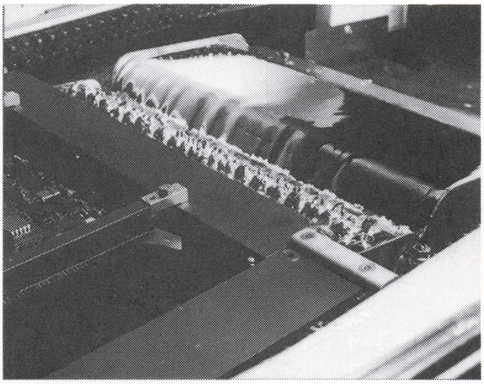
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766-25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

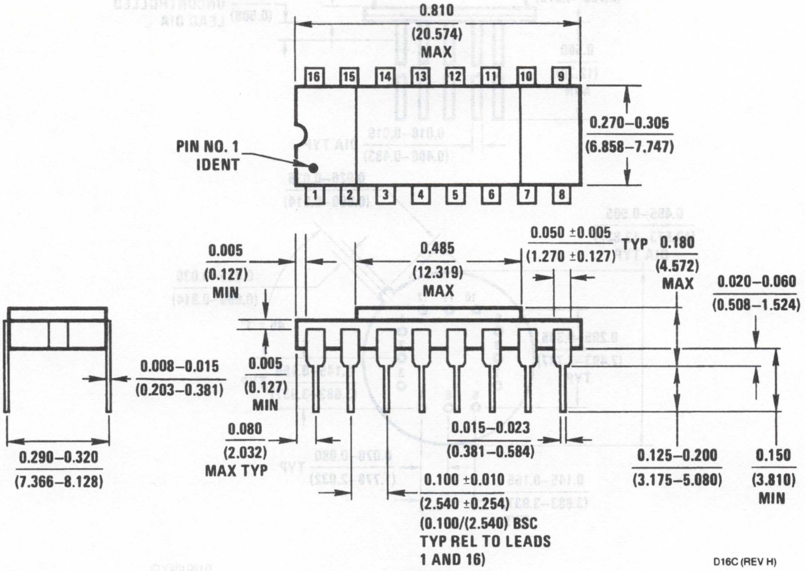
Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

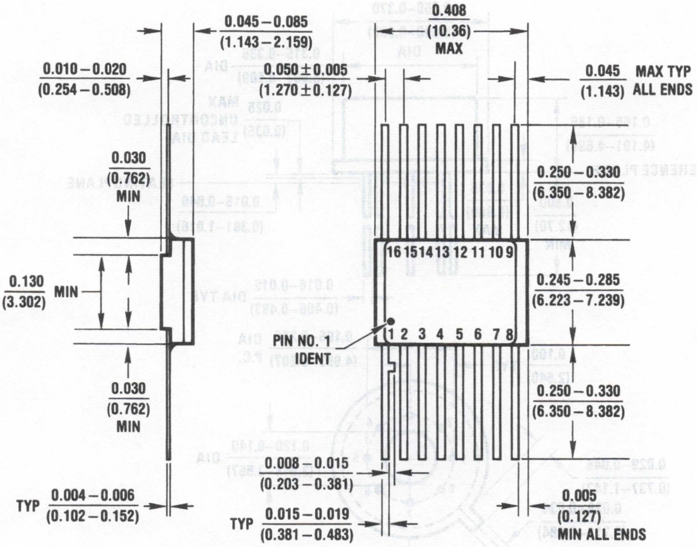
In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

All dimensions are in inches (millimeters)


0.810
(20.574)
MAX
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
PIN NO. 1
IDENT
0.270–0.305
(6.858–7.747)
0.005
(0.127)
MIN
0.485
(12.319)
MAX
0.050 ±0.005
(1.270 ±0.127)
TYP
0.180
(4.572)
MAX
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.005
(0.127)
MIN
0.080
(2.032)
MAX TYP
0.015–0.023
(0.381–0.584)
0.290–0.320
(7.366–8.128)
0.100 ±0.010
(2.540 ±0.254)
(0.100/(2.540) BSC
TYP REL TO LEADS
1 AND 16)
0.125–0.200
(3.175–5.080)
0.150
(3.810)
MIN

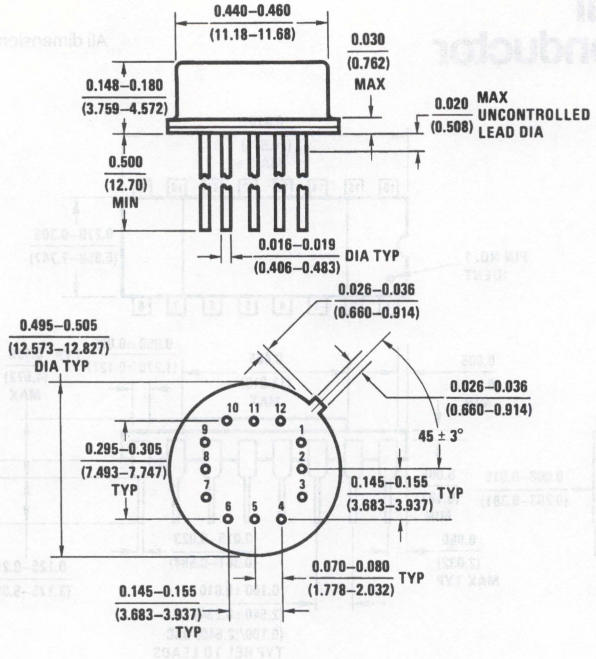
D16C (REV H)

NS Package D16C


0.045 – 0.085
(1.143 – 2.159)
0.408
(10.36)
MAX
0.010 – 0.020
(0.254 – 0.508)
0.050 ± 0.005
(1.270 ± 0.127)
0.045
(1.143)
MAX TYP
ALL ENDS
0.030
(0.762)
MIN
0.250 – 0.330
(6.350 – 8.382)
16 15 14 13 12 11 10 9
0.130
(3.302)
MIN
0.245 – 0.285
(6.223 – 7.239)
1 2 3 4 5 6 7 8
PIN NO. 1
IDENT
0.030
(0.762)
MIN
0.250 – 0.330
(6.350 – 8.382)
0.008 – 0.015
(0.203 – 0.381)
TYP
0.004 – 0.006
(0.102 – 0.152)
TYP
0.015 – 0.019
(0.381 – 0.483)
0.005
(0.127)
MIN ALL ENDS

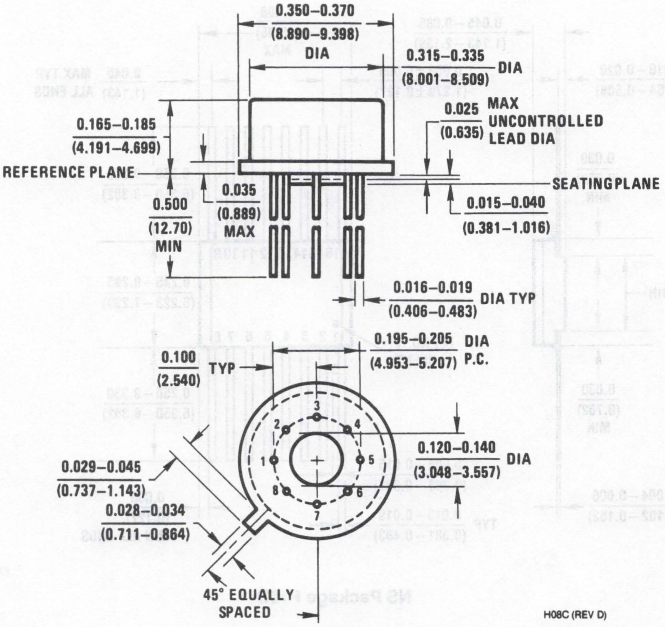
F16B (REV H)

NS Package F16B


0.440–0.460
(11.18–11.68)
0.030
(0.762)
MAX
0.148–0.180
(3.759–4.572)
0.020 MAX
(0.508) UNCONTROLLED LEAD DIA
0.500
(12.70)
MIN
0.016–0.019
(0.406–0.483) DIA TYP
0.026–0.036
(0.660–0.914)
0.495–0.505
(12.573–12.827)
DIA TYP
0.026–0.036
(0.660–0.914)
45 ± 3°
10 11 12
9
8
7
1
2
3
6 5 4
0.295–0.305
(7.493–7.747)
TYP
0.145–0.155
(3.683–3.937) TYP
0.070–0.080
(1.778–2.032) TYP
0.145–0.155
(3.683–3.937)
TYP

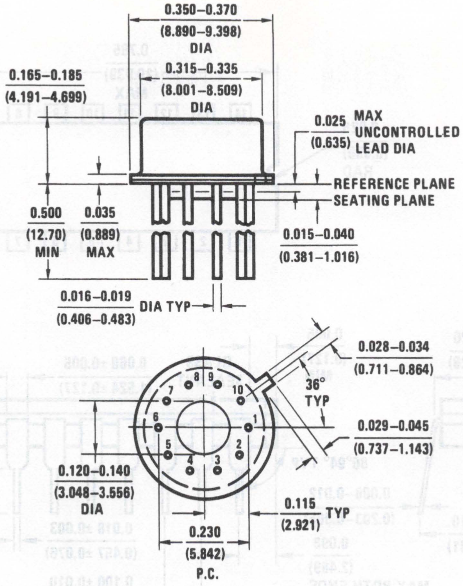
G12C (REV C)

NS Package G12C


0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509) DIA
0.025 MAX
(0.635) UNCONTROLLED LEAD DIA
0.165–0.185
(4.191–4.699)
REFERENCE PLANE
SEATING PLANE
0.035
(0.889)
MAX
0.500
(12.70)
MIN
0.015–0.040
(0.381–1.016)
0.016–0.019
(0.406–0.483) DIA TYP
0.195–0.205 DIA
(4.953–5.207) P.C.
0.100
(2.540) TYP
3
2
4
1
5
8
6
7
0.120–0.140
(3.048–3.557) DIA
0.029–0.045
(0.737–1.143)
0.028–0.034
(0.711–0.864)
45° EQUALLY
SPACED

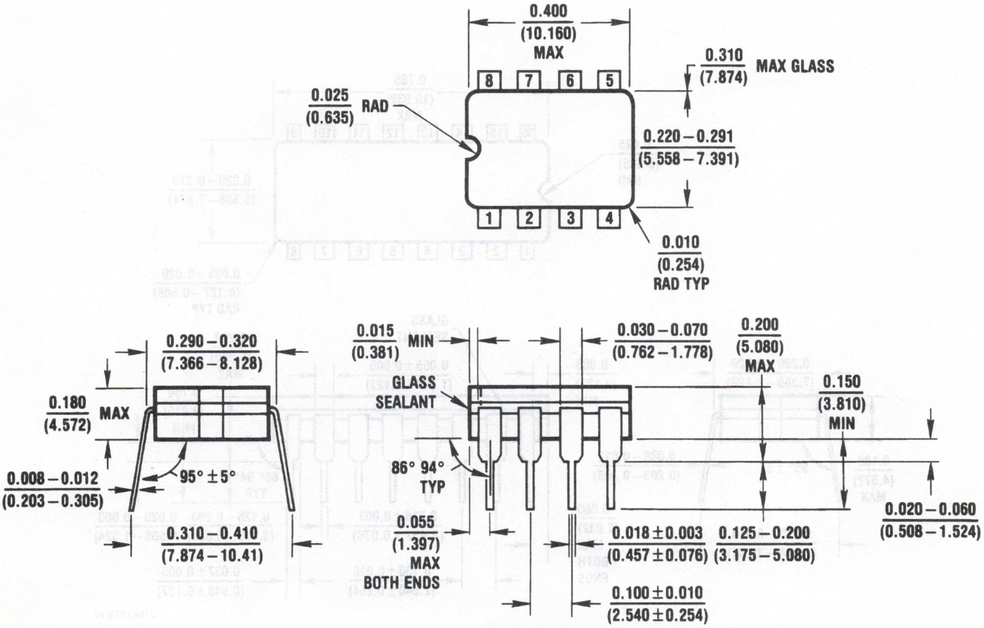
H08C (REV D)

NS Package H08C


0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509)
DIA
0.165–0.185
(4.191–4.699)
0.025 MAX
(0.635) UNCONTROLLED LEAD DIA
REFERENCE PLANE
SEATING PLANE
0.500
(12.70)
MIN
0.035
(0.889)
MAX
0.015–0.040
(0.381–1.016)
0.016–0.019
(0.406–0.483)
DIA TYP
0.028–0.034
(0.711–0.864)
36°
TYP
0.029–0.045
(0.737–1.143)
1
2
3
4
5
6
7
8
9
10
0.120–0.140
(3.048–3.556)
DIA
0.115
(2.921)
TYP
0.230
(5.842)
P.C.

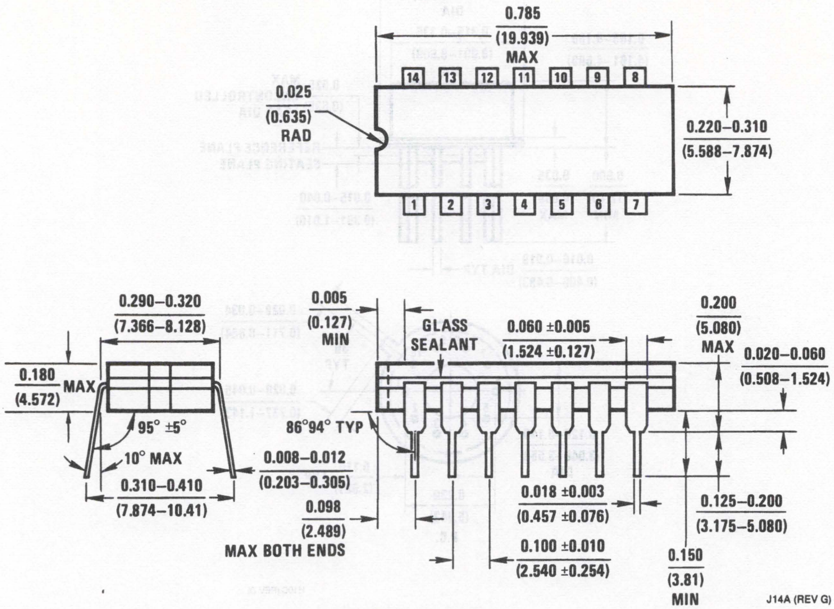
H10C (REV D)

NS Package H10C

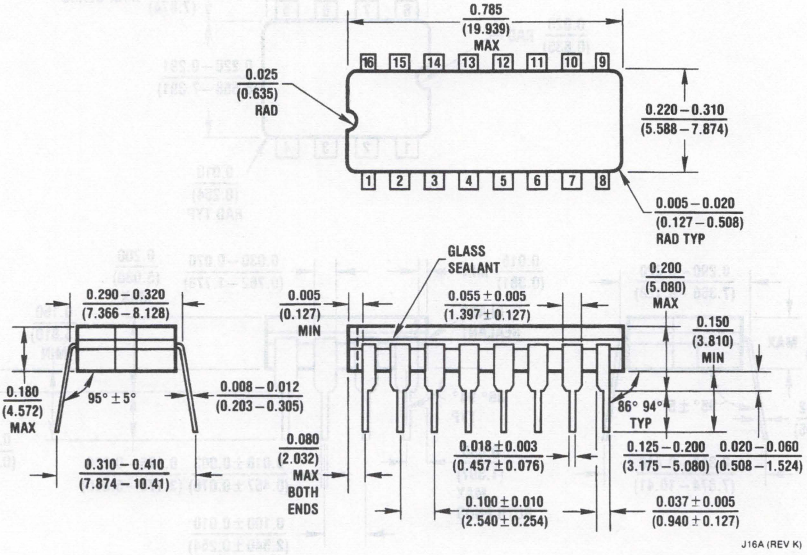

0.400
(10.160)
MAX
0.310
(7.874)
MAX GLASS
8
7
6
5
0.025
(0.635)
RAD
0.220 – 0.291
(5.558 – 7.391)
1
2
3
4
0.010
(0.254)
RAD TYP
0.290 – 0.320
(7.366 – 8.128)
0.180
(4.572)
MAX
0.008 – 0.012
(0.203 – 0.305)
95° ± 5°
0.310 – 0.410
(7.874 – 10.41)
0.015
(0.381)
MIN
GLASS SEALANT
86° 94°
TYP
0.055
(1.397)
MAX
BOTH ENDS
0.030 – 0.070
(0.762 – 1.778)
0.200
(5.080)
MAX
0.150
(3.810)
MIN
0.020 – 0.060
(0.508 – 1.524)
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.100 ± 0.010
(2.540 ± 0.254)

J08A (REV H)

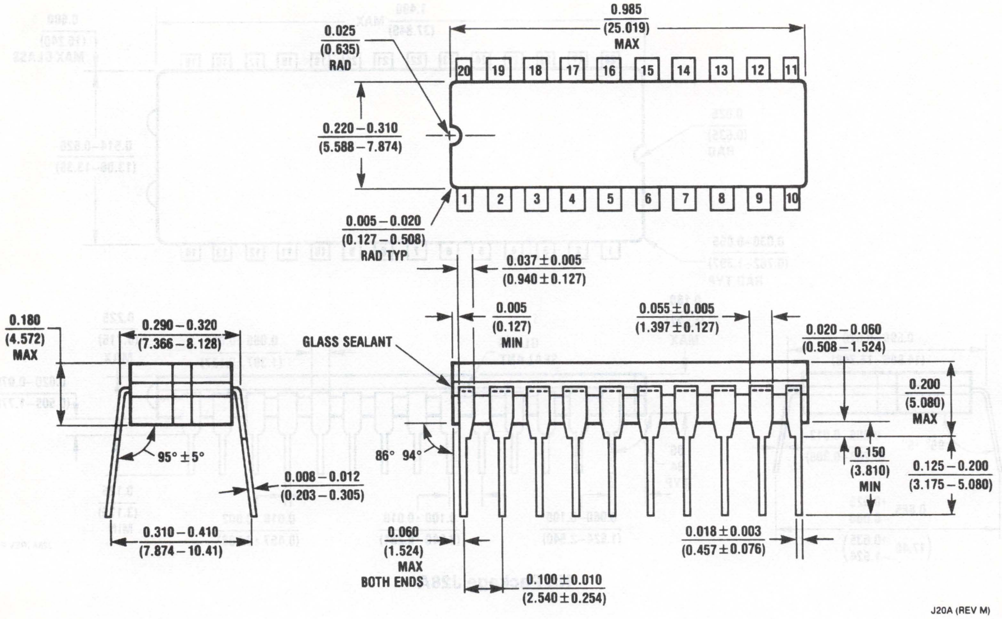
NS Package J08A


0.785
(19.939)
MAX
14
13
12
11
10
9
8
1
2
3
4
5
6
7
0.025
(0.635)
RAD
0.220–0.310
(5.588–7.874)
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
95° ±5°
10° MAX
0.310–0.410
(7.874–10.41)
0.005
(0.127)
MIN
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
0.200
(5.080)
MAX
0.020–0.060
(0.508–1.524)
86°94° TYP
0.008–0.012
(0.203–0.305)
0.098
(2.489)
MAX BOTH ENDS
0.018 ±0.003
(0.457 ±0.076)
0.100 ±0.010
(2.540 ±0.254)
0.125–0.200
(3.175–5.080)
0.150
(3.81)
MIN
J14A (REV G)

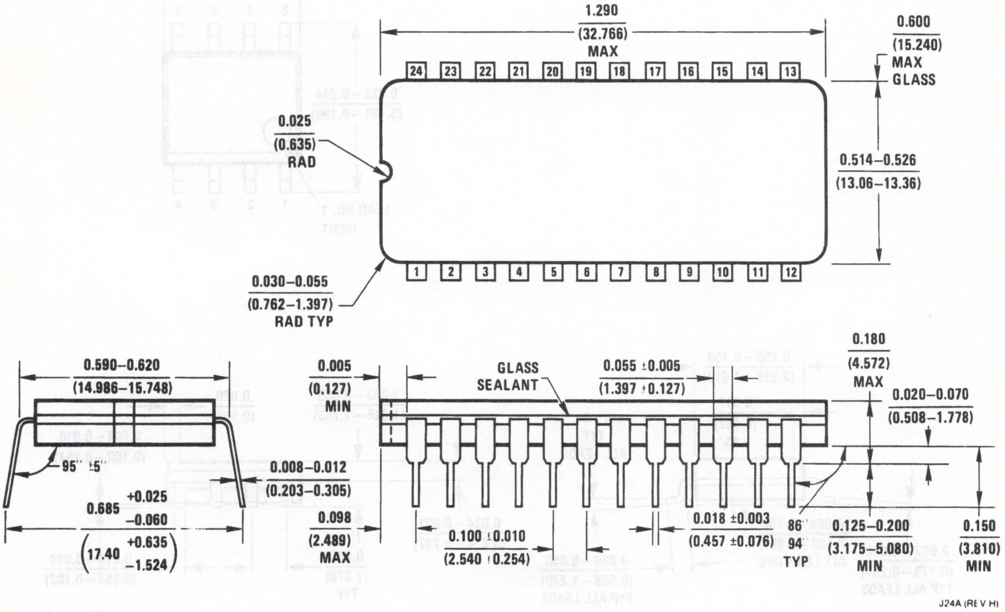
NS Package J14A


0.785
(19.939)
MAX
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.025
(0.635)
RAD
0.220 – 0.310
(5.588 – 7.874)
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
GLASS
SEALANT
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.200
(5.080)
MAX
0.150
(3.810)
MIN
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.310 – 0.410
(7.874 – 10.41)
0.080
(2.032)
MAX
BOTH
ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.100 ± 0.010
(2.540 ± 0.254)
0.037 ± 0.005
(0.940 ± 0.127)
J16A (REV K)

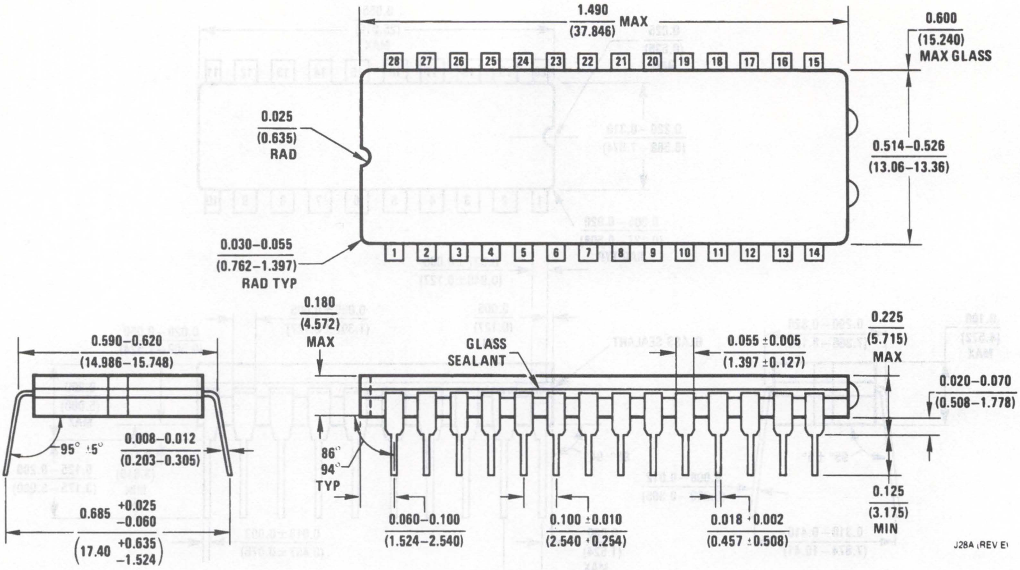
NS Package J16A


0.985
(25.019)
MAX
0.025
(0.635)
RAD
20 19 18 17 16 15 14 13 12 11
0.220 – 0.310
(5.588 – 7.874)
1 2 3 4 5 6 7 8 9 10
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
0.037 ± 0.005
(0.940 ± 0.127)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
0.180
(4.572)
MAX
0.290 – 0.320
(7.366 – 8.128)
GLASS SEALANT
0.200
(5.080)
MAX
95° ± 5°
86° 94°
0.150
(3.810)
MIN
0.125 – 0.200
(3.175 – 5.080)
0.008 – 0.012
(0.203 – 0.305)
0.310 – 0.410
(7.874 – 10.41)
0.060
(1.524)
MAX
BOTH ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
J20A (REV M)

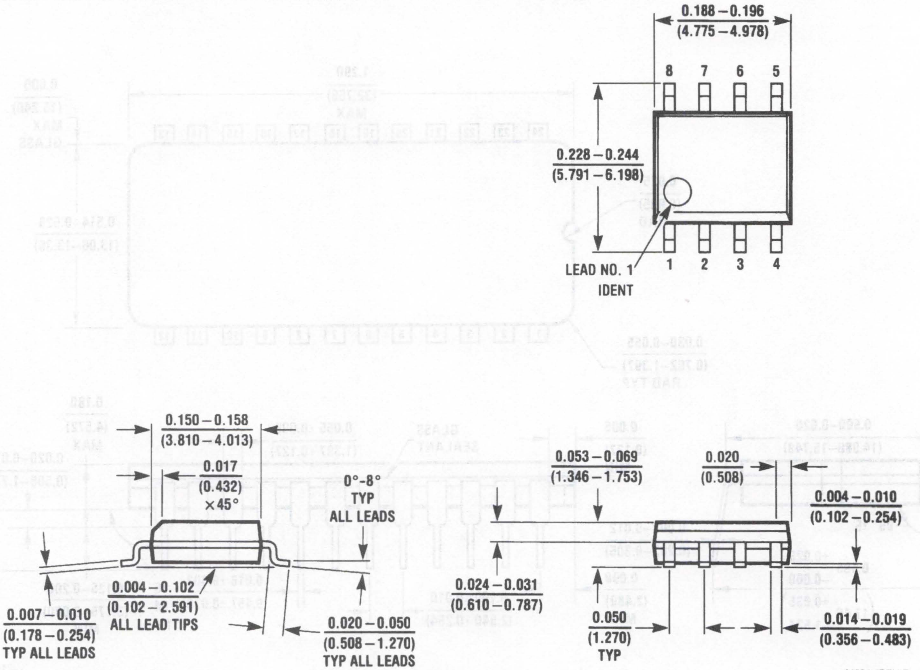
NS Package J20A


1.290
(32.766)
MAX
0.600
(15.240)
MAX
GLASS
24 23 22 21 20 19 18 17 16 15 14 13
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
1 2 3 4 5 6 7 8 9 10 11 12
0.030–0.055
(0.762–1.397)
RAD TYP
0.180
(4.572)
MAX
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.020–0.070
(0.508–1.778)
95° ±5°
0.008–0.012
(0.203–0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.098
(2.489)
MAX
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
86°
94°
TYP
0.125–0.200
(3.175–5.080)
MIN
0.150
(3.810)
MIN
J24A (REV H)

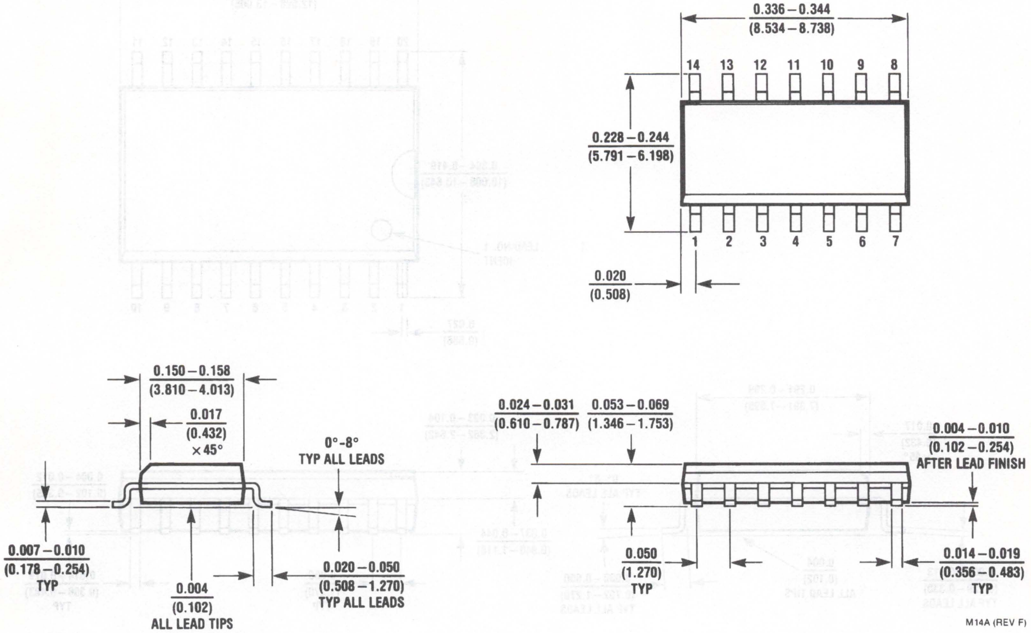
NS Package J24A


1.490
(37.846) MAX
0.600
(15.240)
MAX GLASS
28 27 26 25 24 23 22 21 20 19 18 17 16 15
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
0.030–0.055
(0.762–1.397)
RAD TYP
1 2 3 4 5 6 7 8 9 10 11 12 13 14
0.180
(4.572)
MAX
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.225
(5.715)
MAX
0.020–0.070
(0.508–1.778)
0.590–0.620
(14.986–15.748)
95° ±5°
0.008–0.012
(0.203–0.305)
86°
94°
TYP
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.060–0.100
(1.524–2.540)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.002
(0.457 ±0.508)
0.125
(3.175)
MIN
J28A (REV E)

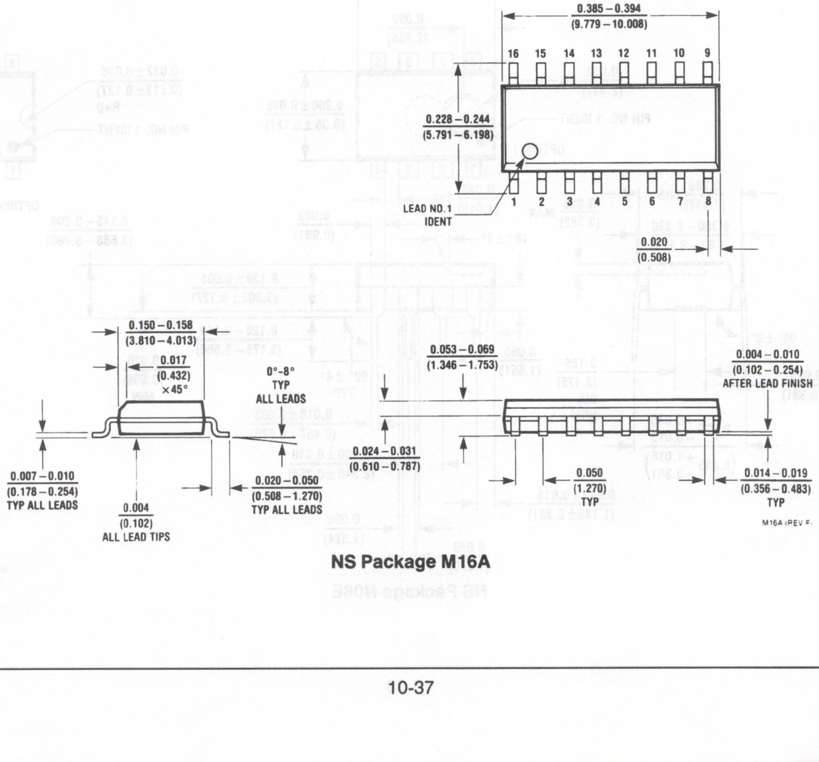
NS Package J28A


0.188 – 0.196
(4.775 – 4.978)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
LEAD NO. 1
IDENT
1 2 3 4
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
×45°
0°-8°
TYP
ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.020
(0.508)
0.004 – 0.010
(0.102 – 0.254)
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.004 – 0.102
(0.102 – 2.591)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.024 – 0.031
(0.610 – 0.787)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
M08A (REV F)

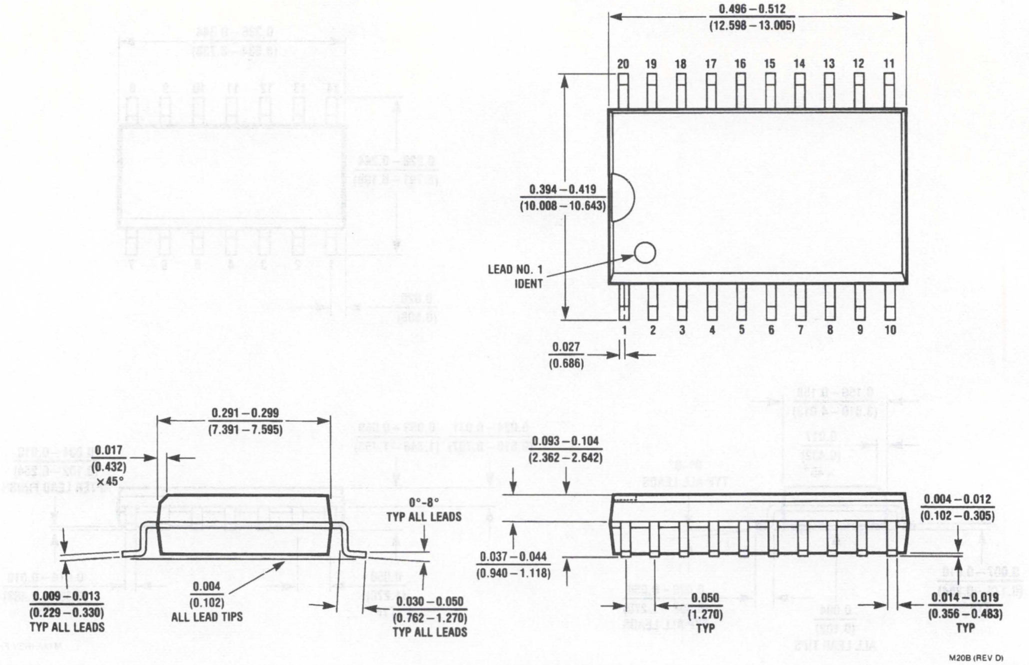
NS Package M08A


0.336 – 0.344
(8.534 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
1 2 3 4 5 6 7
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
× 45°
0°-8°
TYP ALL LEADS
0.024 – 0.031
(0.610 – 0.787)
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.007 – 0.010
(0.178 – 0.254)
TYP
0.004
(0.102)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14A (REV F)

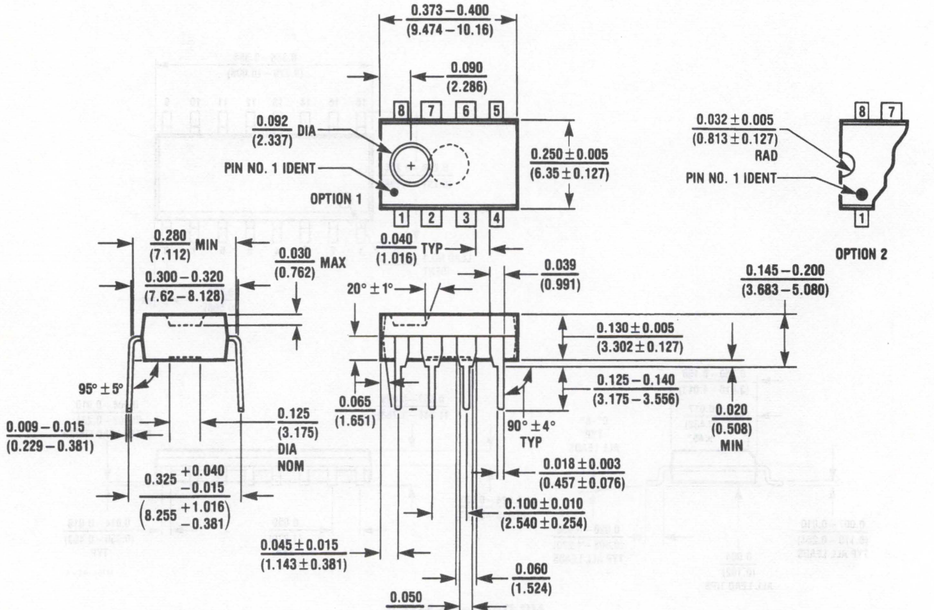
NS Package M14A


0.385 – 0.394
(9.779 – 10.008)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
LEAD NO.1
IDENT
1 2 3 4 5 6 7 8
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
× 45°
0°-8°
TYP
ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.024 – 0.031
(0.610 – 0.787)
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
0.004
(0.102)
ALL LEAD TIPS
M16A (REV F)

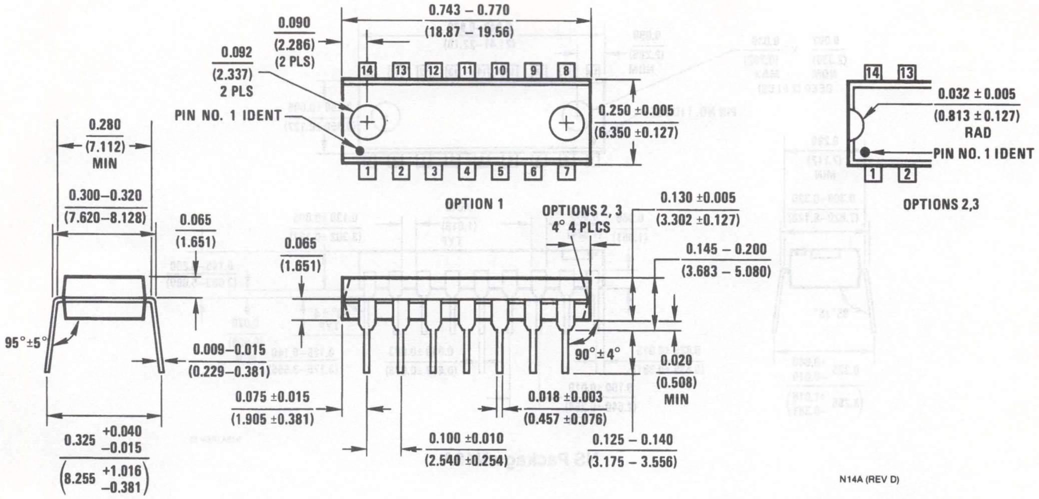
NS Package M16A


0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
0.394 – 0.419
(10.008 – 10.643)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8 9 10
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
×45°
0°–8°
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
0.037 – 0.044
(0.940 – 1.118)
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M20B (REV D)

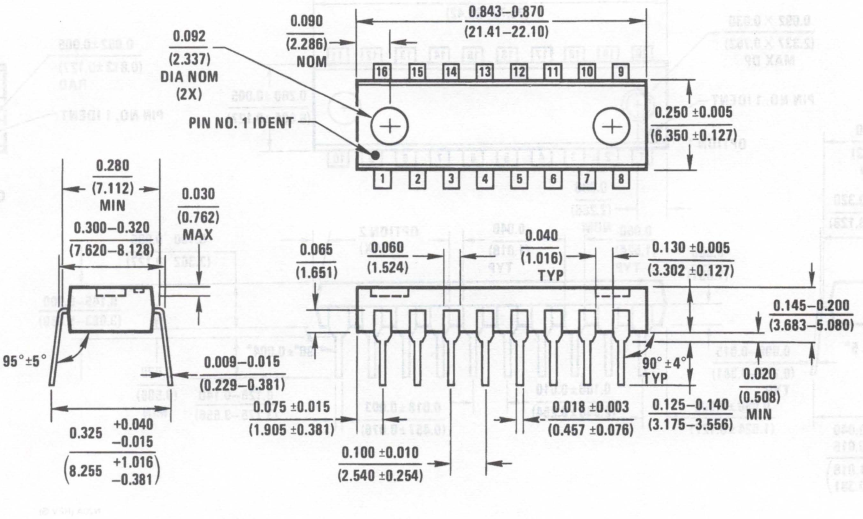
NS Package M20B


0.373 – 0.400
(9.474 – 10.16)
0.090
(2.286)
8 7 6 5
0.092
(2.337) DIA
PIN NO. 1 IDENT
OPTION 1
1 2 3 4
0.250 ± 0.005
(6.35 ± 0.127)
8 7
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
1
OPTION 2
0.280
(7.112) MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762) MAX
0.040
(1.016) TYP
20° ± 1°
0.039
(0.991)
0.145 – 0.200
(3.683 – 5.080)
0.130 ± 0.005
(3.302 ± 0.127)
95° ± 5°
0.065
(1.651)
0.125 – 0.140
(3.175 – 3.556)
0.009 – 0.015
(0.229 – 0.381)
0.125
(3.175)
DIA
NOM
90° ± 4°
TYP
0.020
(0.508)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 ± 0.015
(1.143 ± 0.381)
0.060
(1.524)
0.050
(1.270)
N08E (REV F)

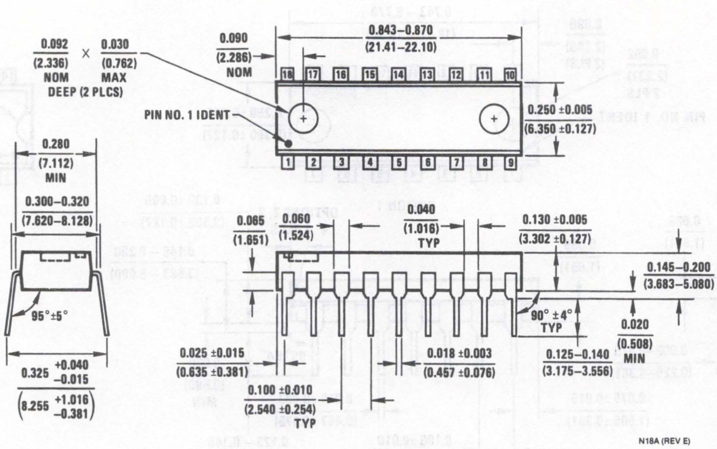
NS Package N08E


0.743 – 0.770
(18.87 – 19.56)
0.090
(2.286)
(2 PLS)
0.092
(2.337)
2 PLS
PIN NO. 1 IDENT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
0.250 ±0.005
(6.350 ±0.127)
OPTION 1
14
13
1
2
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
OPTIONS 2,3
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.065
(1.651)
0.065
(1.651)
OPTIONS 2, 3
4° 4 PLCS
0.130 ±0.005
(3.302 ±0.127)
0.145 – 0.200
(3.683 – 5.080)
95°±5°
0.009–0.015
(0.229–0.381)
90° ± 4°
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ±0.010
(2.540 ±0.254)
0.125 – 0.140
(3.175 – 3.556)
N14A (REV D)

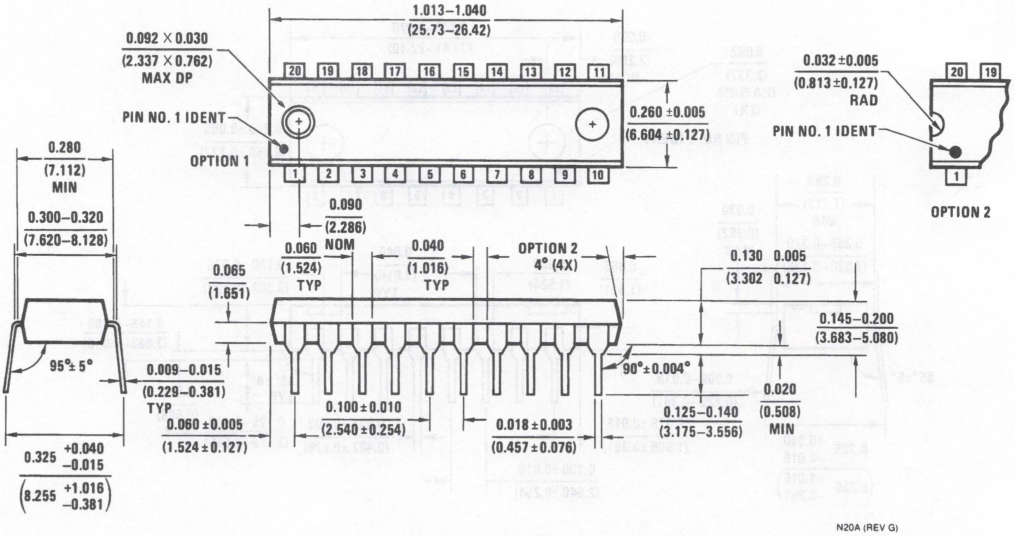
NS Package N14A


0.843–0.870
(21.41–22.10)
0.090
(2.286)
NOM
0.092
(2.337)
DIA NOM
(2X)
PIN NO. 1 IDENT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.030
(0.762)
MAX
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
95°±5°
0.009–0.015
(0.229–0.381)
90° ±4°
TYP
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ±0.010
(2.540 ±0.254)
N16A (REV E)

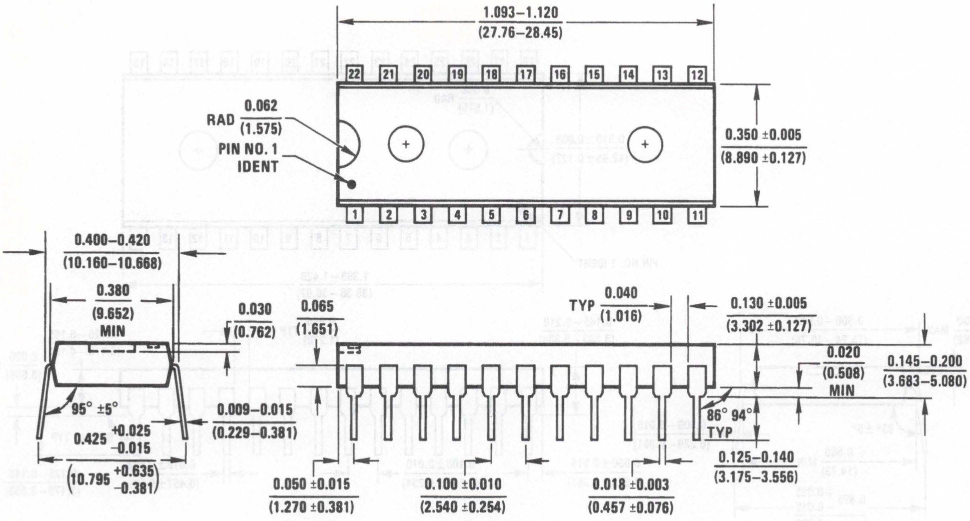
NS Package N16A


0.092 (2.336) NOM × 0.030 (0.762) MAX DEEP (2 PLCS)
0.090 (2.286) NOM
0.843–0.870 (21.41–22.10)
18 17 16 15 14 13 12 11 10
1 2 3 4 5 6 7 8 9
PIN NO. 1 IDENT
0.250 ±0.005 (6.350 ±0.127)
0.280 (7.112) MIN
0.300–0.320 (7.620–8.128)
95° ±5°
0.325 +0.040 −0.015 (8.255 +1.016 −0.381)
0.065 (1.651)
0.060 (1.524)
0.040 (1.016) TYP
0.130 ±0.005 (3.302 ±0.127)
0.145–0.200 (3.683–5.080)
90° ±4° TYP
0.020 (0.508) MIN
0.125–0.140 (3.175–3.556)
0.025 ±0.015 (0.635 ±0.381)
0.018 ±0.003 (0.457 ±0.076)
0.100 ±0.010 (2.540 ±0.254) TYP
N18A (REV E)

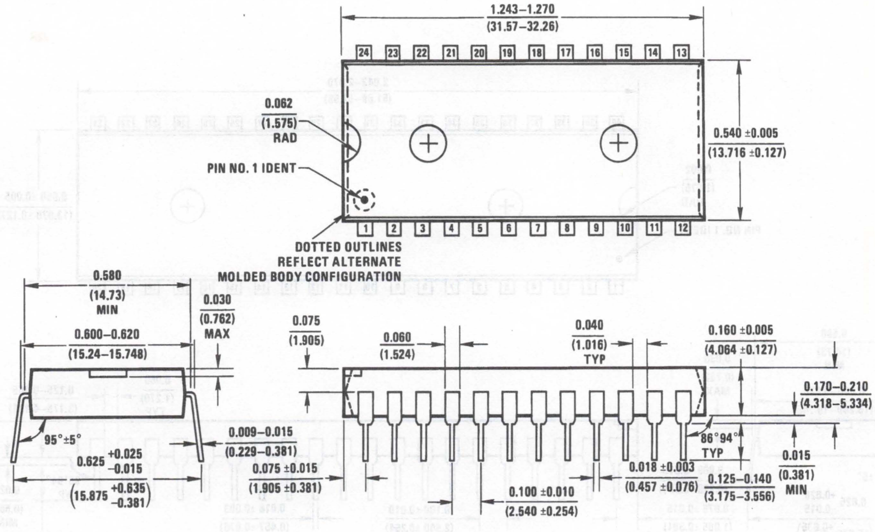
NS Package N18A


1.013–1.040 (25.73–26.42)
0.092 × 0.030 (2.337 × 0.762) MAX DP
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
PIN NO. 1 IDENT
OPTION 1
0.260 ±0.005 (6.604 ±0.127)
0.032 ±0.005 (0.813 ±0.127) RAD
PIN NO. 1 IDENT
20 19
1
OPTION 2
0.280 (7.112) MIN
0.300–0.320 (7.620–8.128)
0.090 (2.286) NOM
0.065 (1.651)
0.060 (1.524) TYP
0.040 (1.016) TYP
OPTION 2 4° (4X)
0.130 0.005 (3.302 0.127)
0.145–0.200 (3.683–5.080)
95° ± 5°
0.009–0.015 (0.229–0.381) TYP
90° ± 0.004°
0.020 (0.508) MIN
0.125–0.140 (3.175–3.556)
0.100 ± 0.010 (2.540 ± 0.254)
0.060 ± 0.005 (1.524 ± 0.127)
0.018 ± 0.003 (0.457 ± 0.076)
0.325 +0.040 −0.015 (8.255 +1.016 −0.381)
N20A (REV G)

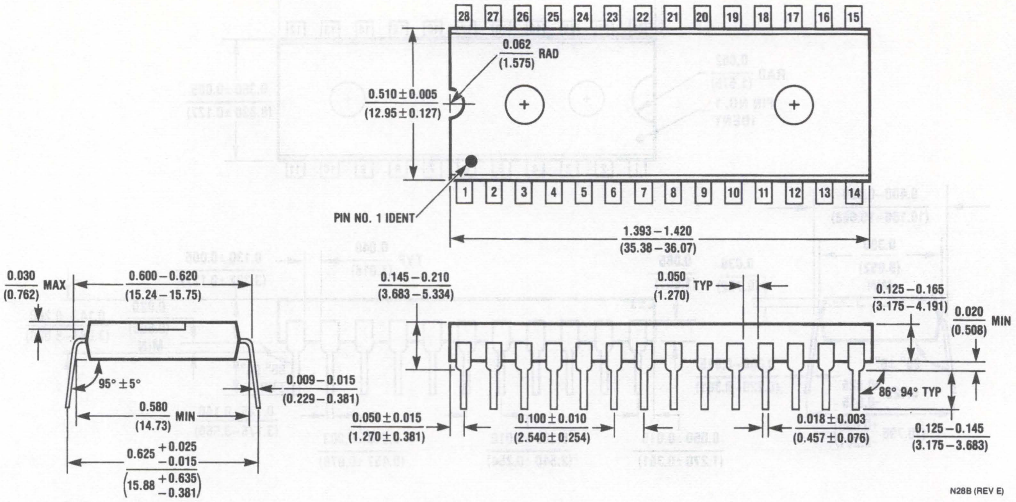
NS Package N20A


1.093–1.120
(27.76–28.45)
22 21 20 19 18 17 16 15 14 13 12
RAD 0.062
(1.575)
PIN NO. 1
IDENT
0.350 ±0.005
(8.890 ±0.127)
1 2 3 4 5 6 7 8 9 10 11
0.400–0.420
(10.160–10.668)
0.380
(9.652)
MIN
0.030
(0.762)
0.065
(1.651)
TYP 0.040
(1.016)
0.130 ±0.005
(3.302 ±0.127)
0.020
(0.508)
MIN
0.145–0.200
(3.683–5.080)
95° ±5°
0.009–0.015
(0.229–0.381)
0.425 +0.025 −0.015
(10.795 +0.635 −0.381)
86° 94°
TYP
0.125–0.140
(3.175–3.556)
0.050 ±0.015
(1.270 ±0.381)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
N22A (REV D)

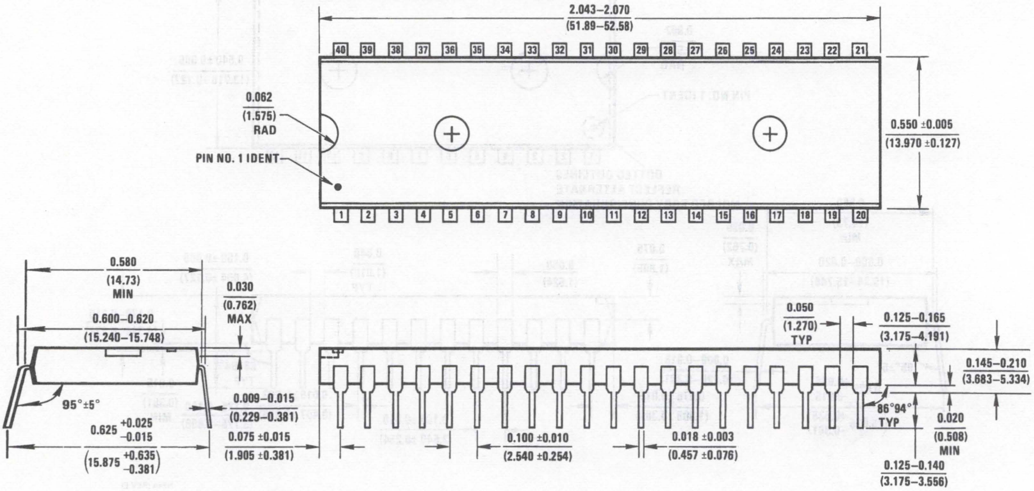
NS Package N22A


1.243–1.270
(31.57–32.26)
24 23 22 21 20 19 18 17 16 15 14 13
0.062
(1.575)
RAD
PIN NO. 1 IDENT
0.540 ±0.005
(13.716 ±0.127)
1 2 3 4 5 6 7 8 9 10 11 12
DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION
0.580
(14.73)
MIN
0.030
(0.762)
MAX
0.600–0.620
(15.24–15.748)
0.075
(1.905)
0.060
(1.524)
0.040
(1.016)
TYP
0.160 ±0.005
(4.064 ±0.127)
0.170–0.210
(4.318–5.334)
95°±5°
0.009–0.015
(0.229–0.381)
0.625 +0.025 −0.015
(15.875 +0.635 −0.381)
0.075 ±0.015
(1.905 ±0.381)
86°94°
TYP
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.015
(0.381)
MIN
0.100 ±0.010
(2.540 ±0.254)
N24A (REV E)

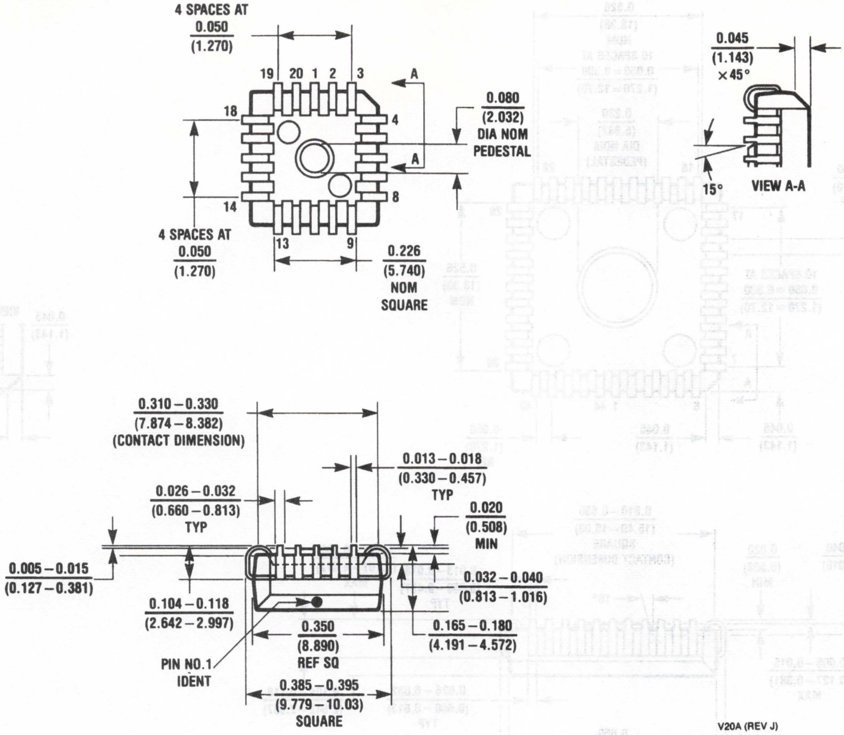
NS Package N24A


28
27
26
25
24
23
22
21
20
19
18
17
16
15
0.062
(1.575)
RAD
0.510 ± 0.005
(12.95 ± 0.127)
PIN NO. 1 IDENT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
1.393 – 1.420
(35.38 – 36.07)
0.030
(0.762)
MAX
0.600 – 0.620
(15.24 – 15.75)
0.145 – 0.210
(3.683 – 5.334)
0.050
(1.270)
TYP
0.125 – 0.165
(3.175 – 4.191)
0.020
(0.508)
MIN
95° ± 5°
0.009 – 0.015
(0.229 – 0.381)
0.580
(14.73)
MIN
0.050 ± 0.015
(1.270 ± 0.381)
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
86° 94° TYP
0.125 – 0.145
(3.175 – 3.683)
0.625 +0.025 −0.015
(15.88 +0.635 −0.381)
N28B (REV E)

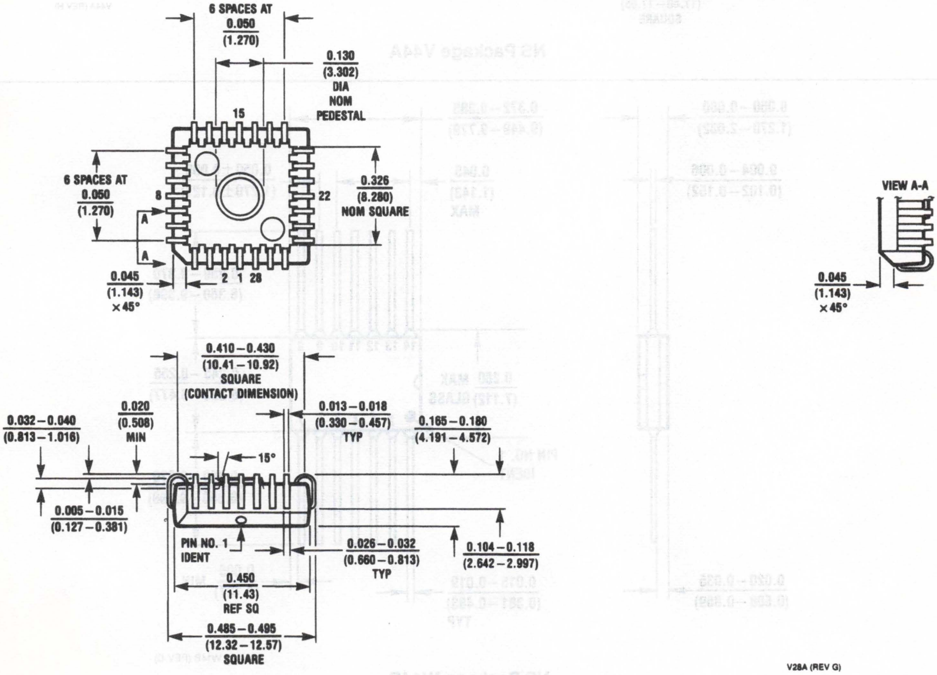
NS Package N28B


2.043–2.070
(51.89–52.58)
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
0.062
(1.575)
RAD
PIN NO. 1 IDENT
0.550 ±0.005
(13.970 ±0.127)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
0.580
(14.73)
MIN
0.030
(0.762)
MAX
0.600–0.620
(15.240–15.748)
0.050
(1.270)
TYP
0.125–0.165
(3.175–4.191)
0.145–0.210
(3.683–5.334)
95°±5°
0.009–0.015
(0.229–0.381)
86°94°
TYP
0.020
(0.508)
MIN
0.625 +0.025 −0.015
(15.875 +0.635 −0.381)
0.075 ±0.015
(1.905 ±0.381)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
N40A (REV E)

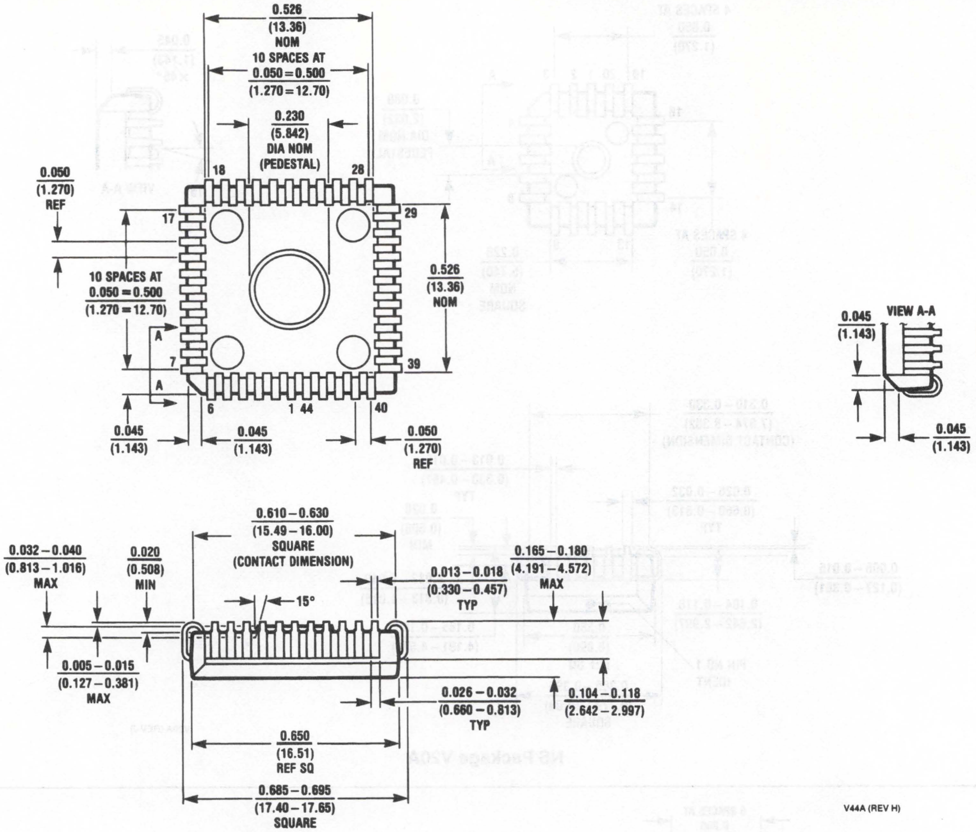
NS Package N40A


4 SPACES AT
0.050
(1.270)
19
20
1
2
3
A
18
4
A
0.080
(2.032)
DIA NOM
PEDESTAL
14
8
4 SPACES AT
0.050
(1.270)
13
9
0.226
(5.740)
NOM
SQUARE
0.045
(1.143)
×45°
15°
VIEW A-A
0.310 – 0.330
(7.874 – 8.382)
(CONTACT DIMENSION)
0.013 – 0.018
(0.330 – 0.457)
TYP
0.026 – 0.032
(0.660 – 0.813)
TYP
0.020
(0.508)
MIN
0.005 – 0.015
(0.127 – 0.381)
0.032 – 0.040
(0.813 – 1.016)
0.104 – 0.118
(2.642 – 2.997)
0.350
(8.890)
REF SQ
0.165 – 0.180
(4.191 – 4.572)
PIN NO.1
IDENT
0.385 – 0.395
(9.779 – 10.03)
SQUARE
V20A (REV J)

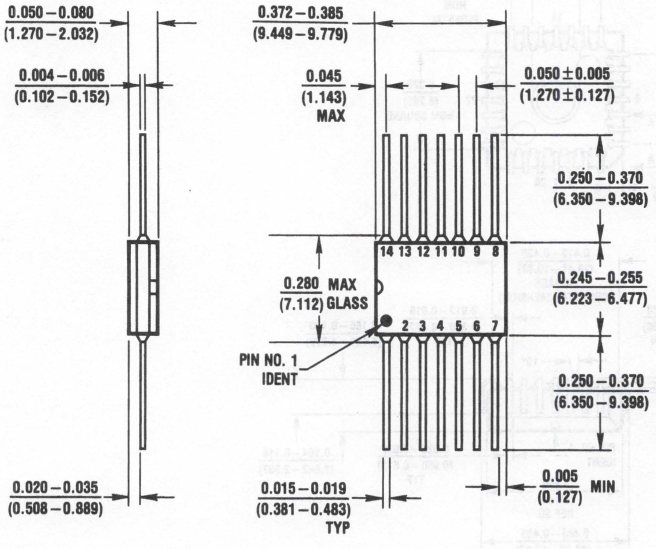
NS Package V20A


6 SPACES AT
0.050
(1.270)
0.130
(3.302)
DIA
NOM
PEDESTAL
15
6 SPACES AT
0.050
(1.270)
8
22
0.326
(8.280)
NOM SQUARE
A
A
2
1
28
0.045
(1.143)
×45°
VIEW A-A
0.045
(1.143)
×45°
0.410 – 0.430
(10.41 – 10.92)
SQUARE
(CONTACT DIMENSION)
0.032 – 0.040
(0.813 – 1.016)
0.020
(0.508)
MIN
0.013 – 0.018
(0.330 – 0.457)
TYP
0.165 – 0.180
(4.191 – 4.572)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.104 – 0.118
(2.642 – 2.997)
0.450
(11.43)
REF SQ
0.485 – 0.495
(12.32 – 12.57)
SQUARE
V28A (REV G)

NS Package V28A


0.526
(13.36)
NOM
10 SPACES AT
0.050 = 0.500
(1.270 = 12.70)
0.230
(5.842)
DIA NOM
(PEDESTAL)
18
28
0.050
(1.270)
REF
17
29
10 SPACES AT
0.050 = 0.500
(1.270 = 12.70)
0.526
(13.36)
NOM
A
7
A
39
6
1 44
40
0.045
(1.143)
0.045
(1.143)
0.050
(1.270)
REF
0.045
(1.143)
VIEW A-A
0.045
(1.143)
0.610 – 0.630
(15.49 – 16.00)
SQUARE
(CONTACT DIMENSION)
0.032 – 0.040
(0.813 – 1.016)
MAX
0.020
(0.508)
MIN
15°
0.013 – 0.018
(0.330 – 0.457)
TYP
0.165 – 0.180
(4.191 – 4.572)
MAX
0.005 – 0.015
(0.127 – 0.381)
MAX
0.026 – 0.032
(0.660 – 0.813)
TYP
0.104 – 0.118
(2.642 – 2.997)
0.650
(16.51)
REF SQ
0.685 – 0.695
(17.40 – 17.65)
SQUARE
V44A (REV H)

NS Package V44A


0.050 – 0.080
(1.270 – 2.032)
0.004 – 0.006
(0.102 – 0.152)
0.372 – 0.385
(9.449 – 9.779)
0.045
(1.143)
MAX
0.050 ± 0.005
(1.270 ± 0.127)
0.250 – 0.370
(6.350 – 9.398)
14 13 12 11 10 9 8
0.280 MAX
(7.112) GLASS
0.245 – 0.255
(6.223 – 6.477)
2 3 4 5 6 7
PIN NO. 1
IDENT
0.250 – 0.370
(6.350 – 9.398)
0.020 – 0.035
(0.508 – 0.889)
0.015 – 0.019
(0.381 – 0.483)
TYP
0.005
(0.127)
MIN
W14B (REV D)

NS Package W14B

NOTES

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